30 V, 3 A, Low V_{CE(sat)} NPN Transistor

ON Semiconductor's e^2 PowerEdge family of low $V_{CE(sat)}$ transistors are miniature surface mount devices featuring ultra low saturation voltage ($V_{CE(sat)}$) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical application are DC-DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e²PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

Features

- AEC-Q101 Qualified and PPAP Capable
- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- These are Pb-Free Devices*



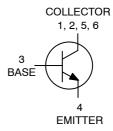
ON Semiconductor®

http://onsemi.com

30 VOLTS 3.0 AMPS NPN LOW $V_{CE(sat)}$ TRANSISTOR EQUIVALENT $R_{DS(on)}$ 100 m Ω



TSOP-6 CASE 318G STYLE 6



DEVICE MARKING



VS7 = Specific Device Code

M = Date Code

= Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
NSS30201MR6T1G	TSOP-6 (Pb-Free)	3,000 / Tape & Reel
SNSS30201MR6T1G	TSOP-6 (Pb-Free)	3,000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure. BRD8011/D.

^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V _{CEO}	30	V
Collector-Base Voltage	V _{CBO}	50	V
Emitter-Base Voltage	V _{EBO}	5.0	V
Collector Current – Continuous	I _C	2.0	Α
Collector Current - Peak	I _{CM}	3.0	Α

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation T _A = 25°C Derate above 25°C	P _D (Note 1)	535 4.3	mW mW/°C
Thermal Resistance, Junction-to-Ambient	R _{θJA} (Note 1)	234	°C/W
Total Device Dissipation T _A = 25°C Derate above 25°C	P _D (Note 2)	1.180 9.4	W mW/°C
Thermal Resistance, Junction-to-Ambient	R _{θJA} (Note 2)	106	°C/W
Thermal Resistance, Junction-to-Lead #1	R _{θJL} (Note 1) R _{θJL} (Note 2)	110 50	°C/W °C/W
Total Device Dissipation (Single Pulse < 10 s)	P _{Dsingle} (Notes 2 and 3)	1.75	W
Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. FR-4 with 1 oz and 3.9 mm² of copper area.

2. FR-4 with 1 oz and 645 mm² of copper area.

- 3. Refer to Figure 8.

ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS			•	1	•
Collector – Emitter Breakdown Voltage (I _C = 10 mA, I _B = 0)	V _(BR) CEO	30	-	-	V
Collector-Base Breakdown Voltage (I _C = 0.1 mA, I _E = 0)	V _{(BR)CBO}	50	-	-	V
Emitter – Base Breakdown Voltage (I _E = 0.1 mA, I _C = 0)	V _{(BR)EBO}	5.0	-	-	V
Collector Cutoff Current $(V_{CB} = 30 \text{ V}, I_E = 0)$	I _{CBO}	-	-	0.1	μΑ
Collector–Emitter Cutoff Current (V _{CES} = 30 V)	I _{CES}	=	-	0.1	μΑ
Emitter Cutoff Current (V _{EB} = 4.0 V)	I _{EBO}	-		0.1	μΑ
ON CHARACTERISTICS	<u> </u>				
DC Current Gain (Note 4) $ (I_C = 1.0 \text{ mA}, V_{CE} = 5.0 \text{ V}) $ $ (I_C = 0.5 \text{ A}, V_{CE} = 5.0 \text{ V}) $ $ (I_C = 1.0 \text{ A}, V_{CE} = 5.0 \text{ V}) $	h _{FE}	300 300 200	- 500 -	900 -	
Collector – Emitter Saturation Voltage (Note 4) (I_C = 1.0 A, I_B = 100 mA) (I_C = 0.5 A, I_B = 50 mA) (I_C = 0.1 A, I_B = 1.0 mA)	V _{CE} (sat)	- - -	0.10 0.06 0.05	0.200 0.125 0.075	V
Base – Emitter Saturation Voltage (Note 4) (I _C = 1.0 A, I _B = 0.1 A)	V _{BE(sat)}	_	-	1.1	V
Base – Emitter Turn–on Voltage (Note 4) $(I_C = 1.0 \text{ A, } V_{CE} = 2.0 \text{ V})$	V _{BE(on)}	_	-	1.1	V
Cutoff Frequency (I _C = 100 mA, V _{CE} = 5.0 V, f = 100 MHz	f _T	200	300	-	MHz
Output Capacitance (f = 1.0 MHz)	C _{obo}	_	-	15	pF

^{4.} Pulsed Condition: Pulse Width \leq 300 μ sec, Duty Cycle \leq 2%.

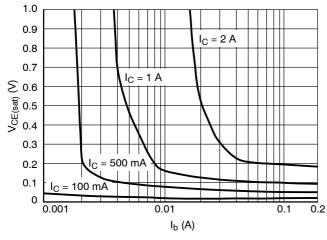


Figure 1. $V_{CE (sat)}$ versus I_b

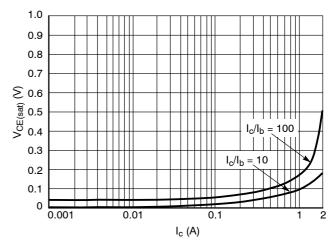


Figure 2. $V_{CE (sat)}$ versus I_c

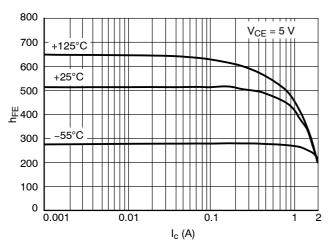


Figure 3. h_{FE} versus I_c

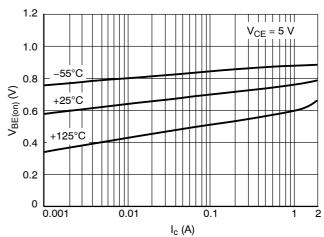


Figure 4. $V_{BE(on)}$ versus I_c

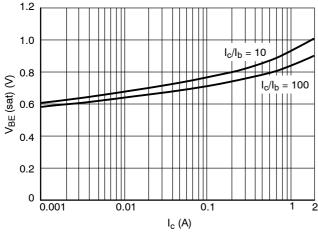


Figure 5. $V_{BE(sat)}$ versus I_c

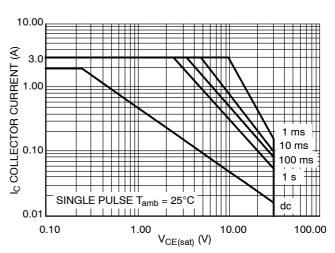


Figure 6. Safe Operating Area

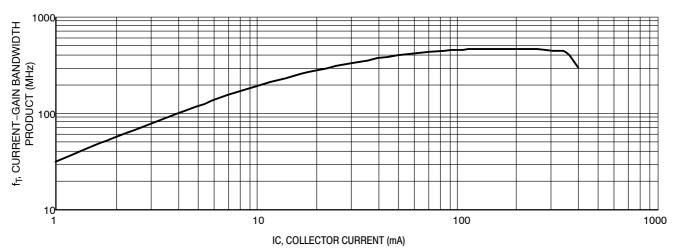


Figure 7. f_T (MHZ) versus I_C (mA) V_{CE} = 5.0 V

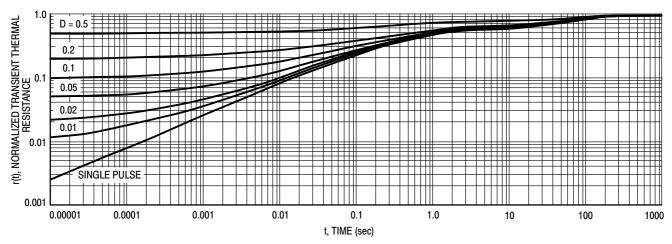


Figure 8. Normalized Thermal Response



TSOP-6 CASE 318G-02 **ISSUE V**

DATE 12 JUN 2012

STYLE 6: PIN 1. COLLECTOR 2. COLLECTOR

3. BASE 4. EMITTER

2. GROUND

3. I/O 4. I/O 5. VCC 6. I/O

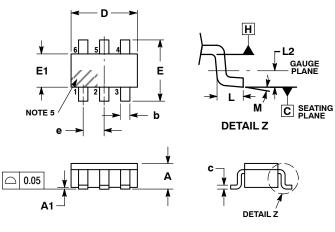
STYLE 12:

5. COLLECTOR 6. COLLECTOR

NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETERS.
 MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM
- LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
 DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH,
 PROTRUSIONS, OR GATE BURRS, MOLD FLASH, PROTRUSIONS, OR
 GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
 5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS						
DIM	MIN NOM MAX						
Α	0.90	1.00	1.10				
A1	0.01	0.06	0.10				
b	0.25	0.38	0.50				
С	0.10	0.18	0.26				
D	2.90	3.00	3.10				
E	2.50	2.75	3.00				
E1	1.30	1.50	1.70				
е	0.85	0.95	1.05				
L	0.20	0.40	0.60				
L2	0.25 BSC						
М	0° – 10°						



STYLE 1: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	STYLE 2: PIN 1. EMITTER 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. BASE 2 6. COLLECTOR 2	STYLE 3: PIN 1. ENABLE 2. N/C 3. R BOOST 4. Vz 5. V in 6. V out	STYLE 4: PIN 1. N/C 2. V in 3. NOT USED 4. GROUND 5. ENABLE 6. LOAD	STYLE 5: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2
STYLE 7: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. N/C 5. COLLECTOR 6. EMITTER	STYLE 8: PIN 1. Vbus 2. D(in) 3. D(in)+ 4. D(out)+ 5. D(out) 6. GND	STYLE 9: PIN 1. LOW VOLTAGE GATE 2. DRAIN 3. SOURCE 4. DRAIN 5. DRAIN 6. HIGH VOLTAGE GATE	2. GND ' 3. D(OUT)- 4. D(IN)- 5. VBUS	SOURCE 2
STYLE 13: PIN 1. GATE 1	STYLE 14: PIN 1. ANODE		LE 16: I 1. ANODE/CATHODE	STYLE 17: PIN 1. EMITTER

2. SOURCE 3. GATE

DRAIN

CATHODE

5. N/C

RECOMMEN SOLDERING FO	
DRAIN 1 6. CATHODE/DF	

3 GATE

5.

SOURCE

CATHODE/DRAIN

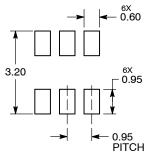
CATHODE/DRAIN

2. SOURCE 2

DRAIN 2

5. SOURCE 1

3 GATE 2



DIMENSIONS: MILLIMETERS

BASE 2. BASE FMITTER 3 ANODE/CATHODE COLLECTOR ANODE CATHODE ANODE

COLLECTOR

GENERIC MARKING DIAGRAM*

M





XXX = Specific Device Code = Date Code

= Pb-Free Package

XXX = Specific Device Code

Α =Assembly Location Υ = Year

W = Work Week

2.

3

5.

= Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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