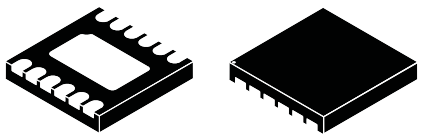
# STOD1317B

## 170 mA 13 V, high efficiency boost converter + LDO

**Datasheet - production data**



**DFN12L (3 x 3 mm)**

## Features

- Operating input voltage range from 2.6 V to 4.8 V
- ±1% output voltage tolerance
- Low output ripple
- True-shutdown
- Short-circuit protection
- Digital low power function
- Very high efficiency at light load thanks to pulse skipping operation
- Very fast line and load transients
- 1.2 MHz switching frequency
- 1 µA max. quiescent current
- DFN12L (3 x 3 x 0.8 mm)

## Applications

- Single rail AMOLED display
- Cellular phones
- Battery powered equipment

## Description

The STOD1317B is a fixed frequency, high efficiency, boost DC-DC converter with cascaded LDO able to provide output voltages ranging from 6 V to 13 V starting with an input voltage from 2.6 V to 4.8 V. The device is designed to supply loads that are very sensitive to output ripple such as AMOLED display panels. A dedicated LDO is able to suppress any ripple and noise coming out from the DC-DC converter. The LDO works with a constant drop in order to maintain high efficiency in the whole operating range. The low $R_{DSon}$ N-channel and P-channel MOSFET switches are integrated and contribute to achieving high efficiency. The true-shutdown feature allows physical disconnection of the battery from the load when the device is in shutdown mode. The control technique is able to maintain efficiency higher than 85% at light loads and higher than 80% at full load. The device includes soft-start control, inrush current limiter, thermal shutdown and inductor peak current limit. The STOD1317B is packaged in DFN12L (3 x 3 x 0.8 mm) height.

**Table 1. Device summary**

| Order code | Marking | Package | Packaging |
|---|---|---|---|
| STOD1317BTPUR | 1317B | DFN12L (3 x 3 mm) | 3000 parts per reel |

# Contents

# 1 Schematic

**Figure 1. Application schematic**

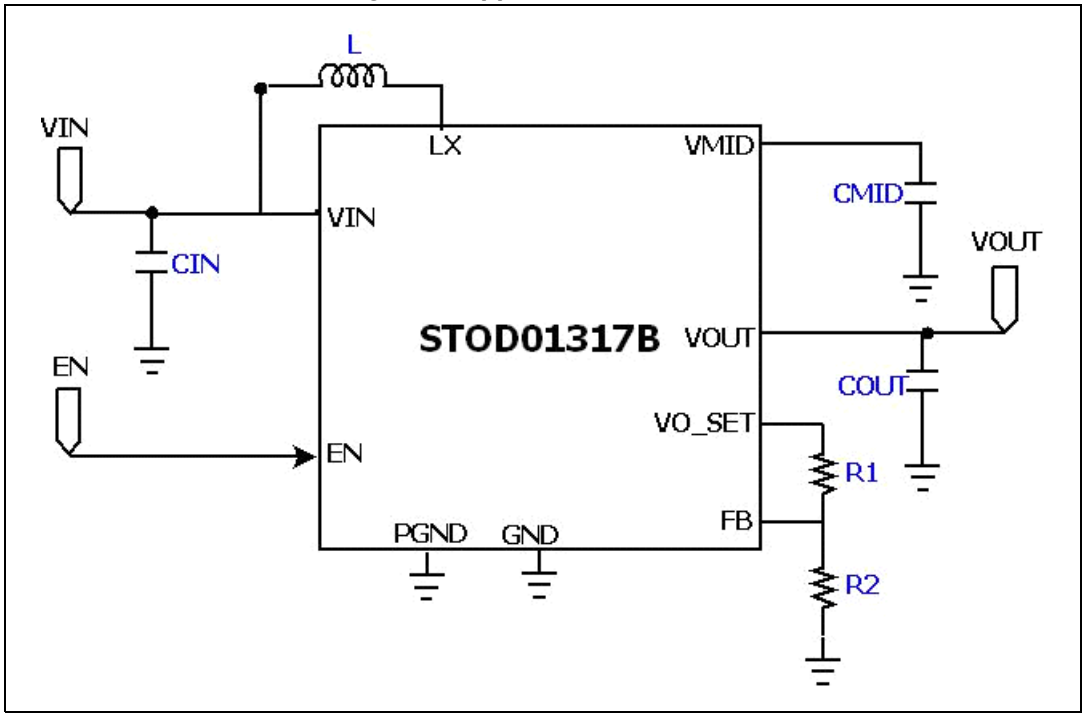


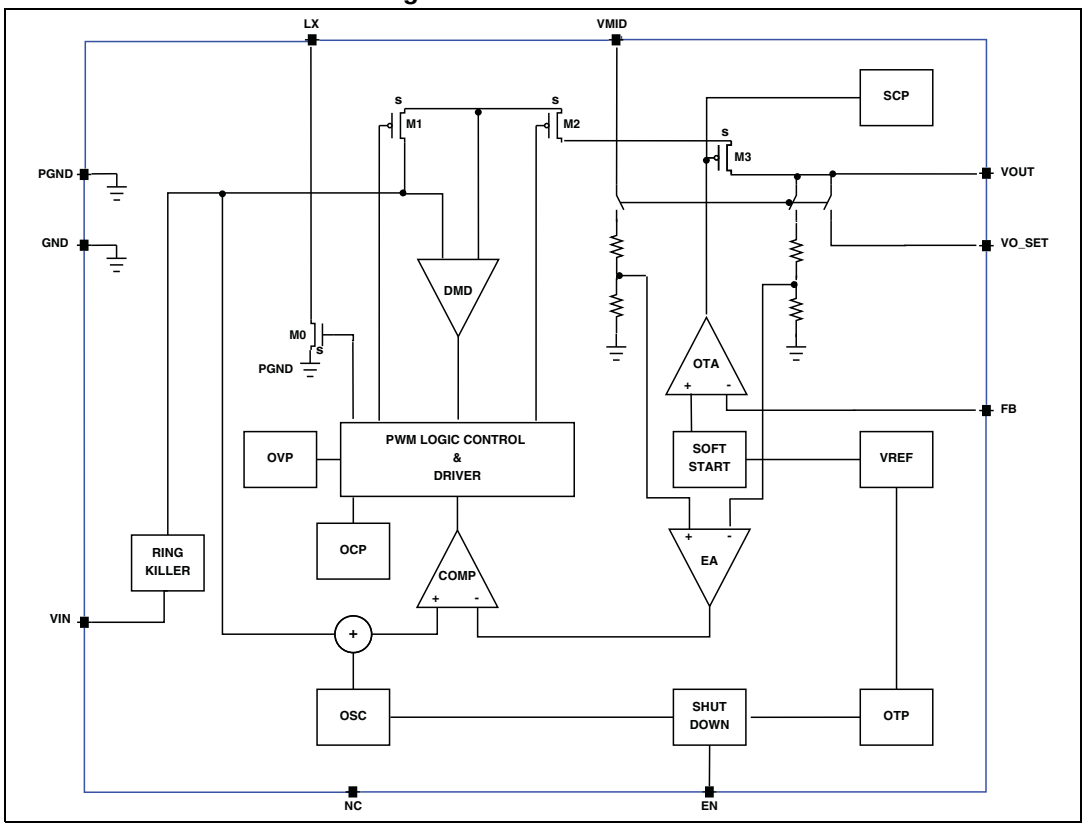

**Table 2. Typical external components**

| Comp. | Manufacturer | Part number | Value | Ratings | Size |
|---|---|---|---|---|---|
| $C_{IN}$ | MURATA<br>Taiyo Yuden<br>TDK | GRM219R61A106KE44<br>LMK212BJ106KD-T<br>C1608X5R0J106 | 10µF | ±10%, X5R, 10V<br>±10%, X5R, 10V<br>±10%, X5R, 6.3V | 0805<br>0805<br>0603 |
| $C_{MID}$ | MURATA<br>TDK | GRM219R61C475KE15<br>C2012X5R1C475 | 4.7µF | ±10%, X5R, 16V<br>±10%, X5R, 16V | 0805<br>0805 |
| $C_{OUT}$ | MURATA<br>TDK | GRM219R61C475KE15<br>C2012X5R1C475 | 4.7µF | ±10%, X5R, 16V<br>±10%, X5R, 16V | 0805<br>0805 |
| L (1) | CoilCraft<br>TDK<br>DASTEK | LPS4012-472ML<br>VLS252012T-4R7MR81<br>PNL3008-4R7M | 4.7µH | ±20%, curr. 1.7A, resist. 0.175Ω<br>±20%, curr. 1.3A, resist. 0.338Ω<br>±20%, curr. 0.9A, resist. 0.280Ω | 4.0 x 4.0 x 1.2<br>2.5 x 2.0 x 1.2<br>3.1 x 3.1 x 0.8 |
| R1 | | | kΩ | | 0402 |
| R2 | | | kΩ | | 0402 |

1. Inductor used for the typical application conditions. Inductance values ranging from 3.3 µH to 6.8 µH can be used together with the STOD1317B. A minimum saturation current of 1.2 A must be ensured to support 170 mA at 2.6 V in full range.

*Note: All the above components refer to a typical application. Operation of the device is not limited to the choice of these external components.*

**Figure 2. Block schematic**



# 2 Pin configuration

**Figure 3. Pin configuration (top view)**

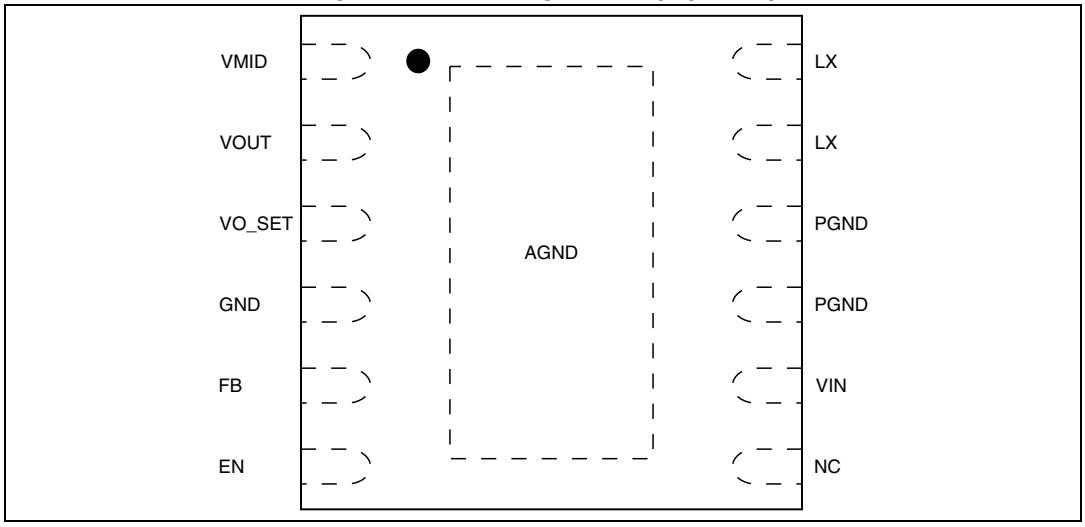



**Table 3. Pin description**

| Pin name | Pin number | Description |
|---|---|---|
| VMID | 1 | Step-up output voltage |
| VOUT | 2 | LDO output voltage |
| VO_SET | 3 | LDO output voltage set |
| GND | 4 | Analog ground |
| FB | 5 | Feedback voltage |
| EN | 6 | Enable pin. Connect this pin to GND or a voltage lower than 0.4V to shut down the IC. A voltage higher than 1.2V is required to enable the IC |
| NC | 7 | Not connected |
| VIN | 8 | Supply voltage |
| PGND | 9, 10 | Power ground |
| LX | 11, 12 | Switch pin. Inductor connection to the internal switches |
| Exposed PAD | | Internally connected to PGND |

# 3 Maximum ratings

**Table 4. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{IN}$ | Supply voltage | -0.3 to +7.0 | V |
| LX | Switching node | -0.3 to +16 | V |
| $V_{OUT\_SET}$ | LDO output voltage set | 16 | V |
| $V_{OUT}$ | Output voltage | -0.3 to +16 | V |
| EN | Logic pin | -0.3 to 4.6 | V |
| FB | Feedback pin | -0.3 to +2.5 | V |
| ESD | Machine model | ±200 | V |
| | Human body model | ±2000 | V |
| $T_{AMB}$ | Operating ambient temperature | -40 to 85 | °C |
| $T_J$ | Maximum operating junction temperature | +150 | °C |
| $T_{STG}$ | Storage temperature | -65 to 150 | °C |

*Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.*

**Table 5. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thJA}$ | Thermal resistance junction-ambient | 49.1 | °C/W |
| $R_{thJC}$ | Thermal resistance junction-case (FR-4 PCB) | 4.216 | °C/W |

# 4 Electrical characteristics

$T_J$ = 25 °C, $V_{IN}$ = 3.7 V, $V_{OUT}$ = 10 V, $C_{IN}$ = 2 x 10 µF, $C_{MID}$ = 2 x 4.7 µF, $C_{OUT}$ = 2 x 4.7 µF, L = 4.7 µH, $V_{EN}$ = 2 V, unless otherwise specified.

**Table 6. Electrical characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **General section** | | | | | | |
| $V_{IN}$ | Operating power input voltage range | | 2.6 | 3.7 | 4.8 | V |
| Iq | Shutdown mode | Shutdown mode, $V_{EN}$=GND | | 0.5 | 1 | µA |
| | No switching | $V_{EN}$=$V_{IN}$=3.7V, $V_{FB}$=1.3V | | 1 | 1.5 | mA |
| $V_{UVLO}$ | Undervoltage lockout threshold | $V_{IN}$ rising | | 2.4 | 2.5 | V |
| | | $V_{IN}$ falling | 2.1 | 2.2 | | |
| $f_{SW}$ | Switching frequency | | 1 | 1.2 | 1.35 | MHz |
| $I_{PK}$ | Switch current limitation | | 1.6 | 2 | 2.4 | A |
| **Output voltage ($V_{OUT}$)** | | | | | | |
| $V_{FB}$ | Feedback voltage | $T_A$=25°C | 1.08 | 1.2 | 1.32 | V |
| $\Delta V_{FB}$ | Accuracy | -40°C<$T_A$<85°C | 1.02 | | 1.38 | V |
| $V_{OUT}$ | Output voltage range | | 6 | 10 | 13 | V |
| $\Delta V_{LINE/LOAD}$ | Total line/load static variation (1) | $T_A$=25°C; $V_{IN}$=2.6V to 4.8V; $I_{OUT}$=5mA to 170mA | | 30 | 40 | mV |
| $V_{OUT\ RIPPLE}$ | Output voltage ripple | $V_{IN}$=3.7V, $V_{OUT}$=10V, $I_{OUT}$=10mA | | | 30 | mV |
| $V_{OVP}$ | Overvoltage protection | $V_{FB}$=0 | 14 | 15 | 16 | V |
| $I_{LKFB}$ | FB pin leakage current | $V_{FB}$=5V to 13V | | | 1 | µA |
| VMID | Step-up output voltage regulation | | $V_{OUT}$ + 0.38 | $V_{OUT}$ + 0.56 | $V_{OUT}$ + 0.7 | V |
| **Logic inputs** | | | | | | |
| $V_{IL}$ | EN low-level input voltage | | | | 0.4 | V |
| $V_{IH}$ | EN high-level input voltage | | 1.2 | | | V |
| $I_{LK-I}$ | EN input leakage current | $V_{EN}$=$V_{IN}$=4.8V | | | 1 | µA |
| **Power switches** | | | | | | |
| $R_{DSON}$ | P-Channel ON resistance | $I_{SW\_P}$=100mA | | 550 | 900 | mΩ |
| | N-Channel ON resistance | $I_{SW\_N}$=100mA | | 250 | 400 | |
| $I_{LKG-LX}$ | LX leakage current | $V_{IN}$=$V_{LX}$=4.8V; $V_{EN}$=0 | | | 1 | µA |

**Table 6. Electrical characteristics (continued)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **DLP function** | | | | | | |
| $I_{O\_LEAK}$ | Leakage current from load | $V_{IN}$=3.7V, $V_{EN}$=0, $V_{OUT}$=6V (supplied by external power) | | 0.5 | 2 | µA |

1. Not tested in production. This value is guaranteed by correlation with $R_{DSON}$, peak current limit and operating input voltage.
2. Not tested in production.

# 5 Typical performance characteristics

$T_J$ = 25 °C, $V_{IN}$ = 3.7 V, $V_{OUT}$ = 10 V, $C_{IN}$ = 2 x 10 µF, $C_{MID}$ = 2 x 4.7 µF, $C_{OUT}$ = 2 x4.7 µF, L = 4.7 µH, $V_{EN}$ = 2 V, unless otherwise specified.

**Figure 4. Quiescent current vs. temperature**

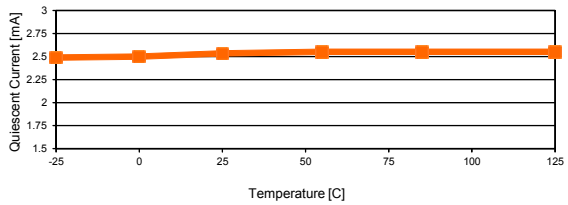



**Figure 5. Switching frequency vs. temperature**

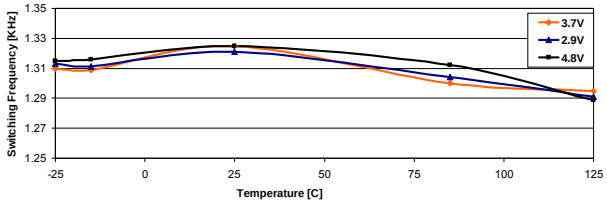



**Figure 6. Efficiency vs. output current**

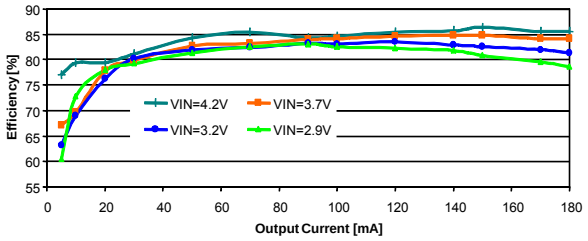
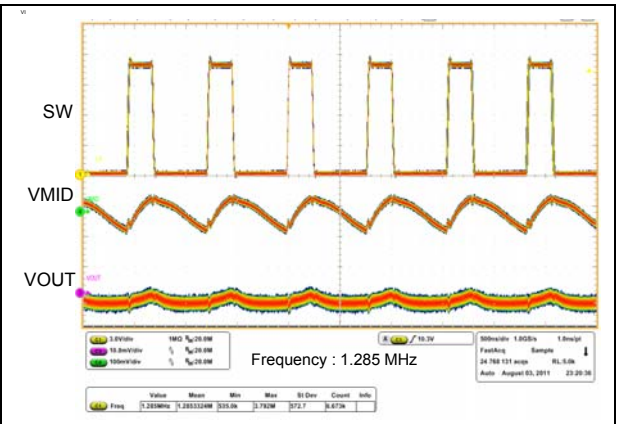
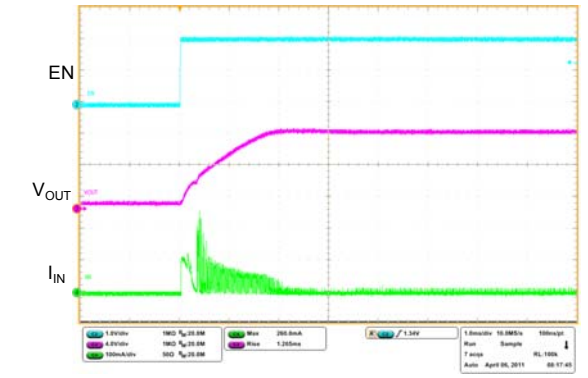



**Figure 7. Switching frequency**




$V_{IN}$ = 3.7 V, $I_{OUT}$ = 170 mA, $T_J$ = 25 °C

**Figure 8. Soft-start inrush current**




$V_{IN}$ = 3.7 V, NO LOAD, $T_J$ = 25°C, SS:1.265 ms, Inrush current: 260 mA

**Figure 9. Feedback voltage vs. temperature**

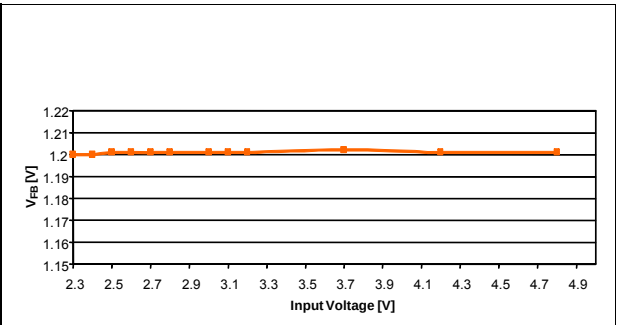
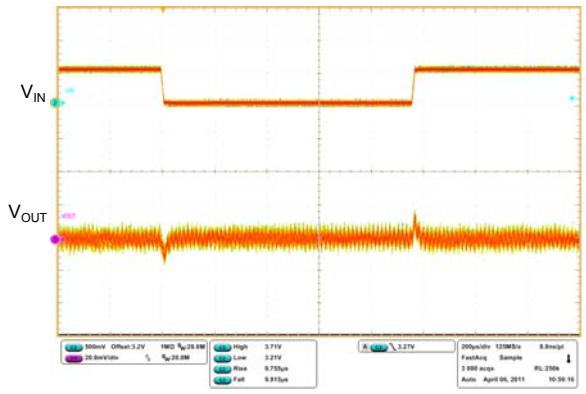


**Figure 10. TDMA noise immunity**




$V_{IN}$ = 2.6 V to 3.1 V, $I_{OUT}$ = 20 mA

# 6 Detailed description

The STOD1317B is a high efficiency DC-DC converter which integrates a step-up and LDO power stage suitable for supplying AMOLED panels. Thanks to the high level of integration it needs only 6 external components to operate and it achieves very high efficiency using a synchronous rectification technique.

The controller uses an average current mode technique in order to obtain good stability and precise voltage regulation in all possible conditions of input voltage, output voltage and output current. In addition, the peak inductor current is monitored in order to avoid saturation of the coils.

The STOD1317B implements a power saving technique in order to maintain high efficiency at very light load and it switches to PWM operation as the load increases in order to guarantee the best dynamic performances and low noise operation.

In order to guarantee very low ripple on the output voltage, the step-up output is filtered by the LDO. There are two control loops; the LDO control loop regulates $V_{OUT}$ in order to provide the right voltage to the output, while the boost control loop is internally set to provide and output voltage 380 mV higher than $V_{OUT}$ in order to maintain the LDO in regulation at the minimum possible drop.

The STOD1317B avoids battery leakage thanks to the true-shutdown feature and it is self protected from overtemperature and short-circuit on the $V_{OUT}$ pin. Undervoltage lockout and soft-start guarantee proper operation during startup.

## 6.1 BOOST multiple mode of operation

The boost DC-DC operates in three different modes: pulse skipping (PS), discontinuous conduction mode (DCM) and continuous conduction mode (CCM). It switches automatically between the three modes according to input voltage, output current and output voltage conditions.

### 6.1.1 Pulse skipping operation

The STOD1317B works in pulse skipping mode when the load current is below some tens of mA. The load current level at which this way of operation occurs depends on the input and output voltage.

### 6.1.2 Discontinuous conduction mode

When the load increases above some tens of mA, the STOD1317B enters DCM operation.

In order to obtain this type of operation the controller must avoid the inductor current going negative. The discontinuous mode detector (DMD) block senses the voltage across the synchronous rectifier and turns off the switch when the voltage crosses a defined threshold which, in turn, represents a certain current in the inductor. This current can vary according to the slope of the inductor current which depends on input voltage, inductance value, and output voltage.

### 6.1.3 Continuous conduction mode

At medium/high output loads the STOD1317B enters full CCM at constant switching frequency mode.

## 6.2 Enable pin

The device operates when the EN pin is set high. If the EN pin is set low, the device stops switching, all the internal blocks are turned off. In this condition the current drawn from $V_{IN}$ is below 1 µA in the whole temperature range. In addition, the internal switches are in OFF state so the load is electrically disconnected from the input, this avoids unwanted current leakage from the input to the load.

## 6.3 Soft-start and inrush current limiting

After the EN pin is pulled high, or after a suitable voltage is applied to $V_{IN}$ and EN, the device initiates the startup phase.

As a first step, the $C_{MID}$ capacitor is charged, the P1 switch implements a current limiting technique in order to keep the charge current below 400 mA. This avoids battery overloading during startup.

After $V_{MID}$ reaches the $V_{IN}$ voltage level, the P1 switch is fully turned on and the soft-start procedure for the step-up is started. $V_{OUT}$ starts to softly increase until it reaches the regulation value.

## 6.4 Undervoltage lockout

The undervoltage lockout function avoids improper operation of the STOD1317B when the input voltage is not high enough. When the input voltage is below the UVLO threshold the device is in shutdown mode. The hysteresis of 100 mV avoids unstable operation when the input voltage is close to the UVLO threshold.

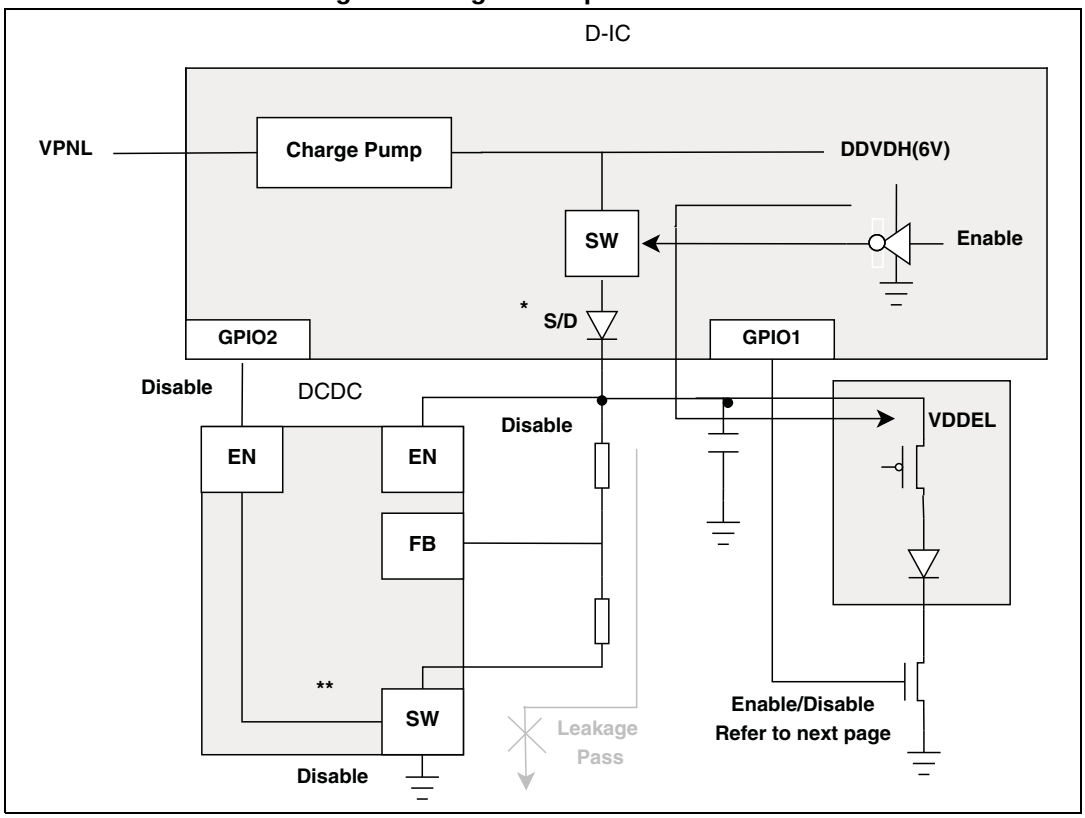
## 6.5 Overtemperature protection

An internal temperature sensor continuously monitors the IC junction temperature. If the IC temperature exceeds 150 °C, typical, the device stops operating. As soon as the temperature falls below 135 °C, typical, normal operation is restored.

## 6.6 Digital low power function

The digital low power (DLP) function allows physical disconnection of the load from the device.

**Figure 11. Digital low power function**




Operation

- (*) When the power IC is disabled, in order to disconnect leakage current through the feedback node, the S/W function is active.
- (**) A new EN transition from low to high and/or device power-up turn off the DLP function and allow IC to work under typical conditions.

# 7 Application information

## 7.1 External passive components

### 7.1.1 Inductor selection

The inductor is the key passive component for switching converters.

For the step-up converter an inductance between 3.3 µH and 6.8 µH is recommended.

It is very important to select the right inductor according to the maximum current the inductor can handle in order to avoid saturation. The peak current for the step-up can be calculated as:

**Equation 1**

$$I_{PEAK\ \ BOOST} = \frac{V_{MID} \times I_{OUT}}{\eta \times VIN_{MIN}} + \frac{VIN_{MIN} \times (V_{MID} - VIN_{MIN})}{2 \times V_{MID} \times fs \times L}$$

where

$V_{MID}$: step-up output voltage, it is fixed internally to $V_{OUT}$ + 0.38 V;

$I_{OUT}$: output current;

$V_{IN}$: input voltage of the STOD1317B;

fs: switching frequency. Use the minimum value of 1 MHz for worst case;

$\eta$: efficiency of the step-up converter (0.80 at maximum load).

### 7.1.2 Input and output capacitor selection

It is recommended to use ceramic capacitors with low ESR as input and output capacitors in order to filter any disturbance present in the input line and to obtain stable operation of the step-up converter and LDO. A minimum real capacitance value of 3 µF must be guaranteed for $C_{MID}$ and $C_{OUT}$ in all conditions.

## 7.2 Recommended PCB layout

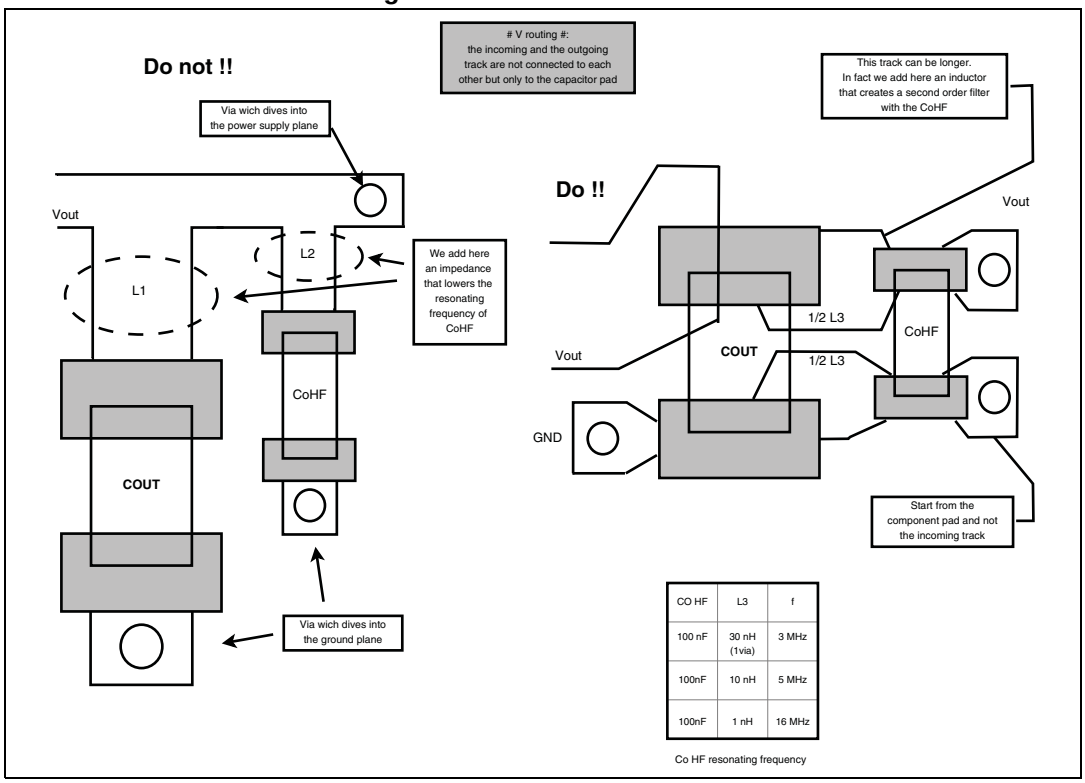
The STOD1317B is a high frequency power switching device so it requires a proper PCB layout in order to obtain the necessary stability and optimize line/load regulation and output voltage ripple.

The input capacitor must be as close as possible to the $V_{IN}$ pin.

In order to minimize the ground noise, a common ground node for power ground (PGND) and a different one for analog ground (GND) must be used. The exposed pad is connected to PGND through vias.
Grounding is fundamental to the operation of DC-DC converters; run separate ground paths for critical parts of the circuit (GND and Power GND), each connected back to a single ground point.

Separate ground lines prevent the current and noise of one component from interfering with other components. If using a ground plane, utilize “split” plane techniques to give effective grounding. Use multiple vias to decrease the trace impedance to ground.

**Figure 12. Ground schematic**




Such isolation is necessary to prevent high-level switching currents from returning to the battery, or other power supply, through the same ground-return path as the analog signals.

If that happens, the ground path of those sensitive signals is disturbed; the high-level switching currents flowing through the ground's resistance and inductance cause the voltage along the return path to vary.

In addition to the grounding scheme, proper placement of the regulator's components is important.

Beginning a new layout, for the reasons above, it is necessary to firstly place the capacitors $C_{IN}$, $C_{OUT}$ and $C_{MID}$ as close as possible to the related device pins.

After that, it is possible to place the inductors and the Power GND routing. Next, we can trace the GND connected through vias to the PGND near to one of the main filter capacitors.

The LDO needs a quiet ground signal in order to operate properly.

It is important to pay close attention to the routing of traces from capacitor terminals in a DC-DC converter circuit.

Large-valued low-ESR capacitors are expensive, and bad routings can cancel their performance.

A good routing, on the other hand, can lower the output noise.

Ripple is directly related to the inductor value, the capacitor ESR, the switching frequency, and so forth, but HF noise (spikes) depends on parasitic elements and the switching action. In a bad routing, parasitic inductance associated with trace lengths causes problems:
In *Figure 12*, L1 brings about an increase in noise, and L2 limits the attenuation of an added HF capacitor. The solution is to bring the input trace in on one side of the capacitor pad, and the output trace out on the other side of the pad.

Figure 13. Top layer

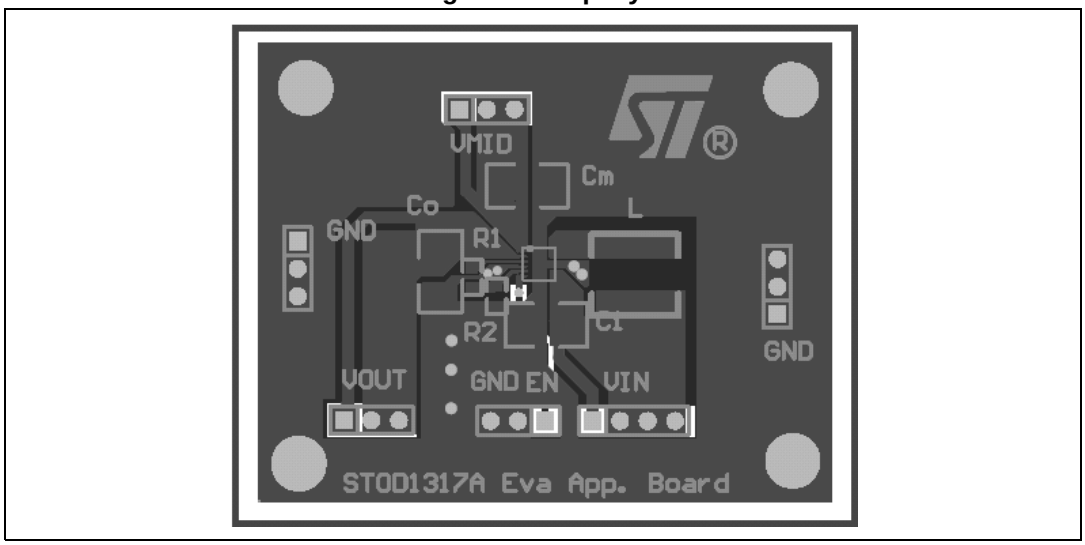
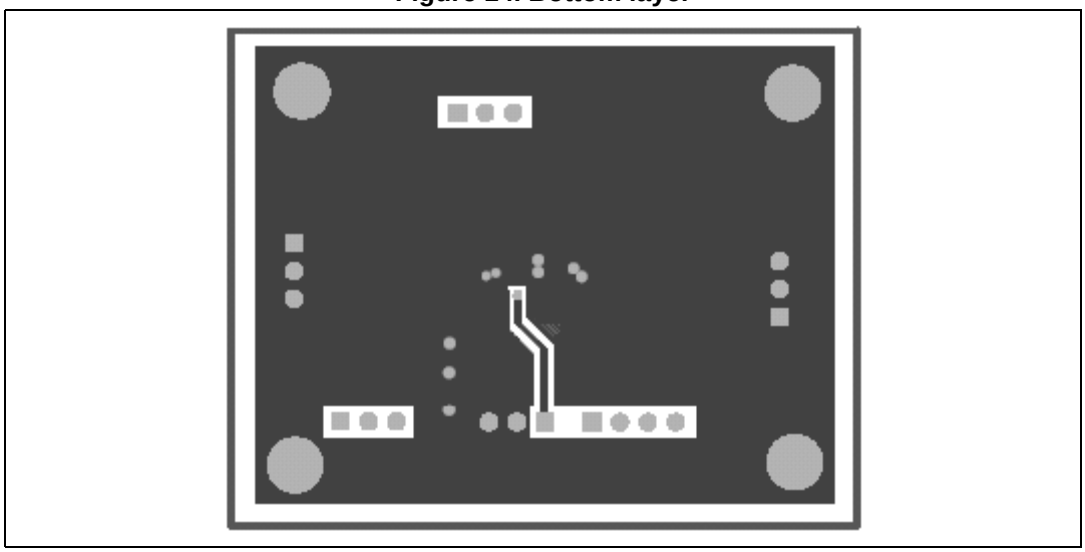



Figure 14. Bottom layer



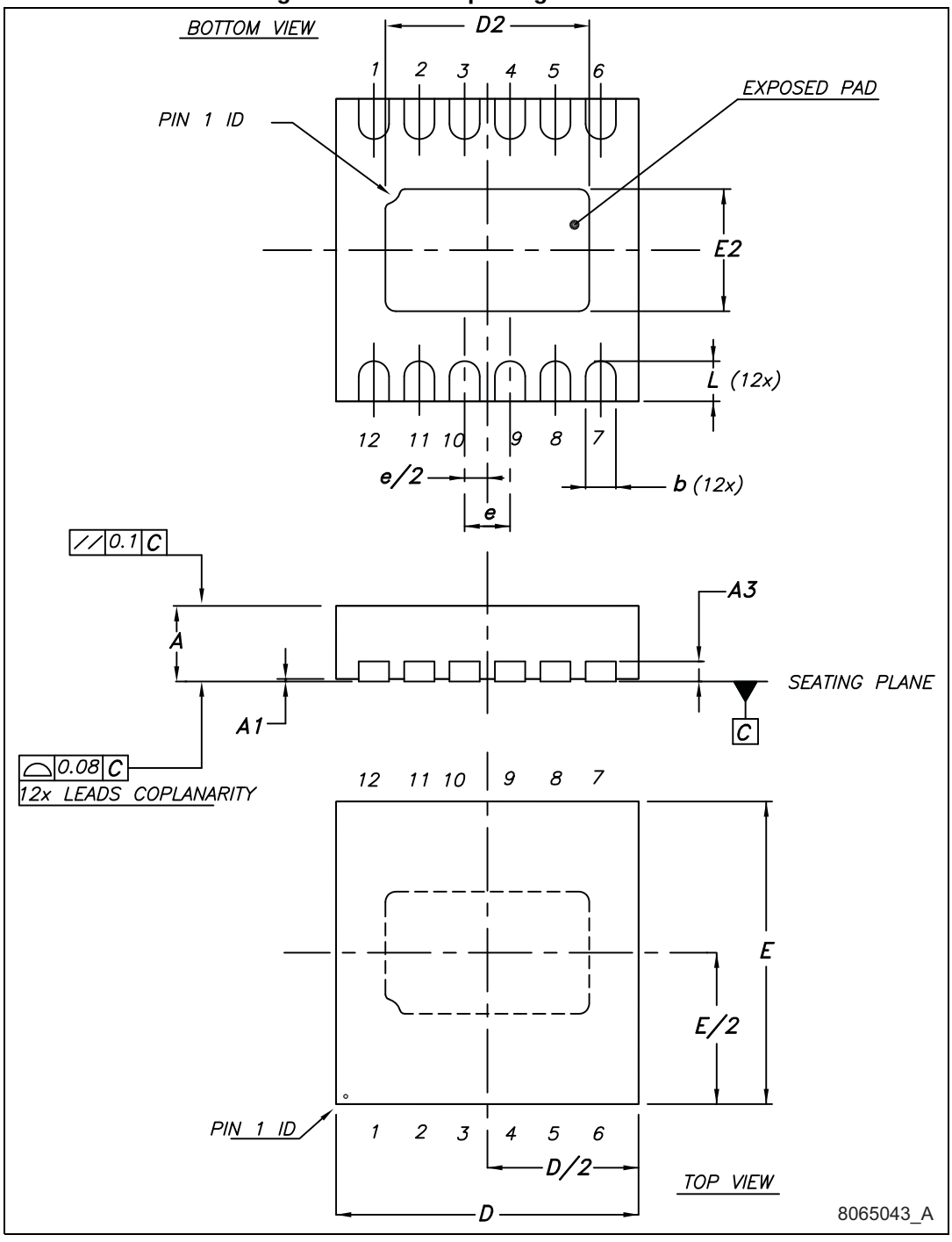
# 8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

**Table 7. DFN12L (3 x 3 x 0.8 mm.) package mechanical data**

| Dim. | mm. | | |
|---|---|---|---|
| | Min. | Typ. | Max |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| A3 | | 0.20 | |
| b | 0.18 | 0.25 | 0.30 |
| D | 2.85 | 3 | 3.15 |
| D2 | 1.87 | 2.02 | 2.12 |
| E | 2.85 | 3 | 3.15 |
| E2 | 1.06 | 1.21 | 1.31 |
| e | | 0.45 | |
| L | 0.30 | 0.40 | 0.50 |

**Figure 15. DFN12L package dimensions**



## Tape & reel QFNxx/DFNxx (3x3) mechanical data

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 330 | | | 12.992 |
| C | 12.8 | | 13.2 | 0.504 | | 0.519 |
| D | 20.2 | | | 0.795 | | |
| N | 99 | | 101 | 3.898 | | 3.976 |
| T | | | 14.4 | | | 0.567 |
| Ao | | 3.3 | | | 0.130 | |
| Bo | | 3.3 | | | 0.130 | |
| Ko | | 1.1 | | | 0.043 | |
| Po | | 4 | | | 0.157 | |
| P | | 8 | | | 0.315 | |

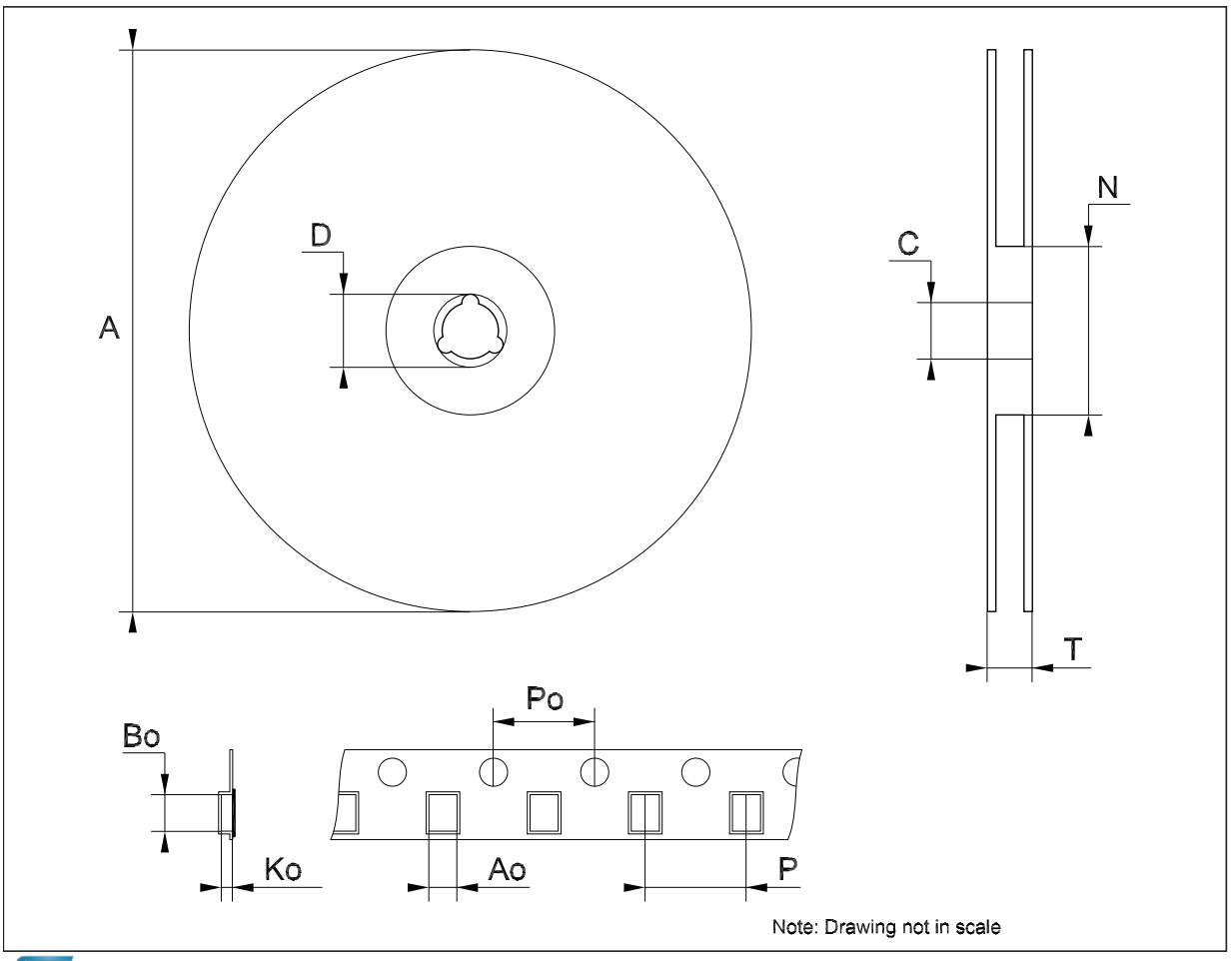
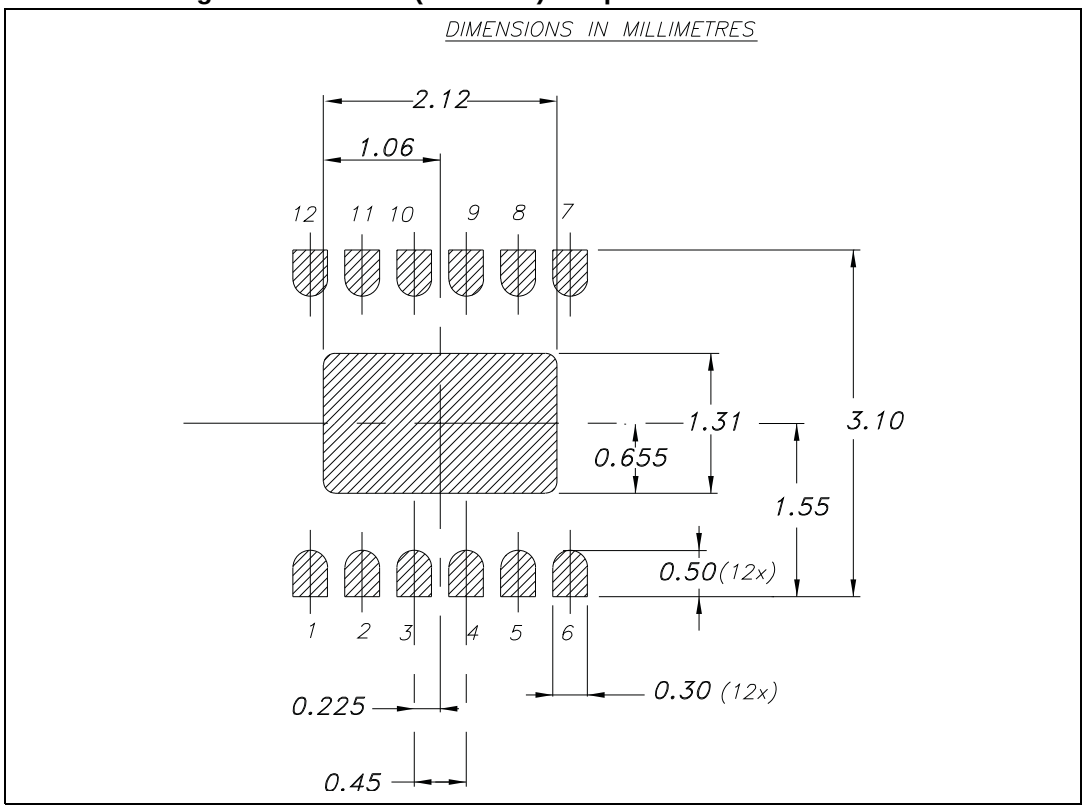


**Figure 16. DFN12L (3 x 3 mm) footprint recommended data**



# 9 Revision history

Table 8. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 19-Dec-2011 | 1 | Initial release. |
| 11-Apr-2013 | 2 | Updated:<br>– Package mechanical data *Table 7 on page 17* and *Figure 15 on page 18*. |

**Please Read Carefully:**

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