

Top Marking Change for 7 Series, UltraScale, and UltraScale+ Products

XCN16014 (v1.0) July 4, 2016

Product Change Notice

Overview

The purpose of this notification is to advise customers of the phased introduction of top marking changes for Xilinx® 7 series, Zynq®-7000, Zynq® UltraScale+™, UltraScale+™, and UltraScale+™ commercial / industrial "XC", Automotive "XA", and Defense-grade "XQ" devices. There is no change to fit, form, function, or reliability.

Description

Xilinx will be adding a 2D barcode to the topside marking for all Xilinx 7 series, Zynq-7000, Zynq UltraScale+, UltraScale, and UltraScale+ commercial / industrial "XC", Automotive "XA", and Defense-grade "XQ" devices. The addition of this 2D barcode allows for improved device-level traceability. The change will be introduced in phases as outlined in Table 1 (refer to XTP424 for transition updates).

To aid in device identification, speed, temperature grade and specification control document (SCD) information will continue to be provided in a human readable format on the moisture barrier bag labels, box labels, and invoice. An example of the device marking will also be included on the bag label as a visual guide to aid in inspection.

Through the enhanced device-level traceability provided to customers using the 2D barcode, Xilinx as a 2nd phase will be improving its delivery support and manufacturing scalability by removing selected topside marking information (line 4 speed, temperature grade and SCD information), as indicated in Table 2 and illustrated in Phase II of Figure 1 and Figure 2.

This enhanced device-level traceability also allows improved material selection based on individual device performance rather than date code and lot number. Xilinx will be combining devices in a shipment based on the device performance characteristics rather than controlling combinations by lot or date codes.

The 2D barcode contains a unique serial number that must be scanned using a camera based application to determine the serial number. The device's speed grade, temperature grade and SCD that were previously found on line 4 can only be retrieve using the unique serial number through an internet based application either on a mobile device or through a web browser using a portal (refer to XTP424 for details). Scanning the existing License Plate Number (LPN) provided on the inner box and bag label will allow access to all device information and codes contained within a specific bag or box using the same portal.

Products Affected

This change affects all package, speed, and temperature grade variations for Xilinx 7 series, Zynq-7000, Zynq UltraScale+, UltraScale, and UltraScale+ commercial / industrial "XC", Automotive "XA", and Defense-grade "XQ" devices, including SCD product.

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Table 1: Addition of 2D Barcode to Top Mark - Phase I (Figures 1 and 2)

Product Line	Device	Anticipated Shipments
XC	Zynq UltraScale+, and UltraScale+	Now – Shipping Engineering Samples (ES)
XC	7 series, Zynq-7000, and UltraScale November 2016	
XA	7 series, Zynq-7000, and Zynq UltraScale+ November 2016	
XQ	7 series, Zynq-7000, UltraScale, Zynq UltraScale+, and UltraScale+	November 2016

Table 2: Marking Simplification (line 4 speed, temperature grade, and SCD) - Phase II (Figures 1 and 2)

Product Line	Device	Anticipated Shipments
XC	Zynq UltraScale+*, and UltraScale+*	Upon Production Release
XC	7 series, Zynq-7000, and UltraScale	May 2017
XA	7 series, Zynq-7000, and Zynq UltraScale+*	July 2017

^{*}Note: UltraScale+ products will not be marked with lot number or date code.

Key Dates and Ordering Information

Xilinx will begin cross shipping devices with either mark as indicated in <u>Table 1</u> and <u>Table 2</u> above. For exact transition dates, please refer to Xilinx <u>XTP424</u>.

Traceability

Affected devices are identified by the following package top marks as shown in Figure 1 and Figure 2.

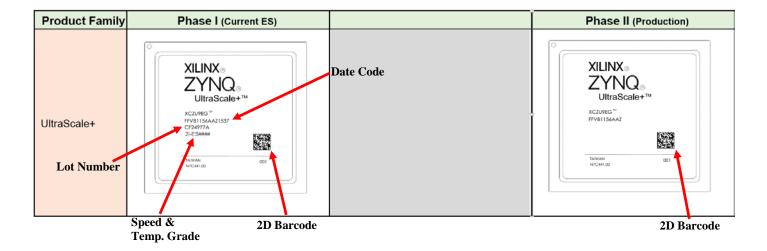


Figure 1: Product marking examples



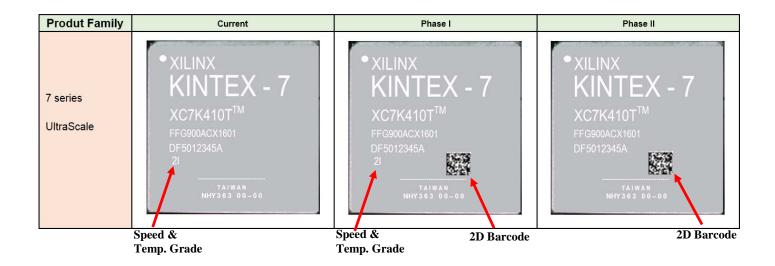


Figure 2: Product marking examples

Response

No response is required. For additional information or questions, please contact Xilinx Technical Support.

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Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
07/04/2016	1.0	Initial release.



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