AOZ1242

EZBuck™ 3A Simple Buck Regulator

General Description

The AOZ1242 is a high efficiency, simple to use, 3A buck regulator flexible enough to be optimized for a variety of applications. The AOZ1242 works from a 4.5V to 32V input voltage range, and provides up to 3A of continuous output current on each buck regulator output. The output voltage is adjustable down to 0.8V.

The AOZ1242 comes in an SO-8 or DFN-8 package and is rated over a -40°C to +85°C ambient temperature range

Features

- 4.5V to 32V operating input voltage range
- 70mΩ internal NFET, efficiency: up to 95%
- Internal soft start
- Output voltage adjustable down to 0.8V
- 3A continuous output current
- Fixed 370kHz PWM operation
- Cycle-by-cycle current limit
- Short-circuit protection
- Thermal shutdown
- Small size, SO-8 or DFN-8 package

Applications

- Point of load DC/DC conversion
- Set top boxes
- DVD drives and HDD
- LCD monitors & TVs
- Cable modems
- Telecom/networking/datacom equipment

Green Product

Typical Application

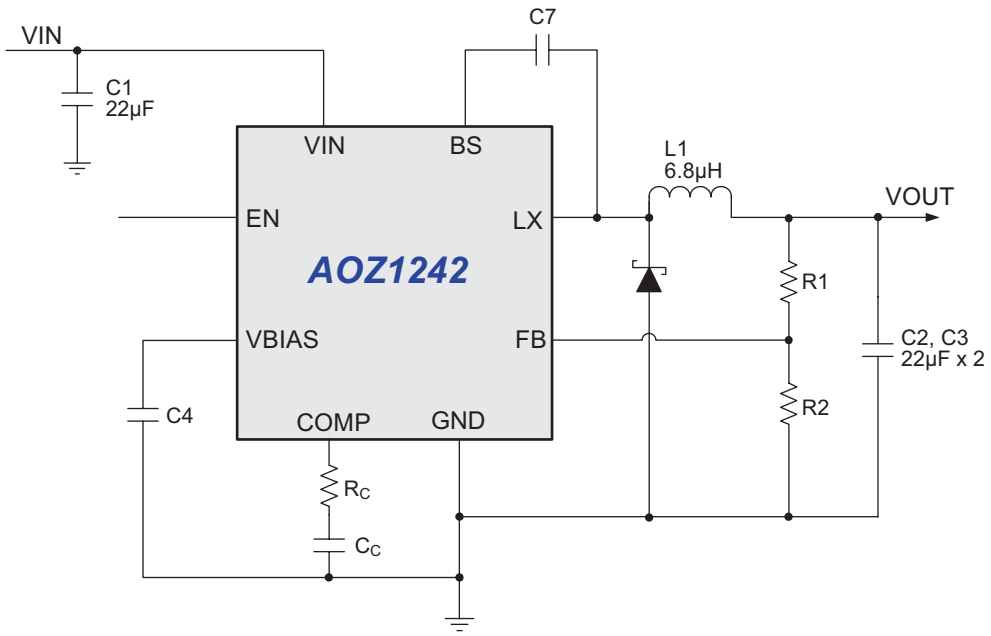


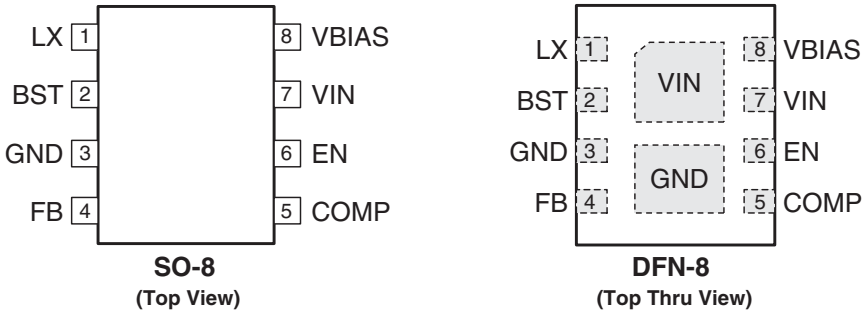
Figure 1. 3.3V/3A Buck Regulator

Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ1242AI	-40°C to +85°C	SO-8	Green Product
AOZ1242DI	-40°C to +85°C	DFN-8	Green Product

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/web/quality/rohs_compliant.jsp for additional information.

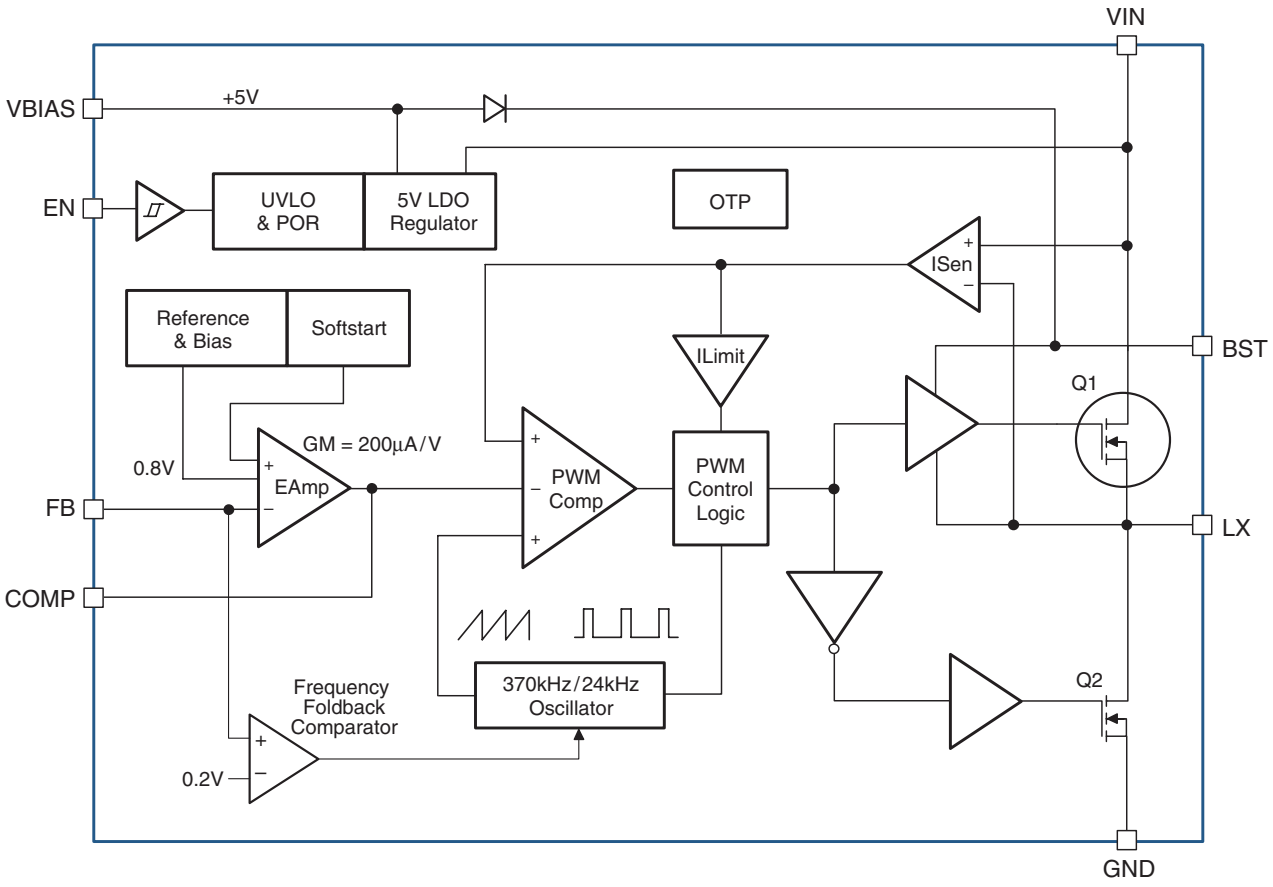
Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Function
1	LX	PWM output connection to inductor. LX pin needs to be connected externally. Thermal connection for output stage.
2	BST	Bootstrap voltage input. High side driver supply. Connected to 0.1µF capacitor between BST and LX.
3	GND	Ground.
4	FB	Feedback input. It is regulated to 0.8V. The FB pin is used to determine the PWM output voltage via a resistor divider between the output and GND.
5	COMP	External loop compensation. Output of internal error amplifier. Connect a series RC network to GND for control loop compensation.
6	EN	Enable pin. The enable pin is active HIGH. Connect EN pin to V_{IN} if not used. Do not leave the EN pin floating.
7	V_{IN}	Supply voltage input. Range from 4.5V to 32V. When V_{IN} rises above the UVLO threshold the device starts up. All V_{IN} pins need to be connected externally.
8	VBIAS	Compensation pin of internal linear regulator. Place a 1µF capacitor between this pin and ground.

Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

Parameter	Rating
Supply Voltage (V_{IN})	34V
LX to GND	-0.7V to V_{IN}+0.3V
EN to GND	-0.3V to V_{IN}+0.3V
FB to GND	-0.3V to 6V
COMP to GND	-0.3V to 6V
BST to GND	V_{LX}+6V
VBIAS to GND	-0.3V to 6V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating(1)	2kV

Note:

1. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Recommended Operating Conditions.

Parameter	Rating
Supply Voltage (V_{IN})	4.5V to 32V
Output Voltage Range	0.8V to V_{IN}
Ambient Temperature (T_A)	-40°C to +85°C
Package Thermal Resistance (Θ_{JA})(2) SO-8 DFN-8	 105°C/W 53°C/W

Note:

2. The value of Θ_{JA} is measured with the device mounted on 1-in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A = 25°C. The value in any given application depends on the user's specific board design.

Electrical Characteristics

T_A = 25°C, V_{IN} = V_{EN} = 12V, unless otherwise specified[3]

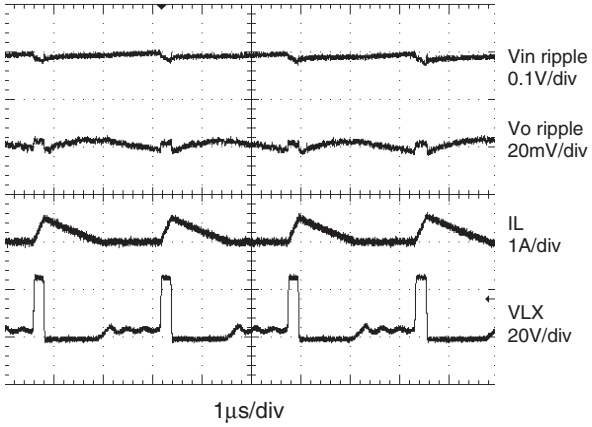
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IN}	Supply Voltage		**4.5**		**32**	V
V_{UVLO}	Input Under-Voltage Lockout Threshold	V_{IN} Rising V_{IN} Falling		4.3 4.1		V
I_{IN}	Supply Current (Quiescent)	I_{OUT} = 0, V_{FB} = 1.2V, V_{EN} > 2V		**2**	**3**	mA
I_{OFF}	Shutdown Supply Current	V_{EN} = 0V		**3**	**20**	µA
V_{FB}	Feedback Voltage		0.782	0.8	0.818	V
	Load Regulation			0.5		%
	Line Regulation			0.08		% / V
I_{FB}	Feedback Voltage Input Current				200	nA
ENABLE						
V_{EN}	EN Input Threshold	Off Threshold On Threshold	 2.5		0.6	V
V_{HYS}	EN Input Hysteresis			200		mV
MODULATOR						
f_O	Frequency		315	370	425	kHz
D_{MAX}	Maximum Duty Cycle		85			%
D_{MIN}	Minimum Duty Cycle				6	%
G_{VEA}	Error Amplifier Voltage Gain			500		V / V
G_{EA}	Error Amplifier Transconductance			200		µA / V
PROTECTION						
I_{LIM}	Current Limit		3.5		5.5	A
	Over-Temperature Shutdown Limit	T_J Rising T_J Falling		145 100		°C
f_{SC}	Short Circuit Hiccup Frequency	V_{FB} = 0V		24		kHz
t_{SS}	Soft Start Interval			4		ms
PWM OUTPUT STAGE						
$R_{DS(ON)}$	High-Side Switch On-Resistance			70	100	mΩ
	High-Side Switch Leakage	V_{EN} = 0V, V_{LX} = 0V			10	µA

Note:
3. Specification in **BOLD** indicate an ambient temperature range of -40°C to +85°C. These specifications are guaranteed by design.

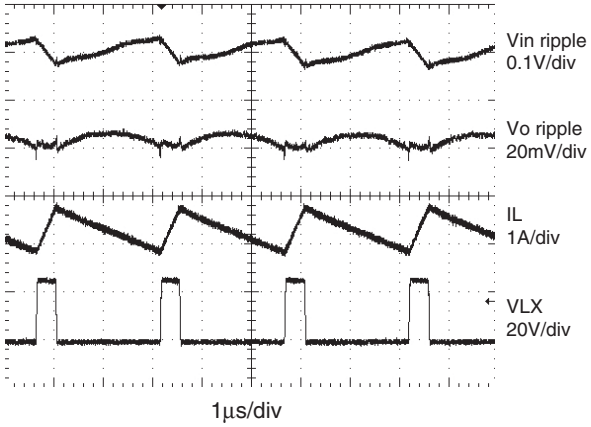
Typical Performance Characteristics

Circuit of Figure 1. T_A = 25°C, V_{IN} = V_{EN} = 24V, V_{OUT} = 3.3V unless otherwise specified.

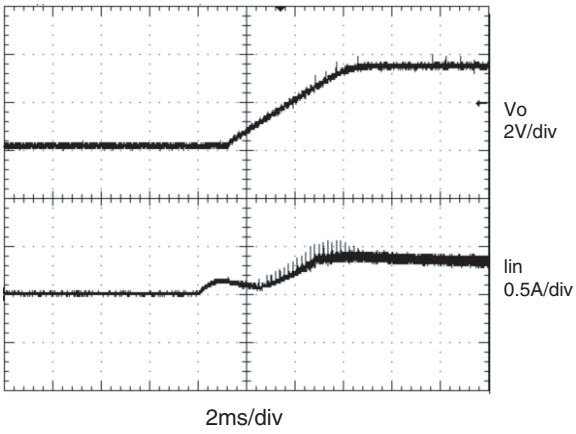
Light Load (DCM) Operation



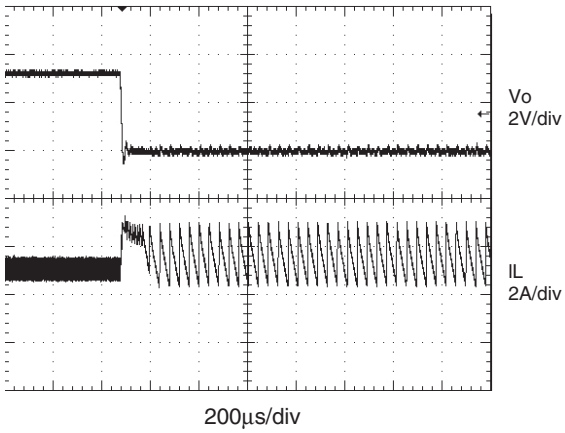
Full Load (CCM) Operation



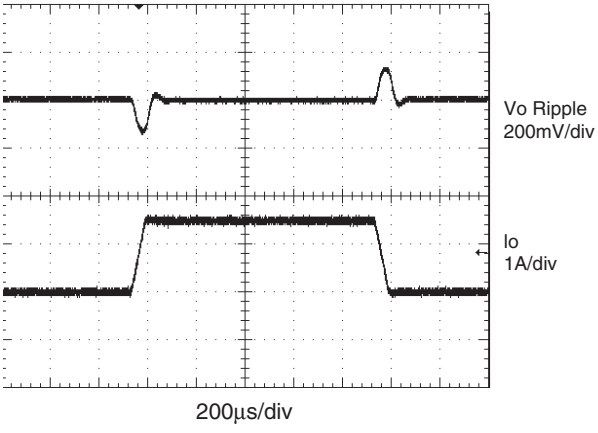
Startup to Full Load



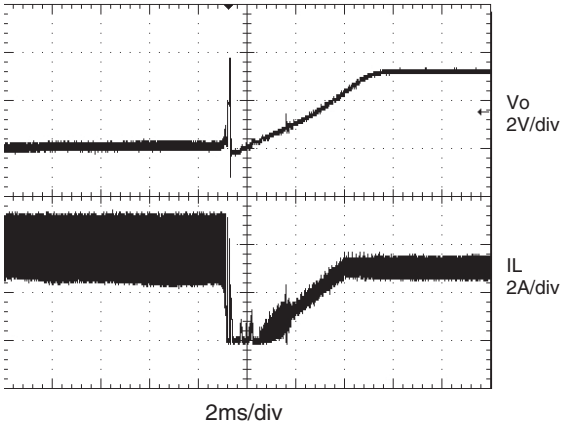
Short Circuit Protection



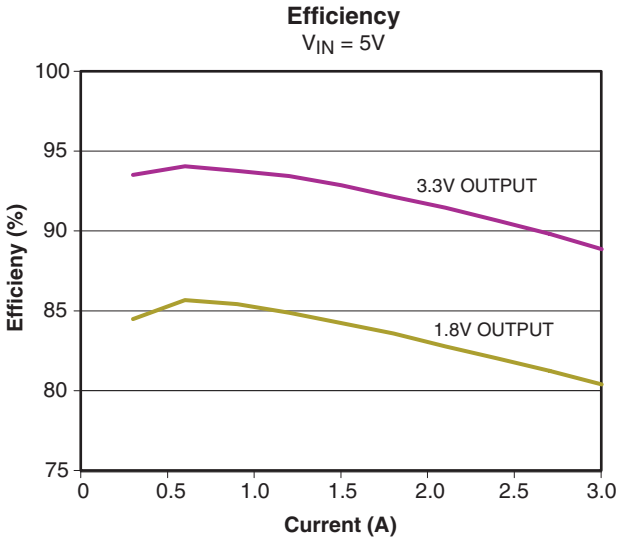
50% to 100% Load Transient

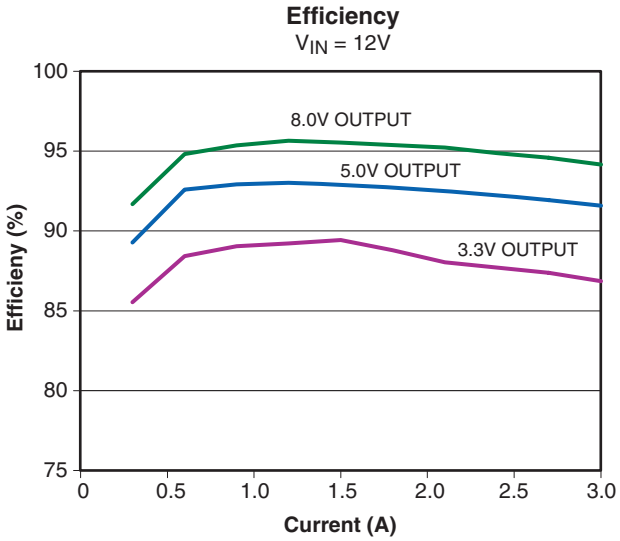


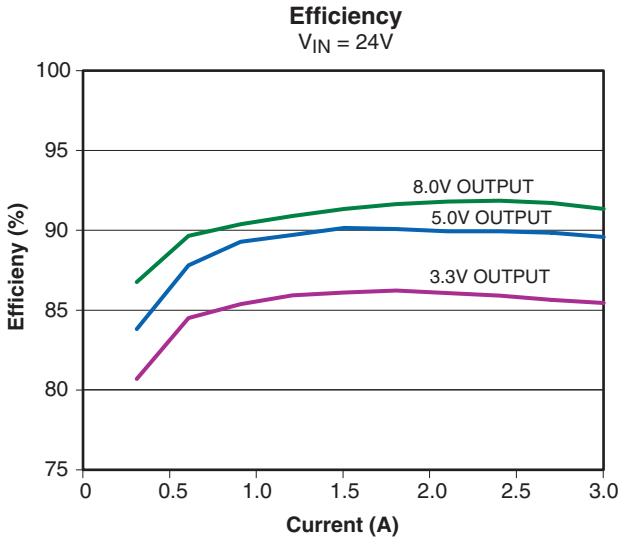
Short Circuit Recovery



Efficiency Curves







Detailed Description

The AOZ1242 is a current-mode step down regulator with integrated high side NMOS switch. It operates from a 4.5V to 32V input voltage range and supplies up to 3A of load current. The duty cycle can be adjusted from 6% to 85% allowing a wide range of output voltage. Features include enable control, Power-On Reset, input under voltage lockout, fixed internal soft-start and thermal shut down.

The AOZ1242 is available in SO-8 or DFN-8 package.

Enable and Soft Start

The AOZ1242 has internal soft start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulation voltage. A soft start process begins when the input voltage rises to 4.1V and voltage on EN pin is HIGH. In soft start process, the output voltage is ramped to regulation voltage in typically 6.8ms. The 6.8ms soft start time is set internally.

Connect the EN pin to V_{IN} if enable function is not used. Pull it to ground will disable the AOZ1242. Do not leave it open. The voltage on EN pin must be above 2.5 V to enable the AOZ1242. When voltage on EN pin falls below 0.6V, the AOZ1242 is disabled. If an application circuit requires the AOZ1242 to be disabled, an open drain or open collector circuit should be used to interface to EN pin.

Steady-State Operation

Under steady-state conditions, the converter operates in fixed frequency and Continuous-Conduction Mode (CCM).

The AOZ1242 integrates an internal N-MOSFET as the high-side switch. Inductor current is sensed by amplifying the voltage drop across the drain to source of the high side power MOSFET. Since the N-MOSFET requires a gate voltage higher than the input voltage, a boost capacitor connected between LX pin and BST pin drives the gate. The boost capacitor is charged while LX is low. An internal 10Ω switch from LX to GND is used to insure that LX is pulled to GND even in the light load. Output voltage is divided down by the external voltage divider at the FB pin. The difference of the FB pin voltage and reference is amplified by the internal transconductance error amplifier. The error voltage, which shows on the COMP pin, is compared against the current signal, which is sum of inductor current signal and ramp compensation signal, at PWM comparator input. If the current signal is less than the error voltage, the internal high-side switch is on. The inductor current flows from the input through the inductor to the output. When the current signal exceeds the error voltage, the high-side switch is off. The inductor current is freewheeling through the Schottky diode to output.

Switching Frequency

The AOZ1242 switching frequency is fixed and set by an internal oscillator. The switching frequency is set 370khz.

Output Voltage Programming

Output voltage can be set by feeding back the output to the FB pin with a resistor divider network. In the application circuit shown in Figure 1. The resistor divider network includes R_1 and R_2. Usually, a design is started by picking a fixed R_2 value and calculating the required R2 with equation below.

$$V_O = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

Some standard values for R_1 and R_2 for the most commonly used output voltages are listed in Table 1.

Table 1.

V_O (V)	R_1 (kΩ)	R_2 (kΩ)
0.8	1.0	Open
1.2	4.99	10
1.5	10	11.5
1.8	12.7	10.2
2.5	21.5	10
3.3	31.6	10
5.0	52.3	10

The combination of R_1 and R_2 should be large enough to avoid drawing excessive current from the output, which will cause power loss.

Protection Features

The AOZ1242 has multiple protection features to prevent system circuit damage under abnormal conditions.

Over Current Protection (OCP)

The sensed inductor current signal is also used for over current protection. Since the AOZ1242 employs peak current mode control, the COMP pin voltage is proportional to the peak inductor current. The COMP pin voltage is limited to be between 0.4V and 2.5V internally. The peak inductor current is automatically limited cycle-by-cycle.

The cycle-by-cycle current limit threshold is internally set. When the load current reaches the current limit threshold, the cycle by cycle current limit circuit turns off the high side switch immediately to terminate the current duty cycle. The inductor current stop rising. The cycle-by-cycle current limit protection directly limits inductor peak current. The average inductor current is also limited due to the limitation on peak inductor current.

When cycle by cycle current limit circuit is triggered, the output voltage drops as the duty cycle decreasing.

The AOZ1242 has internal short circuit protection to protect itself from catastrophic failure under output short circuit conditions. The FB pin voltage is proportional to the output voltage. Whenever FB pin voltage is below 0.2V, the short circuit protection circuit is triggered. To prevent current limit running away, when comp pin voltage is higher than 2.1 V, the short circuit protection is also triggered. As a result, the converter is shut down and hiccups at a frequency equals to 1/16 of normal switching frequency. The converter will start up via a soft start once the short circuit condition disappears. In short circuit protection mode, the inductor average current is greatly reduced because of the low hiccup frequency.

Power-On Reset (POR)

A power-on reset circuit monitors the input voltage. When the input voltage exceeds 4.3V, the converter starts operation. When input voltage falls below 4.1V, the converter will stop switching.

Thermal Protection

An internal temperature sensor monitors the junction temperature. It shuts down the internal control circuit and high side NMOS if the junction temperature exceeds 145°C. The regulator will restart automatically under the control of soft-start circuit when the junction temperature decreases to 100°C.

Application Information

The basic AOZ1242 application circuit is shown in Figure 1. Component selection is explained below.

Input Capacitor

The input capacitor (C_1 in Figure 1) must be connected to the V_{IN} pin and GND pin of the AOZ1242 to maintain steady input voltage and filter out the pulsing input current. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_O}{f \times C_{IN}} \times \left(1 - \frac{V_O}{V_{IN}}\right) \times \frac{V_O}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_O \times \sqrt{\frac{V_O}{V_{IN}}\left(1 - \frac{V_O}{V_{IN}}\right)}$$

if let *m* equal the conversion ratio:

$$\frac{V_O}{V_{IN}} = m$$

The relationship between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Figure 2. It can be seen that when V_O is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on CIN is 0.5 x I_O.

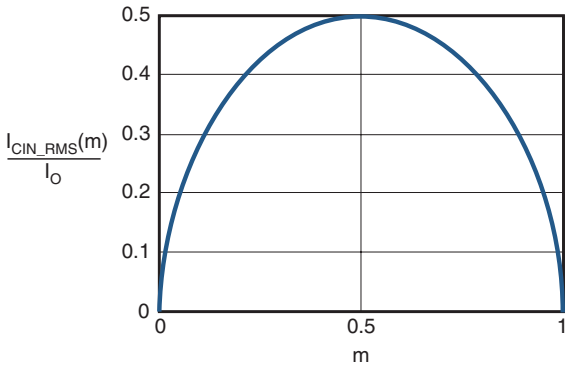


Figure 2. I_{CIN} vs. Voltage Conversion Ratio

For reliable operation and best performance, the input capacitors must have current rating higher than I_{CIN_RMS} at worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high ripple current rating. Depending on the application circuits, other low ESR tantalum capacitor or aluminum electrolytic capacitor may also be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors are preferred for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures is based on certain amount of life time. Further de-rating may be necessary for practical design requirement.

Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is,

$$\Delta I_L = \frac{V_O}{f \times L} \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

The peak inductor current is:

$$I_{Lpeak} = I_O + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also

reduces RMS current through inductor and switches, which results in less conduction loss.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor needs to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise, but they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_O = \Delta I_L \times \left(ESR_{CO} + \frac{1}{8 \times f \times C_O} \right)$$

where;

C_O is output capacitor value and

ESR_{CO} is the Equivalent Series Resistor of output capacitor.

When low ESR ceramic capacitor is used as output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_O = \Delta I_L \times \frac{1}{8 \times f \times C_O}$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_O = \Delta I_L \times ESR_{CO}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum capacitor or aluminum electrolytic capacitor may also be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{CO\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, output capacitor could be overstressed.

Schottky Diode Selection

The external freewheeling diode supplies the current to the inductor when the high side NMOS switch is off. To reduce the losses due to the forward voltage drop and recovery of diode, Schottky diode is recommended to use. The maximum reverse voltage rating of the chosen Schottky diode should be greater than the maximum input voltage, and the current rating should be greater than the maximum load current.

Loop Compensation

The AOZ1242 employs peak current mode control for easy use and fast transient response. Peak current mode control eliminates the double pole effect of the output L&C filter. It greatly simplifies the compensation loop design.

With peak current mode control, the buck power stage can be simplified to be a one-pole and one-zero system in frequency domain. The pole is dominant pole and can be calculated by:

$$f_{p1} = \frac{1}{2\pi \times C_O \times R_L}$$

The zero is a ESR zero due to output capacitor and its ESR. It is can be calculated by:

$$f_{Z1} = \frac{1}{2\pi \times C_O \times ESR_{CO}}$$

where;

C_O is the output filter capacitor,

R_L is load resistor value, and

ESR_{CO} is the equivalent series resistance of output capacitor.

The compensation design is actually to shape the converter close loop transfer function to get desired gain and phase. Several different types of compensation network can be used for AOZ1242. For most cases, a series capacitor and resistor network connected to the COMP pin sets the pole-zero and is adequate for a stable high-bandwidth control loop.

In the AOZ1242, FB pin and COMP pin are the inverting input and the output of internal transconductance error amplifier. A series R and C compensation network connected to COMP provides one pole and one zero. The pole is:

$$f_{p2} = \frac{G_{EA}}{2\pi \times C_C \times G_{VEA}}$$

where;

G_{EA} is the error amplifier transconductance, which is 200 x 10^{-6} A/V,

G_{VEA} is the error amplifier voltage, and

C_C is the compensation capacitor

The zero given by the external compensation network, capacitor C_C (C_5 in Figure 1) and resistor R_C (R_1 in Figure 1), is located at:

$$f_{Z2} = \frac{1}{2\pi \times C_C \times R_C}$$

To design the compensation circuit, a target crossover frequency f_C for close loop must be selected. The system crossover frequency is where control loop has unity gain. The crossover frequency is also called the converter bandwidth. Generally a higher bandwidth means faster response to load transient. However, the bandwidth should not be too high due to system stability concern. When designing the compensation loop, converter stability under all line and load condition must be considered.

Usually, it is recommended to set the bandwidth to be less than 1/10 of switching frequency. It is recommended to choose a crossover frequency less than 30kHz.

$$f_C = 30kHz$$

The strategy for choosing R_C and C_C is to set the cross over frequency with R_C and set the compensator zero with C_C. Using selected crossover frequency, f_C, to calculate R_C:

$$R_C = f_C \times \frac{V_O}{V_{FB}} \times \frac{2\pi \times C_O}{G_{EA} \times G_{CS}}$$

where;

f_C is desired crossover frequency,

V_{FB} is 0.8V,

G_{EA} is the error amplifier transconductance, which is 200x10^{-6} A/V, and

G_{CS} is the current sense circuit transconductance, which is 5.64 A/V

The compensation capacitor C_C and resistor R_C together make a zero. This zero is put somewhere close to the dominate pole f_{p1} but lower than 1/5 of selected crossover frequency. C_C can is selected by:

$$C_C = \frac{1.5}{2\pi \times R_C \times f_{p1}}$$

The equation above can also be simplified to:

$$C_C = \frac{C_O \times R_L}{R_C}$$

An easy-to-use application software which helps to design and simulate the compensation loop can be found at www.aosmd.com.

Thermal Management and Layout Consideration

In the AOZ1242 buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the V_{IN} pin, to the LX pins, to the filter inductor, to the output capacitor and load, and then return to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from inductor, to the output capacitors and load, to the GND pin of the AOZ1242, to the LX pins of the AZO1242. Current flows in the second loop when the low side diode is on.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is recommended to connect input capacitor, output capacitor, and GND pin of the AOZ1242.

In the AOZ1242 buck regulator circuit, the three major power dissipating components are the AOZ1242, external diode and output inductor. The total power dissipation of converter circuit can be measured by input power minus output power.

$$P_{total\_loss} = V_{IN} \times I_{IN} - V_O \times I_O$$

The power dissipation of inductor can be approximately calculated by output current and DCR of the inductor.

$$P_{inductor\_loss} = I_O^2 \times R_{inductor} \times 1.1$$

The power dissipation of the diode is:

$$P_{diode\_loss} = I_O \times V_F \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

The actual AOZ1242 junction temperature can be calculated with power dissipation in the AOZ1242 and thermal impedance from junction to ambient.

$$T_{junction} = (P_{total\_loss} - P_{inductor\_loss}) \times \Theta_{JA} + T_{ambient}$$

The maximum junction temperature of AOZ1242 is 145°C, which limits the maximum load current capability.

The thermal performance of the AOZ1242 is strongly affected by the PCB layout. Extra care should be taken by users during design process to ensure that the IC will operate under the recommended environmental conditions.

Several layout tips are listed below for the best electric and thermal performance. Figure 3a and Figure 3b give the example of layout for AOZ1242A and AOZ1242D respectively.

1. Do not use thermal relief connection to the V_{IN} and the GND pin. Pour a maximized copper area to the GND pin and the V_{IN} pin to help thermal dissipation.
2. Input capacitor should be connected to the V_{IN} pin and the GND pin as close as possible.
3. Make the current trace from LX pins to L to Co to the GND as short as possible.
4. Pour copper plane on all unused board area and connect it to stable DC nodes, like V_{IN}, GND or V_{OUT}.
5. Keep sensitive signal trace such as trace connected with FB pin and COMP pin far away form the LX pins.

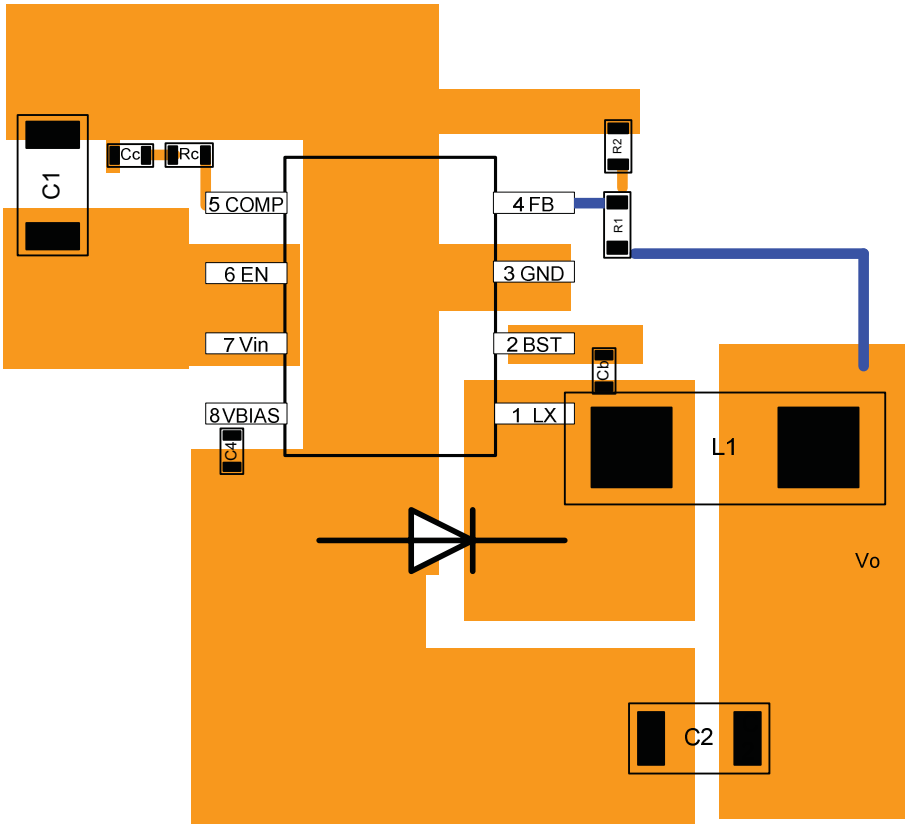


Figure 3a. Layout Example for AOZ1242AI

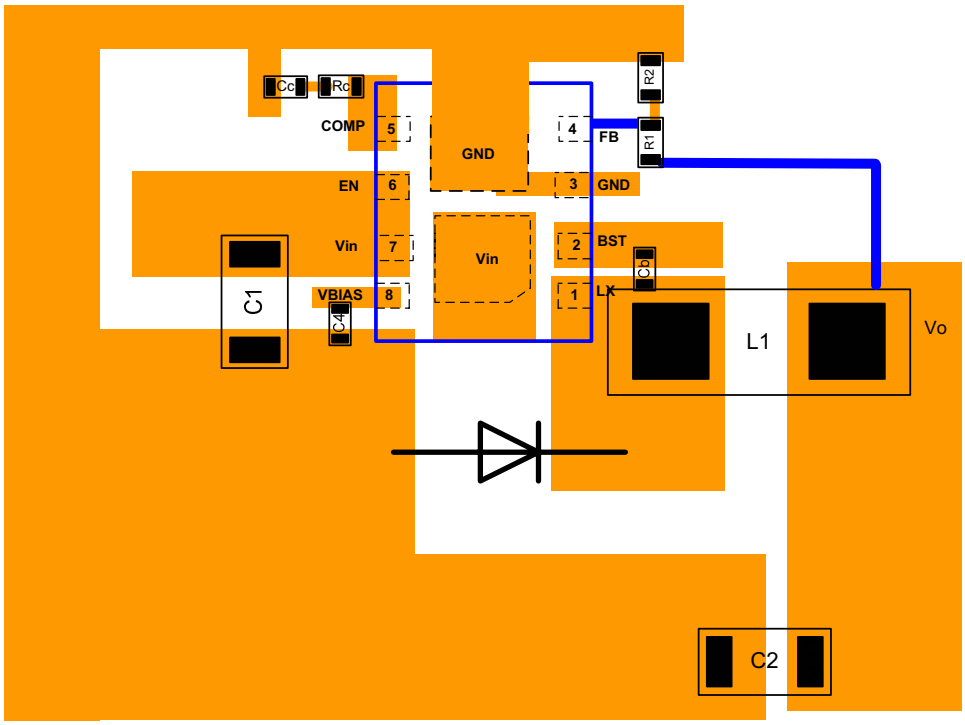
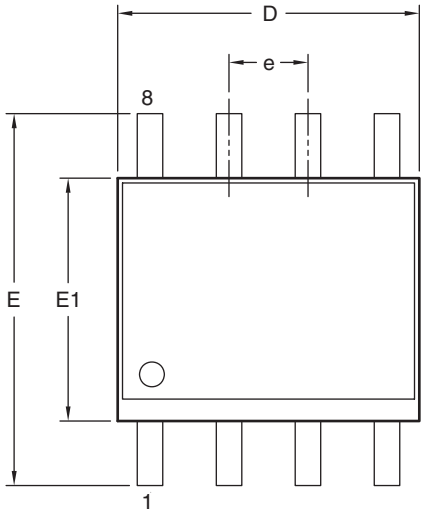
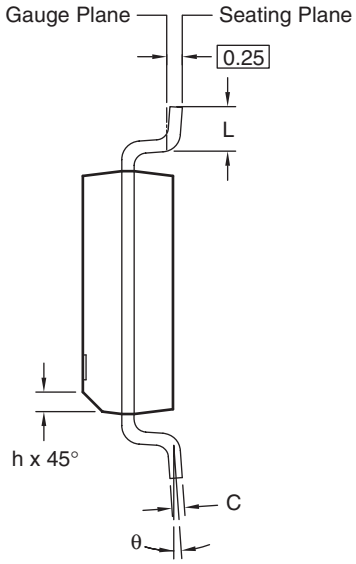
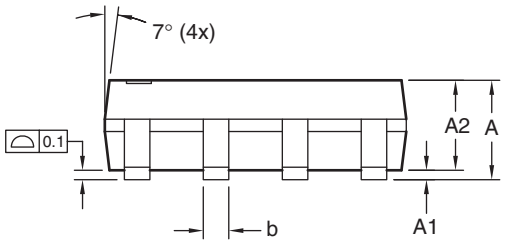


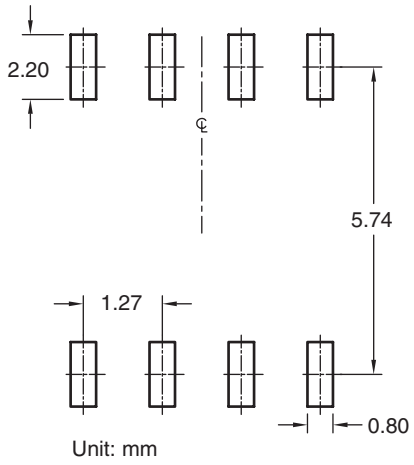
Figure 3b. Layout Example for AOZ1242DI

Package Dimensions, SO-8









Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	1.35	1.65	1.75
A1	0.10	—	0.25
A2	1.25	1.50	1.65
b	0.31	—	0.51
c	0.17	—	0.25
D	4.80	4.90	5.00
E1	3.80	3.90	4.00
e	1.27 BSC		
E	5.80	6.00	6.20
h	0.25	—	0.50
L	0.40	—	1.27
θ	0°	—	8°

Dimensions in inches

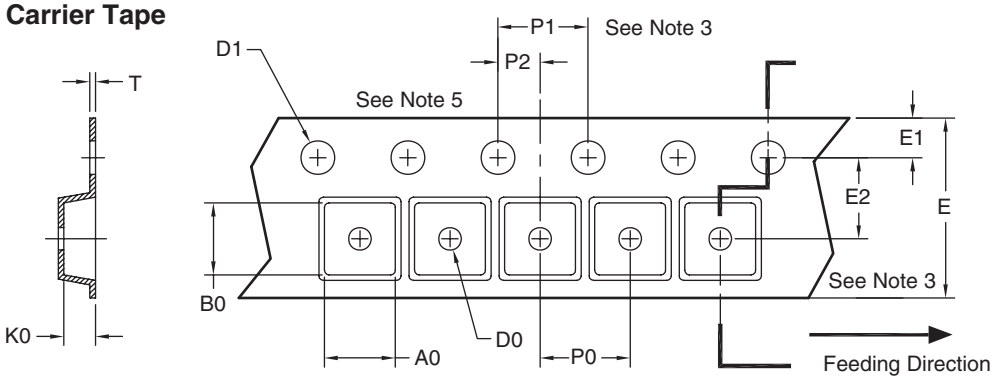
Symbols	Min.	Nom.	Max.
A	0.053	0.065	0.069
A1	0.004	—	0.010
A2	0.049	0.059	0.065
b	0.012	—	0.020
c	0.007	—	0.010
D	0.189	0.193	0.197
E1	0.150	0.154	0.157
e	0.050 BSC		
E	0.228	0.236	0.244
h	0.010	—	0.020
L	0.016	—	0.050
θ	0°	—	8°

Notes:

1. All dimensions are in millimeters.
2. Dimensions are inclusive of plating
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

Tape and Reel Dimensions, SO-8

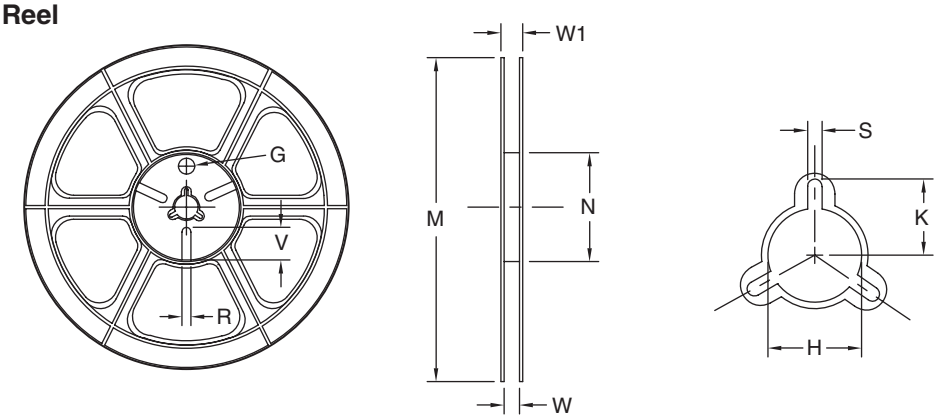
SO-8 Carrier Tape



Unit: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SO-8 (12mm)	6.40 ±0.10	5.20 ±0.10	2.10 ±0.10	1.60 ±0.10	1.50 ±0.10	12.00 ±0.10	1.75 ±0.10	5.50 ±0.10	8.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.25 ±0.10

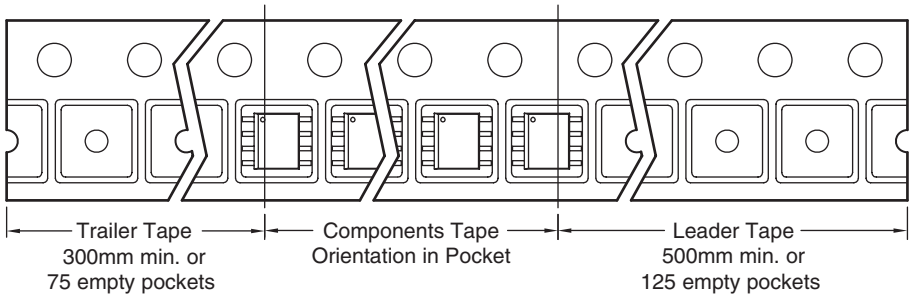
SO-8 Reel



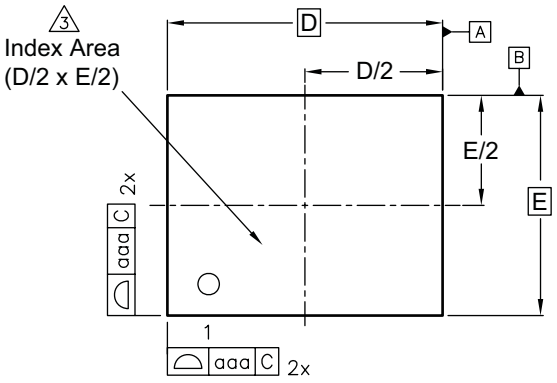
Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12mm	ø330	ø330.00 ±0.50	ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	ø13.00 +0.50/-0.20	10.60	2.00 ±0.50	—	—	—

SO-8 Tape

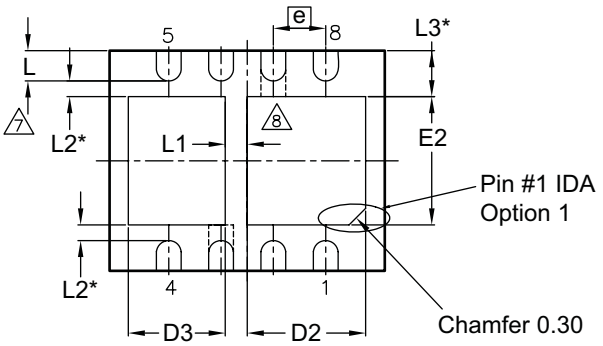
Leader/Trailer & Orientation



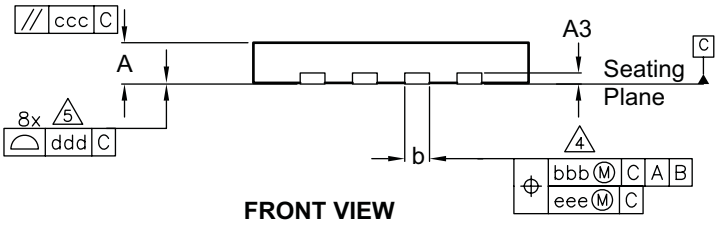
Package Dimensions, 5x4A DFN-8



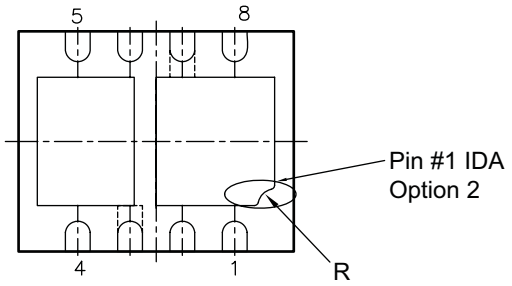
6 TOP VIEW



BOTTOM VIEW

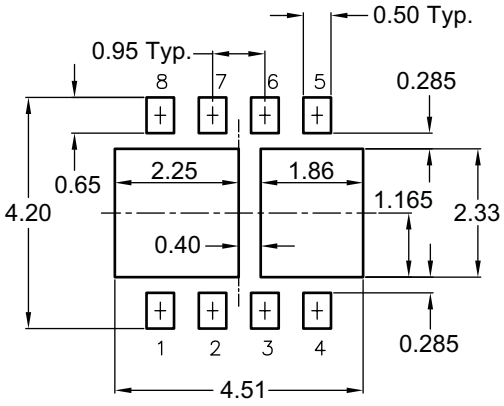


FRONT VIEW



BOTTOM VIEW

RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	0.70	0.75	0.80
A3		0.20 Ref.	
b	0.40	0.45	0.50
D	4.90	5.00	5.10
D2	2.05	2.15	2.25
D3	1.66	1.76	1.86
E	3.90	4.00	4.10
E2	2.23	2.33	2.43
e		0.95 BSC	
L	0.50	0.55	0.60
L1	—	0.40	—
L2		0.285 Ref.	
L3		0.835 Ref.	
R		0.30 Ref.	
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.08	
eee		0.05	

Dimensions in inches

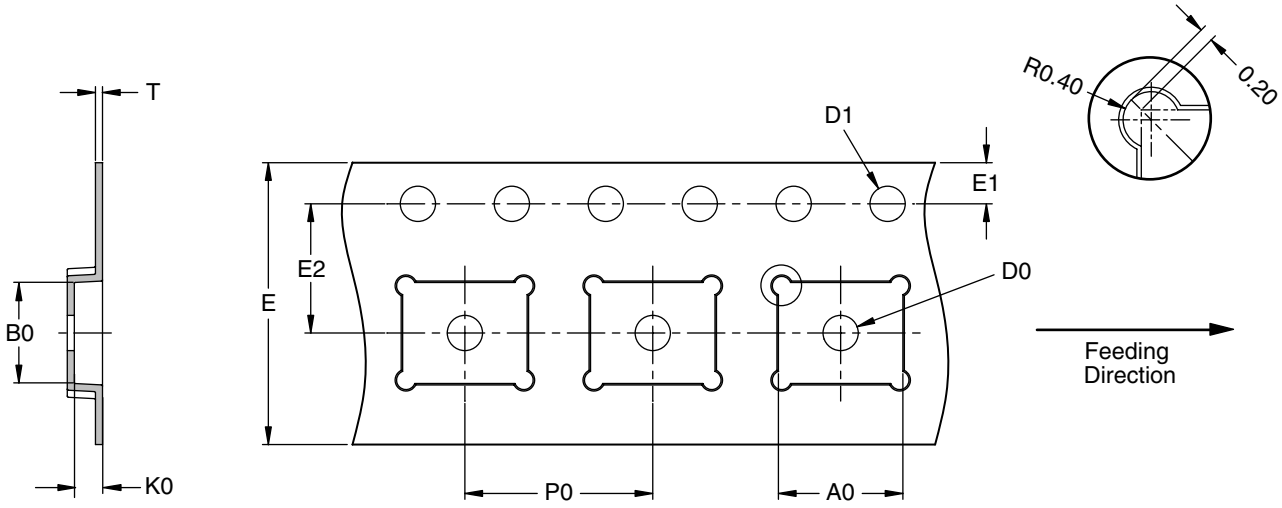
Symbols	Min.	Nom.	Max.
A	0.028	0.30	0.032
A3		0.008 Ref.	
b	0.016	0.018	0.020
D	0.190	0.200	0.201
D2	0.080	0.085	0.089
D3	0.064	0.070	0.074
E	0.154	0.157	0.161
E2	0.088	0.092	0.096
e		0.037 BSC	
L	0.020	0.022	0.024
L1	—	0.016	—
L2		0.011 Ref.	
L3		0.033 Ref.	
R		0.012 Ref.	
aaa		0.006	
bbb		0.004	
ccc		0.004	
ddd		0.003	
eee		0.002	

Notes:

1. Dimensions and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters.
3. The location of the terminal #1 identifier and terminal numbering convention conforms to JEDEC publication 95 SP-002.
4. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
5. Coplanarity applies to the terminals and all other bottom surface metallization.
6. Drawing shown are for illustration only.
7. The dimensions with * are just for reference
8. Pin #3 and Pin #7 are fused to DAP.

Tape and Reel Dimensions, 5x4A DFN-8

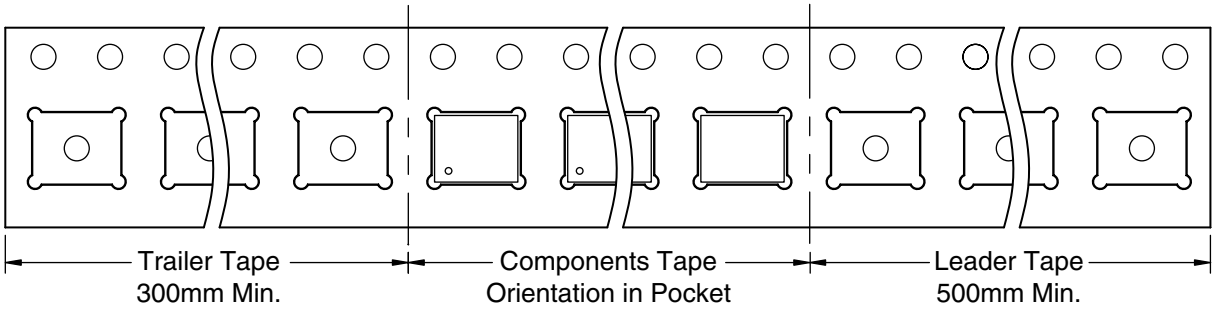
Tape



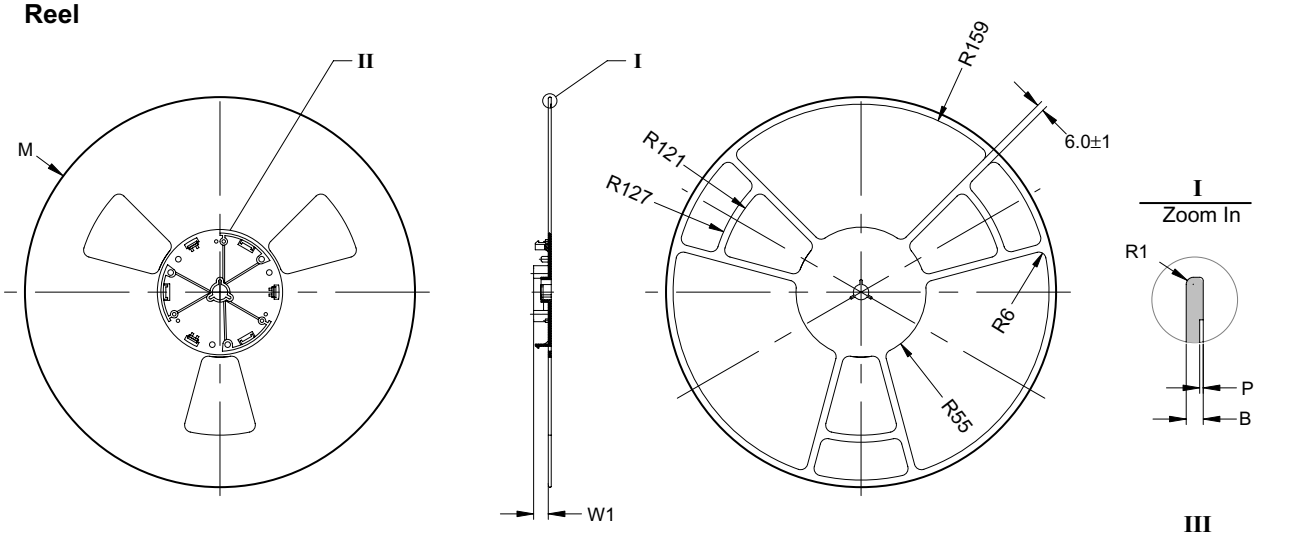
UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN 5x4 (12 mm)	5.30 ±0.10	4.30 ±0.10	1.20 ±0.10	1.50 Min. Typ.	1.50 +0.10 / –0	12.00 ±0.30	1.75 ±0.10	5.50 ±0.10	8.00 ±0.10	4.00 ±0.20	2.00 ±0.10	0.30 ±0.05

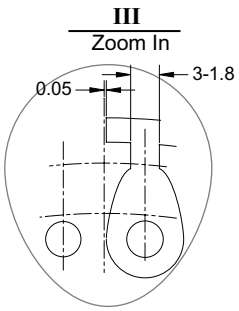
Leader/Trailer and Orientation

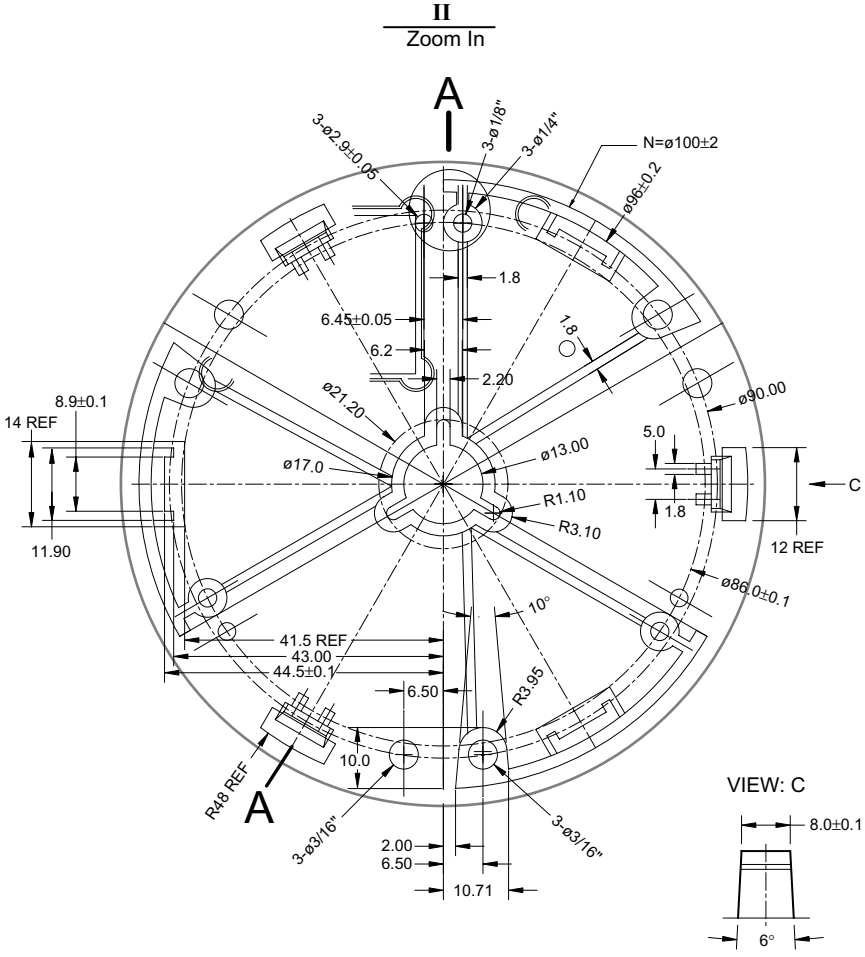


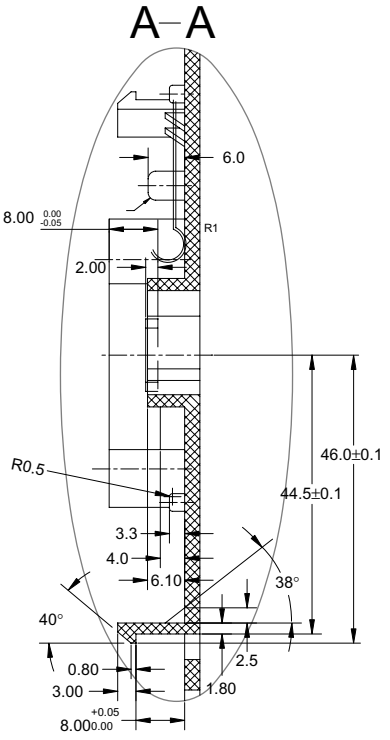
Reel



Tape Size	Reel Size	M	W1	B	P
12mm	ø330	ø330 +0.3 -4.0	12.40 +2.0 -0.0	2.40 ±0.3	0.5

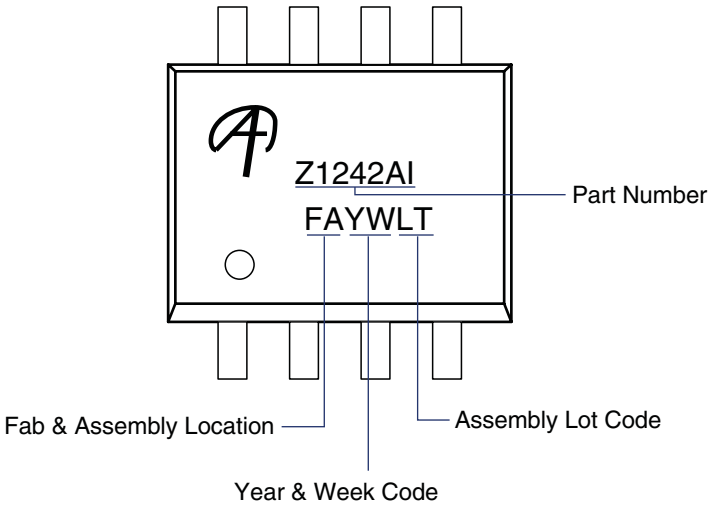




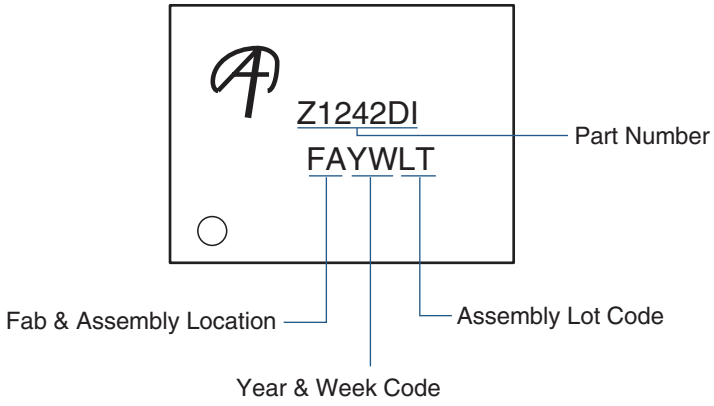


Part Marking

AOZ1242AI



AOZ1242DI



This data sheet contains preliminary data; supplementary data may be published at a later date.
Alpha & Omega Semiconductor reserves the right to make changes at any time without notice.

LIFE SUPPORT POLICY

ALPHA & OMEGA SEMICONDUCTOR PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.