TEXAS INSTRUMENTS

ADS7950, ADS7951, ADS7952, ADS7953, ADS7954, ADS7955
ADS7956, ADS7957, ADS7958, ADS7959, ADS7960, ADS7961

SLAS605C – JUNE 2008 – REVISED JULY 2018

ADS79xx Pin Compatible, 12-, 10-, 8-Bit, 1-MSPS, 16-, 12-, 8-, 4-Channel, Single-Ended, Serial Interface ADCs

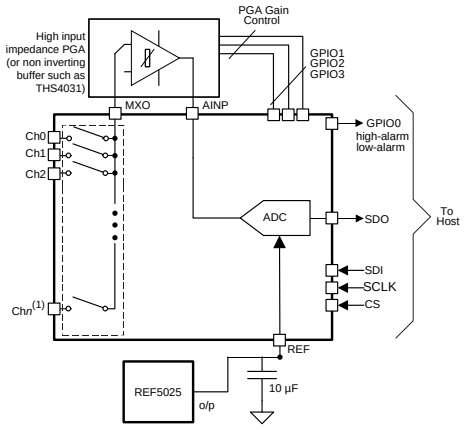
1 Features

- 1-MHz Sample Rate Serial Devices
- Product Family of 12-, 10-, 8-Bit Resolution
- Zero Latency
- 20-MHz Serial Interface
- Analog Supply Range: 2.7 to 5.25 V
- I/O Supply Range: 1.7 to 5.25 V
- Two SW Selectable Unipolar, Input Ranges: 0 to V_{REF} and 0 to 2 x V_{REF}
- Auto and Manual Modes for Channel Selection
- 4-, 8-Channel Devices and 12-, 16-Channel Devices Share the Same Footprint
- Two Programmable Alarm Levels per Channel
- Four Individually Configurable GPIOs in TSSOP Package: One GPIO in VQFN Package
- Typical Power Dissipation: 14.5 mW (+VA = 5 V, +VBD = 3 V) at 1 MSPS
- Power-Down Current (1 μA)
- Input Bandwidth (47 MHz at 3 dB)
- 38-, 30-Pin TSSOP and 32-, 24-Pin VQFN Packages

2 Applications

- PLC/IPC
- Optical Line Card Monitoring
- Medical Instrumentation
- Digital Power Supplies
- Multi-Channel, General-Purpose Signal Monitoring
- High-Speed Data Acquisition Systems
- High-Speed Closed-Loop Systems

Detailed Block Diagram



3 Description

The ADS79xx is a 12-, 10-, 8-bit pin compatible multichannel analog-to-digital converter family. The device comparison table shows all twelve devices from this product family.

The devices include a capacitor based SAR A/D converter with inherent sample and hold.

The devices accept a wide analog supply range from 2.7 V to 5.25 V. Very low power consumption makes these devices suitable for battery-powered and isolated power-supply applications.

A wide 1.7-V to 5.25-V I/O supply range facilitates a glueless interface with the most commonly used digital hosts. The serial interface is controlled by $\overline{CS}$ and SCLK for easy connection with microprocessors and DSP.

The input signal is sampled with the falling edge of $\overline{CS}$. It uses SCLK for conversion, serial data output, and reading serial data in. The devices allow auto sequencing of preselected channels or manual selection of a channel for the next conversion cycle.

There are two software selectable input ranges (0 V to V_{REF} and 0 V to 2 × V_{REF}), individually configurable GPIOs (four in case of the TSSOP and one on the VQFN package devices), and two programmable alarm thresholds per channel. These features make the devices suitable for most data acquisition applications.

The devices offer an attractive power-down feature. This is extremely useful for power saving when the device is operated at lower conversion speeds.

The 16-, 12-channel devices from this family are available in a 38-pin TSSOP and 32 pin VQFN package and the 4/8-channel devices are available in a 30-pin TSSOP and 24 pin VQFN packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS79xx	TSSOP (30)	7.80 mm × 4.40 mm
	VQFN (24)	4.00 mm × 4.00 mm
	TSSOP (38)	9.70 mm × 4.40 mm
	VQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (July 2015) to Revision C **Page**

- Changed *0 to 2.5 V and 0 to 5 V* to *0 to V_{REF} and 0 to 2 x V_{REF}* in *Input Range* Features bullet ... 1
- Changed GPIO *Features* bullet ... 1
- Changed *Optical Line Card Monitoring* and *Multi-Channel, General-Purpose Signal Monitoring* Applications bullets ... 1
- Changed *(0 V to 2.5 V and 0 V to 5 V)* to *(0 V to V_{REF} and 0 V to 2 × V_{REF})* in *Description* section ... 1
- Deleted *Companion Products* table ... 5
- Changed RGE to RHB for two 32-pin VQFN pin diagrams ... 5
- Added 30-pin DBT package ... 5
- Changed I/O column of *Pin Functions: TSSOP Packages* table to show full definition instead of abbreviation ... 6
- Added *active low* to definition of $\overline{CS}$ pin in *Pin Functions: TSSOP Packages* table ... 7
- Changed pin name and description of Alarm pin in *Pin Functions: TSSOP Packages* table ... 7
- Added settings to description of Range pin in *Pin Functions: TSSOP Packages* table: added (1) to high and (0) to low ... 7
- Added *active low* to description of CS pin in *Pin Functions: VQFN Packages* table ... 8
- Changed pin name and description of Alarm pin in *Pin Functions: VQFN Packages* table ... 9
- Changed value of *Input current to any pin except supply pins* row from ±10 mA (max) to –10 mA (min) and 10 mA (max) in *Absolute Maximum Ratings* table ... 10
- Changed *VBD = 1.7 V to 5.25 V* to *VBD = 1.7 V to +VA* in condition statement ... 12
- Changed minimum specification from –1 LSB to –0.99 LSB in first row of *Differential linearity* parameter ... 12
- Added *input* to *Reference input resistance* parameter name ... 13
- Changed maximum specification from *FFC Hex* to *4092 LSB* in *Alarm Setting* parameters ... 13
- Changed unit from *Numbers* to *Conversion* in *Invalid conversions after power up or reset* parameter ... 13
- Changed *VBD = 1.7 V to 5.25 V* to *VBD = 1.7 V to +VA* in condition statement ... 14

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- Added *input* to *Reference input resistance* parameter name 14
- Changed maximum specification from *FFC Hex* to *4092 LSB* in *Alarm Setting* parameters 14
- Changed *VBD = 1.7 V to 5.25 V* to *VBD = 1.7 V to +VA* in condition statement 15
- Added *input* to *Reference input resistance* parameter name 16
- Changed maximum specification from *FF Hex* to *255 LSB* in *Alarm Setting* parameters 16
- Changed unit from *Numbers* to *Conversion* in *Invalid conversions after power up or reset* parameter 16
- Changed *REF and GND pins* to *REFP and REFM pins* in the *Reference* section 29
- Added *Example Manual Mode Timing Diagram* figure and corresponding text to *Operating in Manual Mode* section 33
- Added *Example Auto-1 Mode Timing Diagram* figure and corresponding text to the *Operating in Auto-1 Mode* section 35
- Added *Example Auto-2 Mode Timing Diagram* figure and corresponding text to the *Operating in Auto-2 Mode* section 39
- Changed *2.5V* to V_{REF} in first DI06 row and *5V* to $2xV_{REF}$ in second DI06 row 40
- Changed binary code from *0001 1111 1111* to *0011 1111 1111* in Full scale row of *Ideal Input Voltages for 10-Bit Devices and Digital Output Codes for 10-Bit Devices (ADS7954/55/56/57)* table 41
- Changed *10-Bit* to *8-Bit* in title of *Ideal Input Voltages for 8-Bit Devices and Digital Output Codes for 8-Bit Devices (ADS7958/59/60/61)* table 42
- Changed *Application Diagram for an Unbuffered MXO* figure note 48
- Changed *Recommended Layout* figure title to *Recommended Layout for the TSSOP Packaged Device* 52
- Added *Recommended Layout for the VQFN Packaged Device* figure 53

Changes from Revision A (April 2010) to Revision B **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Changes from Original (June 2008) to Revision A **Page**

- Added QFN information to Features 1
- Added QFN information to Description 1
- Changed VEE to AGND and VCC to +VA on 38-pin TSSOP pinout 5
- Added QFN pinout 5
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- Added QFN pinout 6
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- Added terminal functions for QFN packages 8
- Changed ADS7950/4/8 QFN package MXO pin from 7 to 3 8
- Added V_{REF} = 2.5 V ± 0.1 V to *Electrical Characteristics*, ADS7950/51/52/53 12
- Added while $2V_{REF} \leq$ +VA to full-scale input span range 2 test conditions 12
- Added while $2V_{REF} \leq$ +VA to Absolute input range span range 2 test conditions 12
- Added Total unadjusted error (TUE) specification 12
- Changed reference voltage at REFP min and max values 13
- Added Note to *Electrical Characteristics*, ADS7950/51/52/53 13
- Added V_{REF} = 2.5 V ± 0.1 V to *Electrical Characteristics*, ADS7954/55/56/57 test conditions 14
- Added while $2V_{REF} \leq$ +VA to full-scale input span range 2 test conditions 14
- Added while $2V_{REF} \leq$ +VA to full-scale input span range 2 test conditions 14

- Changed V_{ref} reference voltage at REFP min value from 2.49 V to 2.0 V 14
- Changed V_{ref} reference voltage at REFP max value from 2.51 V to 3.0 V 14
- Added V_{ref} = 2.5 V ± 0.1 V to *Electrical Characteristics*, ADS7958/59/60/61 test conditions..... 15
- Added while $2V_{REF}$ ≤ +VA to full-scale input span range 2 test conditions 15
- Added while $2V_{REF}$ ≤ +VA to full-scale input span range 2 test conditions 15
- Changed V_{ref} reference voltage at REFP min value from 2.49 V to 2.0 V 16
- Changed V_{ref} reference voltage at REFP max value from 2.51 V to 3.0 V 16
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- Changed GPIO pins description 28
- Added device powerdown through GPIO in the case of the TSSOP packaged devices 28
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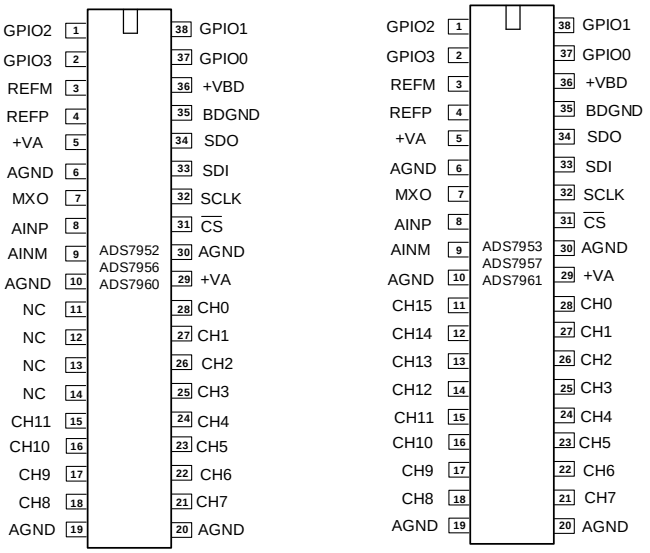
- Added note to Table 2 36
- Added note to Table 5 40
- Added note to Programming GPIO Registers description..... 42
- Added QFN information to Table 11..... 43
- Changed DI12 = 1? from No or No to Yes or No in Figure 59..... 44
- Added note to Figure 60..... 46

5 Device Comparison Table

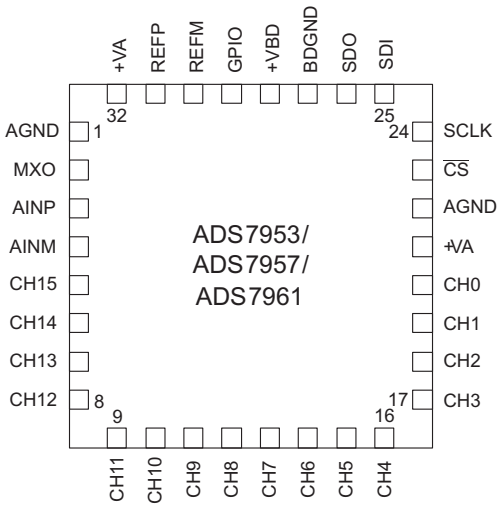
NUMBER OF CHANNELS	RESOLUTION		
	12 BIT	10 BIT	8 BIT
16	ADS7953	ADS7957	ADS7961
12	ADS7952	ADS7956	ADS7960
8	ADS7951	ADS7955	ADS7959
4	ADS7950	ADS7954	ADS7958

6 Pin Configuration and Functions

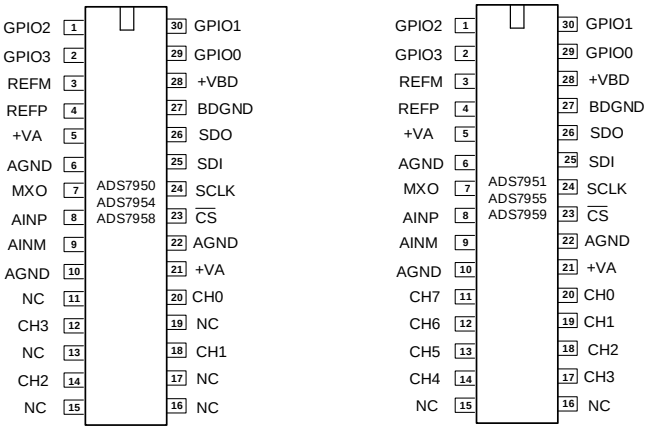
DBT Package
38-Pin TSSOP
Top View



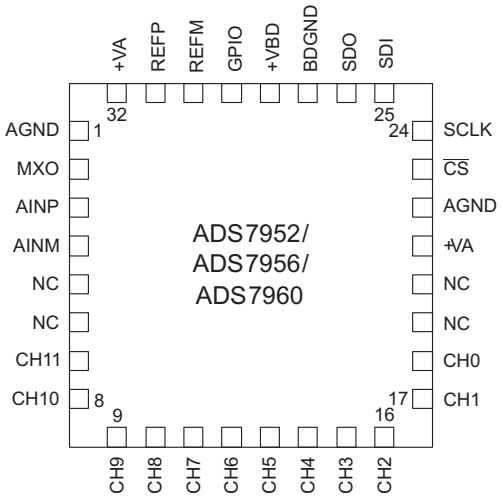
RHB Package
32-Pin VQFN
Top View



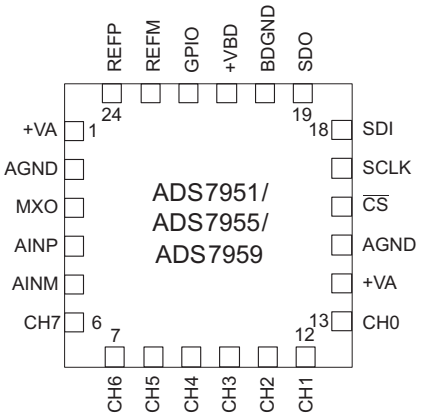
DBT Package
30-Pin TSSOP
Top View



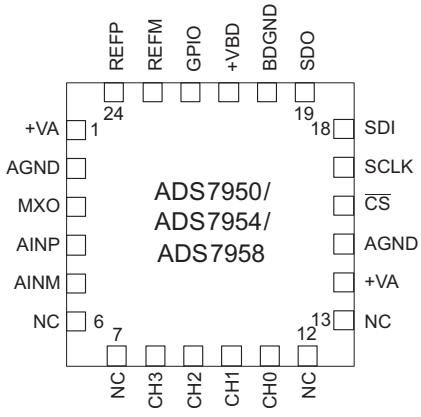
RHB Package
32-Pin VQFN
Top View



RGE Package
24-Pin VQFN
Top View



RGE Package
24-Pin VQFN
Top View



Pin Functions: TSSOP Packages

PIN					I/O	DESCRIPTION
NAME	ADS7953 ADS7957 ADS7961	ADS7952 ADS7956 ADS7960	ADS7951 ADS7955 ADS7959	ADS7950 ADS7954 ADS7958		
REFERENCE						
REFP	4	4	4	4	Analog input	Reference input
REFM	3	3	3	3	Analog input	Reference ground
ADC ANALOG INPUT						
AINP	8	8	8	8	Analog input	ADC input signal
AINM	9	9	9	9	Analog input	ADC input ground
MULTIPLEXER						
MXO	7	7	7	7	Analog output	Multiplexer output
Ch0	28	28	20	20	Analog input	Analog channel for multiplexer
Ch1	27	27	19	18	Analog input	Analog channel for multiplexer
Ch2	26	26	18	14	Analog input	Analog channel for multiplexer
Ch3	25	25	17	12	Analog input	Analog channel for multiplexer
Ch4	24	24	14	—	Analog input	Analog channel for multiplexer
Ch5	23	23	13	—	Analog input	Analog channel for multiplexer
Ch6	22	22	12	—	Analog input	Analog channel for multiplexer
Ch7	21	21	11	—	Analog input	Analog channel for multiplexer
Ch8	18	18	—	—	Analog input	Analog channel for multiplexer
Ch9	17	17	—	—	Analog input	Analog channel for multiplexer

Pin Functions: TSSOP Packages (continued)

PIN					I/O	DESCRIPTION
NAME	ADS7953 ADS7957 ADS7961	ADS7952 ADS7956 ADS7960	ADS7951 ADS7955 ADS7959	ADS7950 ADS7954 ADS7958		
Ch10	16	16	—	—	Analog input	Analog channel for multiplexer
Ch11	15	15	—	—	Analog input	Analog channel for multiplexer
Ch12	14	—	—	—	Analog input	Analog channel for multiplexer
Ch13	13	—	—	—	Analog input	Analog channel for multiplexer
Ch14	12	—	—	—	Analog input	Analog channel for multiplexer
Ch15	11	—	—	—	Analog input	Analog channel for multiplexer
DIGITAL CONTROL SIGNALS						
$\overline{CS}$	31	31	23	23	Digital input	Chip-select input pin; active low
SCLK	32	32	24	24	Digital input	Serial clock input pin
SDI	33	33	25	25	Digital input	Serial data input pin
SDO	34	34	26	26	Digital output	Serial data output pin
GENERAL-PURPOSE INPUTS/OUTPUTS(1)						
GPIO0	37	37	29	29	Digital I/O	General-purpose input or output
Alarm					Digital output	Active high alarm output. For configuration, see the *Programming* section.
GPIO1	38	38	30	30	Digital I/O	General-purpose input or output
Low alarm					Digital output	Active high output indicating low alarm
GPIO2	1	1	1	1	Digital I/O	General-purpose input or output
Range					Digital input	Selects ADC input range: High (1) -> Range 2 (0 to $2xV_{REF}$) / Low (0) -> Range 1 (0 to V_{REF})
GPIO3	2	2	2	2	Digital I/O	General-purpose input or output
$\overline{PD}$					Digital input	Active low power-down input
POWER SUPPLY AND GROUND						
+VA	5, 29	5, 29	5, 21	5, 21	—	Analog power supply
AGND	6, 10, 19, 20, 30	6, 10, 19, 20, 30	6, 10, 22	6, 10, 22	—	Analog ground
+VBD	36	36	28	28	—	Digital I/O supply
BDGND	35	35	27	27	—	Digital ground
NC PINS						
—	—	11, 12, 13, 14	15, 16	11, 13, 15, 16, 17, 19	—	Pins internally not connected, do not float these pins, connect these pins to ground

(1) These pins have programmable dual functionality. See Table 12 for functionality programming.

Pin Functions: VQFN Packages

PIN					I/O	DESCRIPTION
PIN NAME	ADS7953 ADS7957 ADS7961	ADS7952 ADS7956 ADS7960	ADS7951 ADS7955 ADS7959	ADS7950 ADS7954 ADS7958		
REFERENCE						
REFP	31	31	24	24	Analog input	Reference input
REFM	30	30	23	23	Analog input	Reference ground
ADC ANALOG INPUT						
AINP	3	3	4	4	Analog input	ADC input signal
AINM	4	4	5	5	Analog input	ADC input ground
MULTIPLEXER						
MXO	2	2	3	3	Analog output	Multiplexer output
Ch0	20	18	13	11	Analog input	Analog-input channel for multiplexer
Ch1	19	17	12	10	Analog input	Analog-input channel for multiplexer
Ch2	18	16	11	9	Analog input	Analog-input channel for multiplexer
Ch3	17	15	10	8	Analog input	Analog-input channel for multiplexer
Ch4	16	14	9	—	Analog input	Analog-input channel for multiplexer
Ch5	15	13	8	—	Analog input	Analog-input channel for multiplexer
Ch6	14	12	7	—	Analog input	Analog-input channel for multiplexer
Ch7	13	11	6	—	Analog input	Analog-input channel for multiplexer
Ch8	12	10	—	—	Analog input	Analog-input channel for multiplexer
Ch9	11	9	—	—	Analog input	Analog-input channel for multiplexer
Ch10	10	8	—	—	Analog input	Analog-input channel for multiplexer
Ch11	9	7	—	—	Analog input	Analog-input channel for multiplexer
Ch12	8	—	—	—	Analog input	Analog-input channel for multiplexer
Ch13	7	—	—	—	Analog input	Analog-input channel for multiplexer
Ch14	6	—	—	—	Analog input	Analog-input channel for multiplexer
Ch15	5	—	—	—	Analog input	Analog-input channel for multiplexer
DIGITAL CONTROL SIGNALS						
$\overline{CS}$	23	23	16	16	Digital input	Chip-select input pin; active low
SCLK	24	24	17	17	Digital input	Serial clock input pin
SDI	25	25	18	18	Digital input	Serial data input pin

Pin Functions: VQFN Packages (continued)

PIN					I/O	DESCRIPTION
PIN NAME	ADS7953 ADS7957 ADS7961	ADS7952 ADS7956 ADS7960	ADS7951 ADS7955 ADS7959	ADS7950 ADS7954 ADS7958		
SDO	26	26	19	19	Digital output	Serial data output pin
GENERAL-PURPOSE INPUT/OUTPUT(1)						
GPIO0	29	29	22	22	Digital I/O	General purpose input or output
Alarm					Digital output	Active high alarm output. For configuration, see the *Programming* section.
POWER SUPPLY AND GROUND						
+VA	21, 32	21, 32	1, 14	1, 14	—	Analog power supply
AGND	1, 22	1, 22	2, 15	2, 15	—	Analog ground
+VBD	28	28	21	21	—	Digital I/O supply
BDGND	27	27	20	20	—	Digital ground
NC PINS						
—	—	5, 6, 19, 20	—	6, 7, 12, 13	—	Pins internally not connected, do not float these pins, connect these pins to ground

(1) This pin has programmable dual functionality. See Table 12 for functionality programming.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
AINP or CHn to AGND	–0.3	VA +0.3	V
+VA to AGND, +VBD to BDGND	–0.3	7	V
Digital input voltage to BDGND	–0.3	7	V
Digital output to BDGND	–0.3	VA + 0.3	V
Input current to any pin except supply pins	–10	10	mA
Operating temperature	–40	125	°C
Junction temperature (T_J Max)		150	°C
Storage temperature (T_{stg})	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) DBT packaged versions of ADS79xx family devices are rated for MSL2 260°C per the JSTD-020 specifications and the RGE and RHB packaged versions of ADS79xx family devices are rated for MSL3 260C per JSTD-020 specifications

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{(+VA)}$	Analog power-supply voltage	2.7	3.3	5.25	V
$V_{(+VBD)}$	Digital I/O-supply voltage	1.7	3.3	$V_{(+VA)}$	V
$V_{(REF)}$	Reference voltage	2	2.5	3	V
$f_{(SCLK)}$	SCLK frequency			20	MHz
T_A	Operating temperature range	–40		125	°C

7.4 Thermal Information: TSSOP

THERMAL METRIC(1)		ADS795x		UNIT
		DBT (TSSOP)	DBT (TSSOP)	
		38 PINS	30 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.6	89.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.8	22.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.7	43.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.9	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44.1	42.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: VQFN

THERMAL METRIC(1)		ADS7953, ADS7957, ADS7961		UNIT
		RHB (VQFN)	RGE (VQFN)	
		32 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.6	36.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.1	39.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.1	14.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13	14.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.7	5.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Electrical Characteristics: ADS7950, ADS7951, ADS7952, ADS7953

VA = 2.7 V to 5.25 V, VBD = 1.7 V to +VA, V_{REF} = 2.5 V ± 0.1 V, T_A = –40°C to 125°C, f_{sample} = 1 MHz (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT					
Full-scale input span(1)	Range 1	0		V_{REF}	V
	Range 2 while 2xV_{REF} ≤ +VA	0		2*V_{REF}	
Absolute input range	Range 1	–0.2		V_{REF} + 0.2	V
	Range 2 while 2xV_{REF} ≤ +VA	–0.2		2*V_{REF} + 0.2	
Input capacitance			15		pF
Input leakage current	T_A = 125°C		61		nA
SYSTEM PERFORMANCE					
Resolution			12		Bits
No missing codes	ADS795XSB(2)	12			Bits
	ADS795XS(2)	11			
Integral linearity	ADS795XSB(2)	–1	±0.5	1	LSB(3)
	ADS795XS(2)	–1.5	±0.75	1.5	
Differential linearity	ADS795XSB(2)	–0.99	±0.5	1	LSB
	ADS795XS(2)	–2	±0.75	1.5	
Offset error(4)		–3.5	±1.1	3.5	LSB
Gain error	Range 1	–2	±0.2	2	LSB
	Range 2		±0.2		
Total unadjusted error (TUE)			±2		LSB
SAMPLING DYNAMICS					
Conversion time	20 MHz SCLK			800	ns
Acquisition time		325			ns
Maximum throughput rate	20 MHz SCLK			1	MHz
Aperture delay			5		ns
Step response			150		ns
Overvoltage recovery			150		ns

(1) Ideal input span; does not include gain or offset error.
(2) ADS795X, where X indicates 0, 1, 2, or 3.
(3) LSB means least significant bit.
(4) Measured relative to an ideal full-scale input.

Electrical Characteristics: ADS7950, ADS7951, ADS7952, ADS7953 (continued)

VA = 2.7 V to 5.25 V, VBD = 1.7 V to +VA, V_{REF} = 2.5 V ± 0.1 V, T_A = –40°C to 125°C, f_{sample} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS						
Total harmonic distortion(5)		100 kHz		–82		dB
Signal-to-noise ratio		100 kHz, ADS795XSB(2)	70	71.7		dB
		100 kHz, ADS795XS(2)	70	71.7		
Signal-to-noise + distortion		100 kHz, ADS795XSB(2)	69	71.3		dB
		100 kHz, ADS795XS(2)	68	71.3		
Spurious free dynamic range		100 kHz		84		dB
Small signal bandwidth		At –3 dB		47		MHz
Channel-to-channel crosstalk		Any off-channel with 100 kHz, Full-scale input to channel being sampled with DC input (isolation crosstalk).		–95		dB
		From previously sampled to channel with 100 kHz, Full-scale input to channel being sampled with DC input (memory crosstalk).		–85		
EXTERNAL REFERENCE INPUT						
V_{REF} reference voltage at REFP(6)			2	2.5	3	V
Reference input resistance		At fsample = 1 MHz		100		kΩ
ALARM SETTING						
High threshold range			0		4092	LSB
Low threshold range			0		4092	LSB
DIGITAL INPUT/OUTPUT						
Logic family		CMOS				
Logic level	V_{IH}		0.7*(+VBD)			V
	V_{IL}	+VBD = 5 V			0.8	
	V_{IL}	+VBD = 3 V			0.4	
	V_{OH}	At I_{source} = 200 µA	+VBD-0.2			
	V_{OL}	At I_{sink} = 200 µA	0.4			
Data format MSB first			MSB First			
POWER SUPPLY REQUIREMENTS						
+VA supply voltage			2.7	3.3	5.25	V
+VBD supply voltage			1.7	3.3	5.25	V
Supply current (normal mode)		At +VA = 2.7 to 3.6 V and 1 MHz throughput		1.8		mA
		At +VA = 2.7 to 3.6 V static state		1.05		
		At +VA = 4.7 to 5.25 V and 1 MHz throughput		2.3	3	
		At +VA = 4.7 to 5.25 V static state		1.1	1.5	
Power-down state supply current				1		µA
+VBD supply current		+VA = 5.25 V, f_s = 1MHz		1		mA
Power-up time					1	µs
Invalid conversions after power up or reset					1	Conversion

(5) Calculated on the first nine harmonics of the input frequency.
(6) Device is designed to operate over V_{REF} = 2 V to 3 V. However one can expect lower noise performance at V_{ref} < 2.4 V. This is due to SNR degradation resulting from lowered signal range.

7.7 Electrical Characteristics, ADS7954, ADS7955, ADS7956, ADS7957

+VA = 2.7 V to 5.25 V, +VBD = 1.7 V to +VA, V_{REF} = 2.5 V ± 0.1 V, T_A = –40°C to 125°C, f_{sample} = 1 MHz (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT					
Full-scale input span(1)	Range 1	0		V_{REF}	V
	Range 2 while 2xV_{REF} ≤ +VA	0		2*V_{REF}	
Absolute input range	Range 1	–0.20		V_{REF} +0.20	V
	Range 2 while 2xV_{REF} ≤ +VA	–0.20		2*V_{REF} +0.20	
Input capacitance			15		pF
Input leakage current	T_A = 125°C		61		nA
SYSTEM PERFORMANCE					
Resolution			10		Bits
No missing codes		10			Bits
Integral linearity		–0.5	±0.2	0.5	LSB(2)
Differential linearity		–0.5	±0.2	0.5	LSB
Offset error(3)		–1.5	±0.5	1.5	LSB
Gain error	Range 1	–1	±0.1	1	LSB
	Range 2		±0.1		
SAMPLING DYNAMICS					
Conversion time	20 MHz SCLK			800	ns
Acquisition time		325			ns
Maximum throughput rate	20 MHz SCLK			1	MHz
Aperture delay			5		ns
Step response			150		ns
Overvoltage recovery			150		ns
DYNAMIC CHARACTERISTICS					
Total harmonic distortion(4)	100 kHz		–80		dB
Signal-to-noise ratio	100 kHz	60			dB
Signal-to-noise + distortion	100 kHz	60			
Spurious free dynamic range	100 kHz		82		dB
Full power bandwidth	At –3 dB		47		MHz
Channel-to-channel crosstalk	Any off-channel with 100 kHz, Full-scale input to channel being sampled with DC input.		–95		dB
	From previously sampled to channel with 100 kHz, Full-scale input to channel being sampled with DC input.		–85		
EXTERNAL REFERENCE INPUT					
V_{REF} reference voltage at REFP		2	2.5	3	V
Reference input resistance	fsample = 1 MHz		100		kΩ
ALARM SETTING					
High threshold range		000		4092	LSB
Low threshold range		000		4092	LSB

(1) Ideal input span; does not include gain or offset error.
(2) LSB means least significant bit.
(3) Measured relative to an ideal full-scale input.
(4) Calculated on the first nine harmonics of the input frequency.

Electrical Characteristics, ADS7954, ADS7955, ADS7956, ADS7957 (continued)

+VA = 2.7 V to 5.25 V, +VBD = 1.7 V to +VA, V_{REF} = 2.5 V ± 0.1 V, T_A = –40°C to 125°C, f_{sample} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT						
Logic family		CMOS				
Logic level	V_{IH}		0.7*(+VBD)			V
	V_{IL}	+VBD = 5 V			0.8	
	V_{IL}	+VBD = 3 V			0.4	
	V_{OH}	At I_{source} = 200 µA	+VBD-0.2			
	V_{OL}	At I_{sink} = 200 µA	0.4			
Data format MSB first				MSB First		
POWER SUPPLY REQUIREMENTS						
+VA supply voltage			2.7	3.3	5.25	V
+VBD supply voltage			1.7	3.3	5.25	V
Supply current (normal mode)		At +VA = 2.7 to 3.6 V and 1MHz throughput		1.8		mA
		At +VA = 2.7 to 3.6 V static state		1.05	1	
		At +VA = 4.7 to 5.25 V and 1 MHz throughput		2.3	3	
		At +VA = 4.7 to 5.25 V static state		1.1	1.5	
Power-down state supply current				1		µA
+VBD supply current		+VA = 5.25V, f_s = 1MHz		1		mA
Power-up time					1	µs
Invalid conversions after power up or reset					1	Conversion

7.8 Electrical Characteristics, ADS7958, ADS7959, ADS7960, ADS7961

+VA = 2.7 V to 5.25 V, +VBD = 1.7 V to +VA, V_{REF} = 2.5 V ± 0.1 V, T_A = –40°C to 125°C, f_{sample} = 1 MHz (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT					
Full-scale input span(1)	Range 1	0		V_{REF}	V
	Range 2 while 2xV_{REF} ≤ +VA	0		2*V_{REF}	
Absolute input range	Range 1	–0.20		V_{REF} + 0.2	V
	Range 2 while 2xV_{REF} ≤ +VA	–0.20		2*V_{REF} + 0.2	
Input capacitance			15		pF
Input leakage current	T_A = 125°C		61		nA
SYSTEM PERFORMANCE					
Resolution			8		Bits
No missing codes		8			Bits
Integral linearity		–0.3	±0.1	0.3	LSB(2)
Differential linearity		–0.3	±0.1	0.3	LSB
Offset error(3)		–0.5	±0.2	0.5	LSB
Gain error	Range 1	–0.6	±0.1	0.6	LSB
	Range 2		±0.1		

(1) Ideal input span; does not include gain or offset error.
(2) LSB means least significant bit.
(3) Measured relative to an ideal full-scale input.

Electrical Characteristics, ADS7958, ADS7959, ADS7960, ADS7961 (continued)

+VA = 2.7 V to 5.25 V, +VBD = 1.7 V to +VA, V_{REF} = 2.5 V ± 0.1 V, T_A = –40°C to 125°C, f_{sample} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SAMPLING DYNAMICS						
Conversion time		20 MHz SCLK			800	ns
Acquisition time			325			ns
Maximum throughput rate		20 MHz SCLK			1	MHz
Aperture delay				5		ns
Step response				150		ns
Overvoltage recovery				150		ns
DYNAMIC CHARACTERISTICS						
Total harmonic distortion(4)		100 kHz		–75		dB
Signal-to-noise ratio		100 kHz	49			dB
Signal-to-noise + distortion		100 kHz	49			
Spurious free dynamic range		100 kHz		–78		dB
Full power bandwidth		At –3 dB		47		MHz
Channel-to-channel crosstalk		Any off-channel with 100 kHz, Full-scale input to channel being sampled with DC input.		–95		dB
		From previously sampled to channel with 100 kHz, Full-scale input to channel being sampled with DC input.		–85		
EXTERNAL REFERENCE INPUT						
V_{REF} reference voltage at REFP			2	2.5	3	V
Reference input resistance		fsample = 1 MHz		100		kΩ
ALARM SETTING						
High threshold range			000		255	LSB
Low threshold range			000		255	LSB
DIGITAL INPUT/OUTPUT						
Logic family		CMOS				
Logic level	V_{IH}		0.7*(+VBD)			V
	V_{IL}	+VBD = 5 V			0.8	
	V_{IL}	+VBD = 3 V			0.4	
	V_{OH}	At I_{source} = 200 µA	+VBD-0.2			
	V_{OL}	At I_{sink} = 200 µA	0.4			
Data format			MSB First			
POWER SUPPLY REQUIREMENTS						
+VA supply voltage			2.7	3.3	5.25	V
+VBD supply voltage			1.7	3.3	5.25	V
Supply current (normal mode)		At +VA = 2.7 to 3.6 V and 1 MHz throughput		1.8		mA
		At +VA = 2.7 to 3.6 V static state		1.05		
		At +VA = 4.7 to 5.25 V and 1 MHz throughput		2.3	3	
		At +VA = 4.7 to 5.25 V static state		1.1	1.5	
Power-down state supply current				1		µA
+VBD supply current		+VA = 5.25V, f_s = 1MHz		1		mA
Power-up time					1	µs
Invalid conversions after power up or reset					1	Conversion

(4) Calculated on the first nine harmonics of the input frequency.

7.9 Timing Requirements

All specifications typical at –40°C to 125°C, +VA = 2.7 V to 5.25 V (unless otherwise specified)(1)(2) (see Figure 1, Figure 2, Figure 3, and Figure 4)

			MIN	NOM	MAX	UNIT
t_{conv}	Conversion time	+VBD = 1.8 V			16	SCLK
		+VBD = 3 V			16	
		+VBD = 5 V			16	
t_q	Minimum quiet sampling time needed from bus 3-state to start of next conversion	+VBD = 1.8 V	40			ns
		+VBD = 3 V	40			
		+VBD = 5 V	40			
t_{d1}	Delay time, $\overline{CS}$ low to first data (DO–15) out	+VBD = 1.8 V			38	ns
		+VBD = 3 V			27	
		+VBD = 5 V			17	
t_{su1}	Setup time, $\overline{CS}$ low to first rising edge of SCLK	+VBD = 1.8 V	8			ns
		+VBD = 3 V	6			
		+VBD = 5 V	4			
t_{d2}	Delay time, SCLK falling to SDO next data bit valid	+VBD = 1.8 V			35	ns
		+VBD = 3 V			27	
		+VBD = 5 V			17	
t_{h1}	Hold time, SCLK falling to SDO data bit valid	+VBD = 1.8 V	7			ns
		+VBD = 3 V	5			
		+VBD = 5 V	3			
t_{d3}	Delay time, 16th SCLK falling edge to SDO 3-state	+VBD = 1.8 V			26	ns
		+VBD = 3 V			22	
		+VBD = 5 V			13	
t_{su2}	Setup time, SDI valid to rising edge of SCLK	+VBD = 1.8 V	2			ns
		+VBD = 3 V	3			
		+VBD = 5 V	4			
t_{h2}	Hold time, rising edge of SCLK to SDI valid	+VBD = 1.8 V	12			ns
		+VBD = 3 V	10			
		+VBD = 5 V	6			
t_{w1}	Pulse duration $\overline{CS}$ high	+VBD = 1.8 V	20			ns
		+VBD = 3 V	20			
		+VBD = 5 V	20			
t_{d4}	Delay time $\overline{CS}$ high to SDO 3-state	+VBD = 1.8 V			24	ns
		+VBD = 3 V			21	
		+VBD = 5 V			12	
t_{wh}	Pulse duration SCLK high	+VBD = 1.8 V	20			ns
		+VBD = 3 V	20			
		+VBD = 5 V	20			
t_{wl}	Pulse duration SCLK low	+VBD = 1.8 V	20			ns
		+VBD = 3 V	20			
		+VBD = 5 V	20			
	Frequency SCLK	+VBD = 1.8 V			20	MHz
		+VBD = 3 V			20	
		+VBD = 5 V			20	

(1) 1.8V specifications apply from 1.7 V to 1.9 V, 3 V specifications apply from 2.7 V to 3.6 V, 5 V specifications apply from 4.75 V to 5.25 V.
(2) With 50-pF load

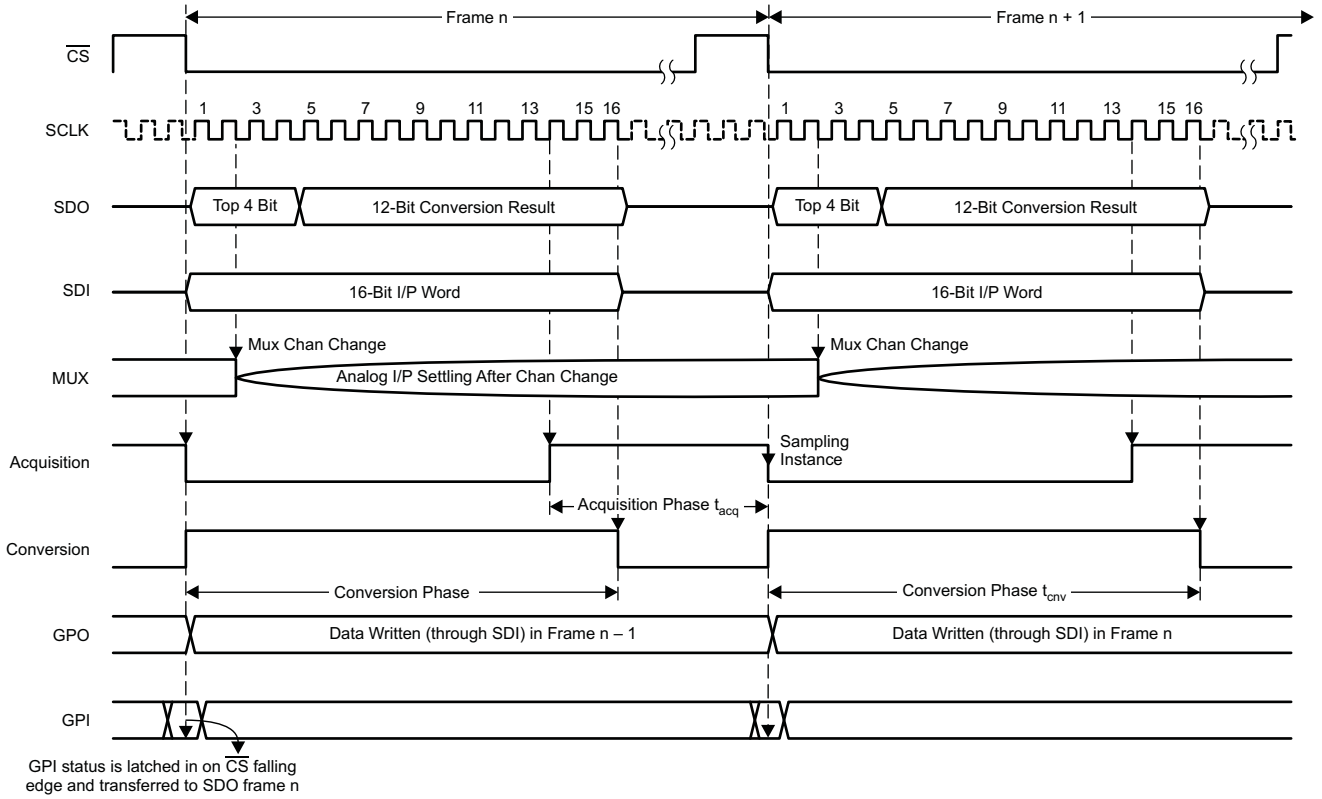


Figure 1. Device Operation Timing Diagram

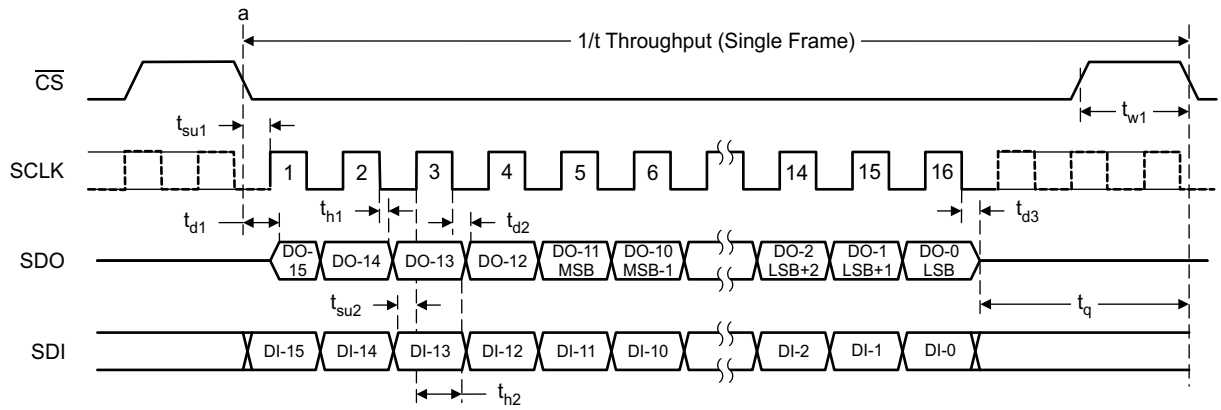


Figure 2. Serial Interface Timing Diagram for 12-Bit Devices (ADS7950/51/52/53)

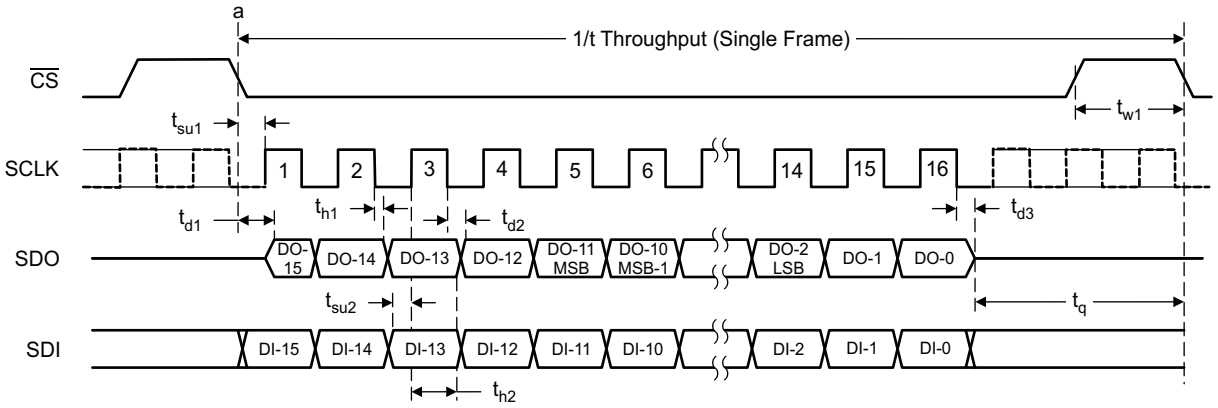


Figure 3. Serial Interface Timing Diagram for 10-Bit Devices (ADS7954/55/56/57)

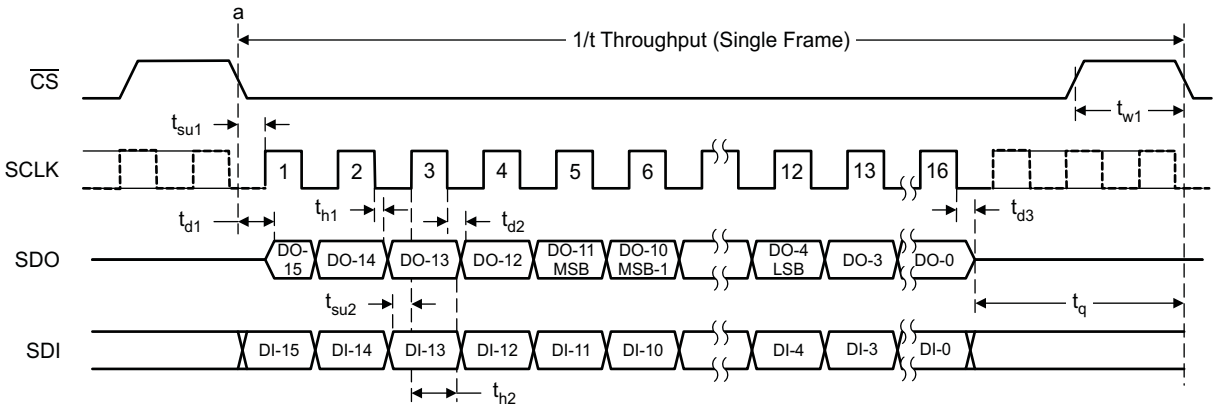


Figure 4. Serial Interface Timing Diagram for 8-Bit Devices (ADS7958/59/60/61)

7.10 Typical Characteristics (All ADS79xx Family Devices)

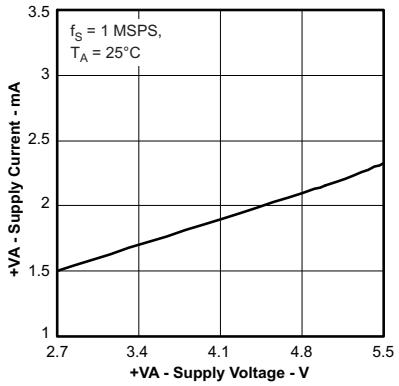


Figure 5. Supply Current vs Supply Voltage

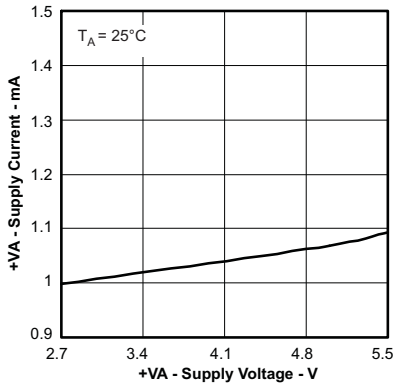


Figure 6. Static Supply Current vs Supply Voltage

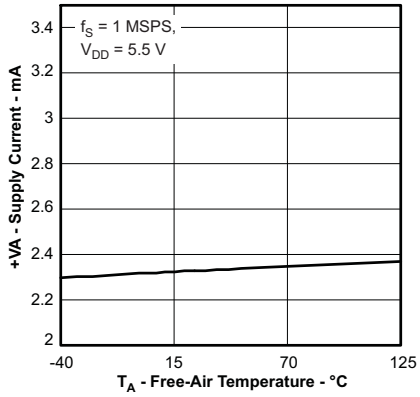


Figure 7. Supply Current vs Free-Air Temperature

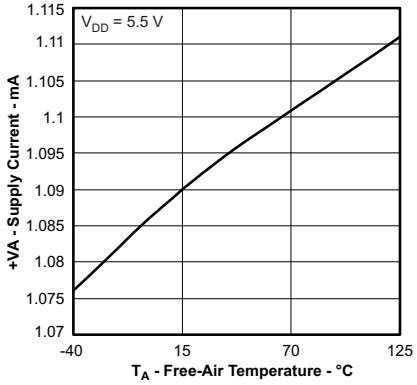


Figure 8. Static Supply Current vs Free-Air Temperature

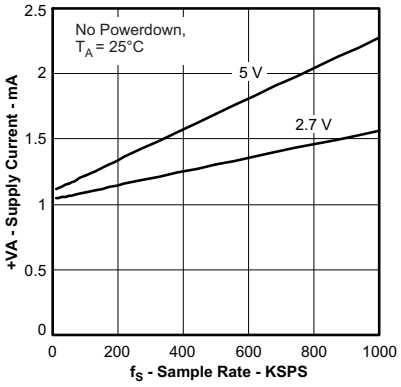


Figure 9. Supply Current vs Sample Rate

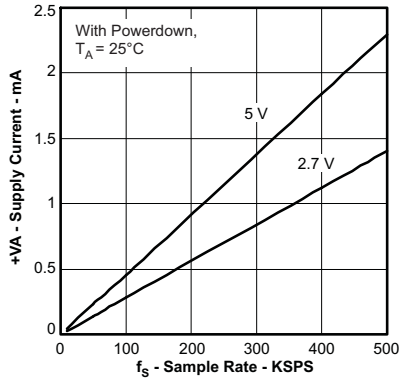


Figure 10. Supply Current vs Sample Rate

7.11 Typical Characteristics (12-Bit Devices Only)

Variations for 10-bit and 8-bit devices are too small to be illustrated through the characteristic curves

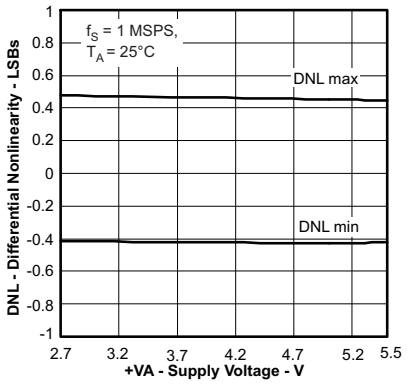


Figure 11. Differential Nonlinearity vs Supply Voltage

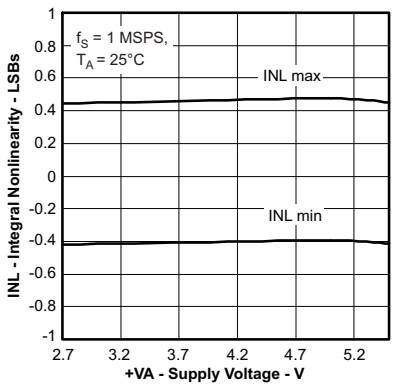


Figure 12. Integral Nonlinearity vs Supply Voltage

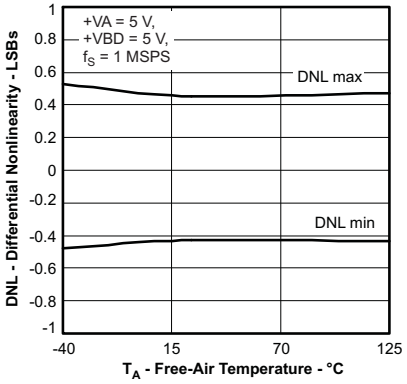


Figure 13. Differential Nonlinearity vs Free-Air Temperature

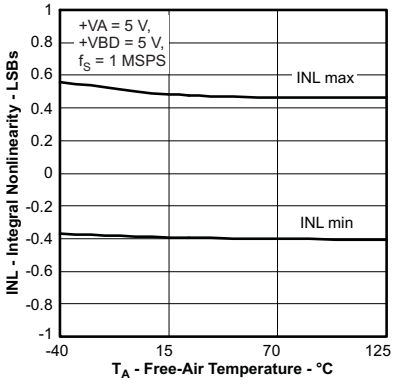


Figure 14. Integral Nonlinearity vs Free-Air Temperature

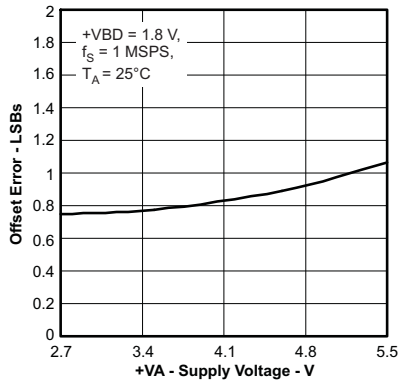


Figure 15. Offset Error vs Supply Voltage

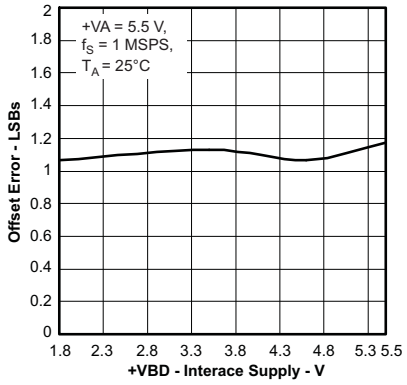


Figure 16. Offset Error vs Interface Supply Voltage

Typical Characteristics (12-Bit Devices Only) (continued)

Variations for 10-bit and 8-bit devices are too small to be illustrated through the characteristic curves

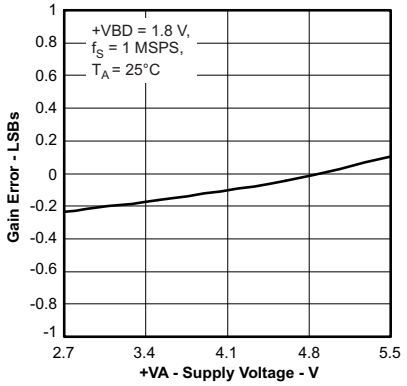


Figure 17. Gain Error vs Supply Voltage

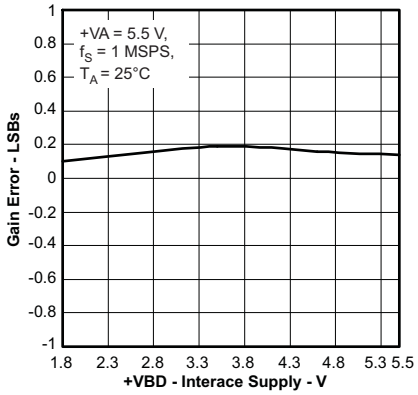


Figure 18. Gain Error vs Interface Supply Voltage

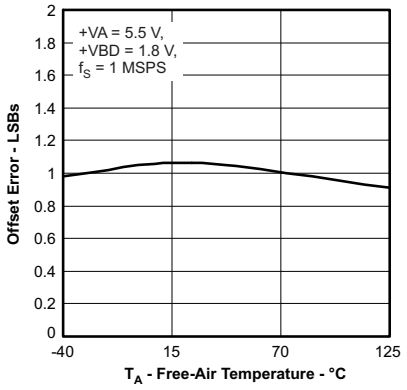


Figure 19. Offset Error vs Free-Air Temperature

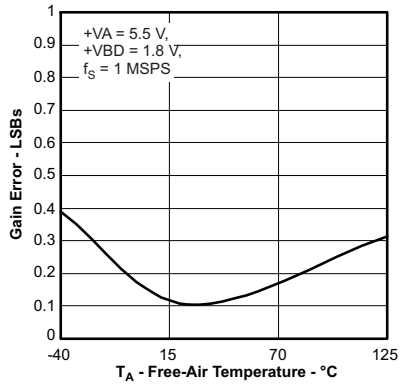


Figure 20. Gain Error vs Free-Air Temperature

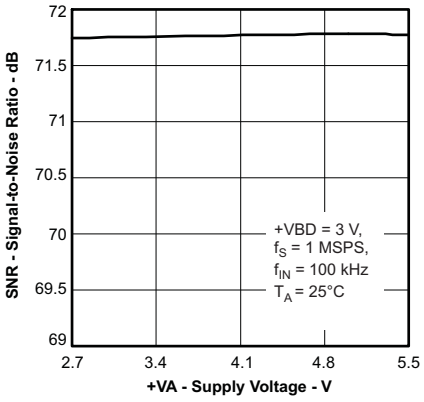


Figure 21. Signal-to-Noise Ratio vs Supply Voltage

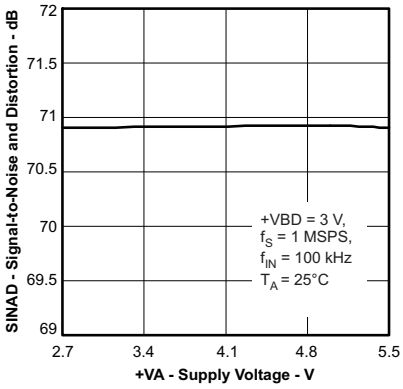


Figure 22. Signal-to-Noise + Distortion vs Supply Voltage

Typical Characteristics (12-Bit Devices Only) (continued)

Variations for 10-bit and 8-bit devices are too small to be illustrated through the characteristic curves

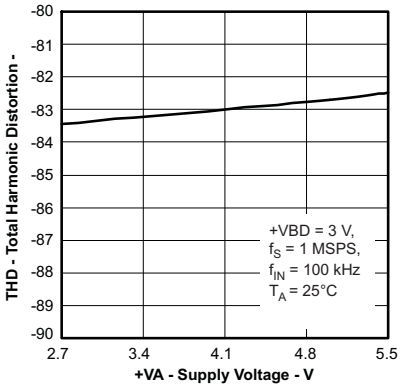


Figure 23. Total Harmonic Distortion vs Supply Voltage

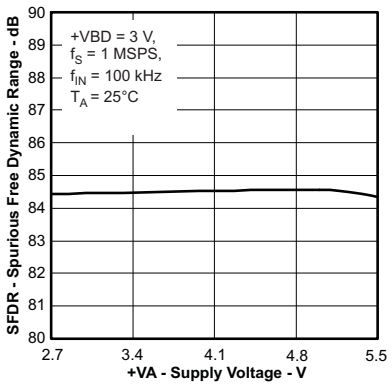


Figure 24. Spurious Free Dynamic Range vs Supply Voltage

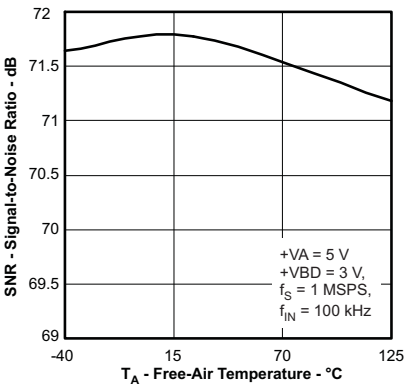


Figure 25. Signal-To-Noise Ratio vs Free-Air Temperature

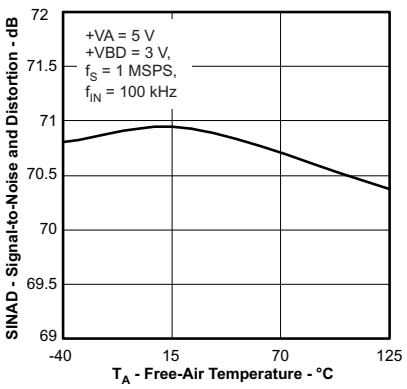


Figure 26. Signal-to-Noise + Distortion vs Free-Air Temperature

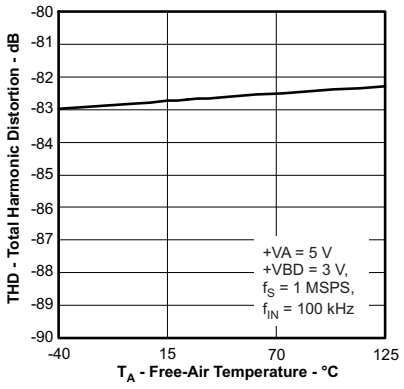


Figure 27. Total Harmonic Distortion vs Free-Air Temperature

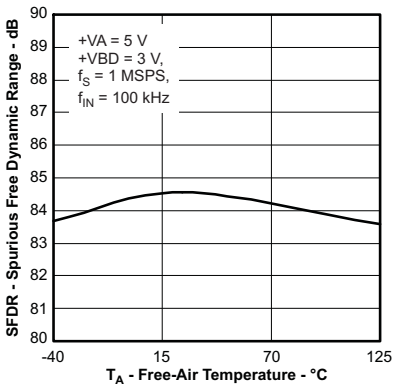


Figure 28. Spurious Free Dynamic Range vs Free-Air Temperature

Typical Characteristics (12-Bit Devices Only) (continued)

Variations for 10-bit and 8-bit devices are too small to be illustrated through the characteristic curves

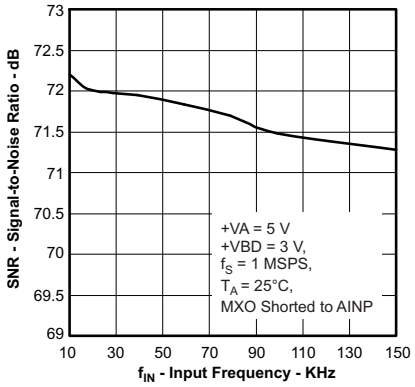


Figure 29. Signal-to-Noise Ratio vs Input Frequency

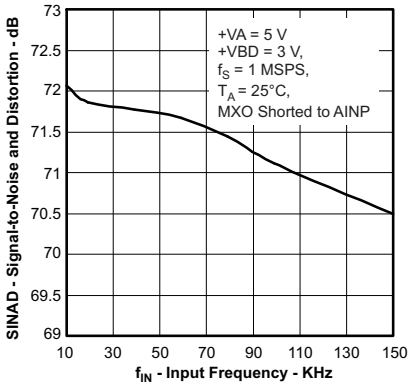


Figure 30. Signal-to-Noise + Distortion vs Input Frequency

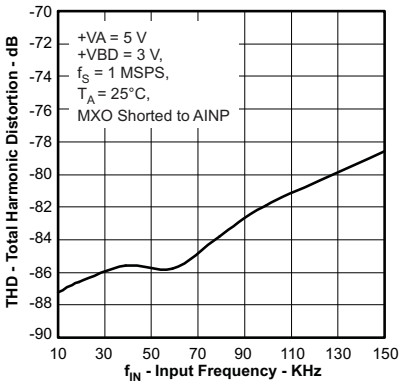


Figure 31. Total Harmonic Distortion vs Input Frequency

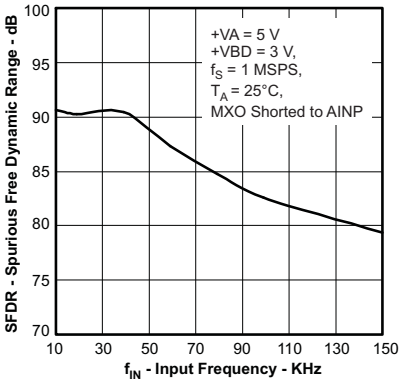


Figure 32. Spurious Free Dynamic Range vs Input Frequency

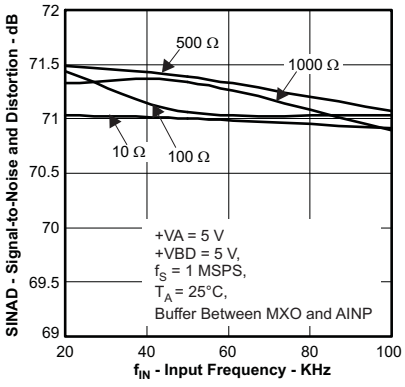


Figure 33. Signal-to-Noise + Distortion vs Input Frequency (Across Different Source Resistance Values)

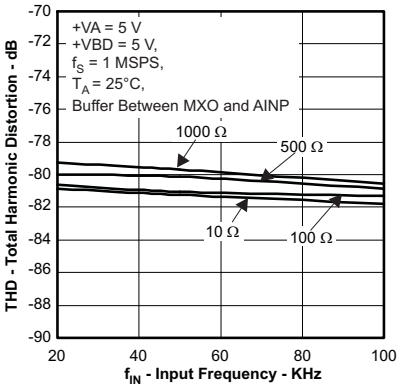


Figure 34. Total Harmonic Distortion vs Input Frequency (Across Different Source Resistance Values)

Typical Characteristics (12-Bit Devices Only) (continued)

Variations for 10-bit and 8-bit devices are too small to be illustrated through the characteristic curves

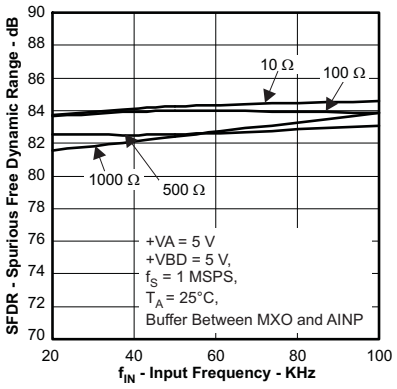


Figure 35. Spurious Free Dynamic Range vs Input Frequency (Across Different Source Resistance Values)

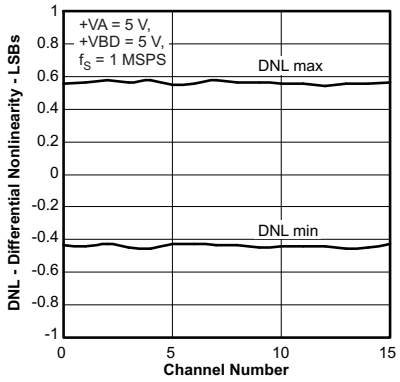


Figure 36. Differential Nonlinearity Variation Across Channels

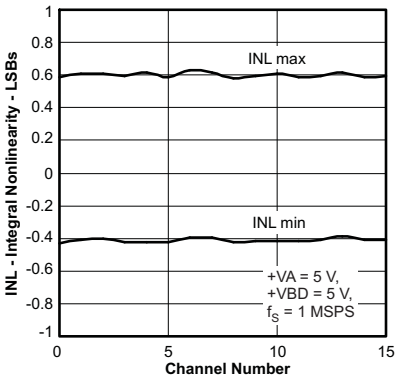


Figure 37. Integral Nonlinearity Variation Across Channels

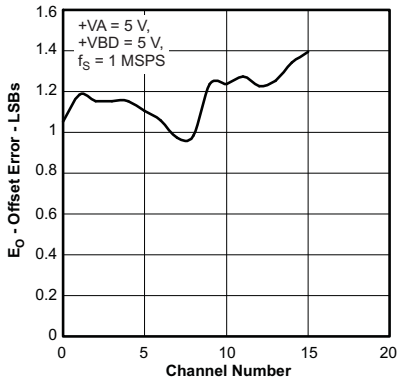


Figure 38. Offset Error Variation Across Channels

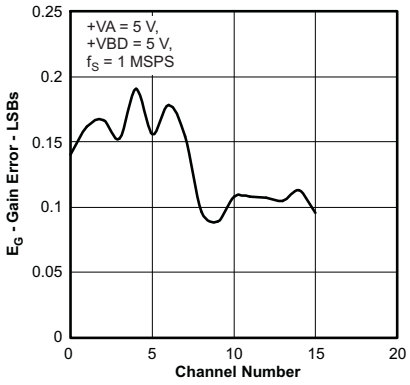


Figure 39. Gain Error Variation Across Channels

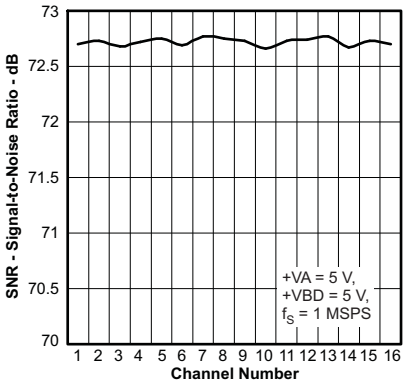


Figure 40. Signal-to-Noise Ratio Variation Across Channels

Typical Characteristics (12-Bit Devices Only) (continued)

Variations for 10-bit and 8-bit devices are too small to be illustrated through the characteristic curves

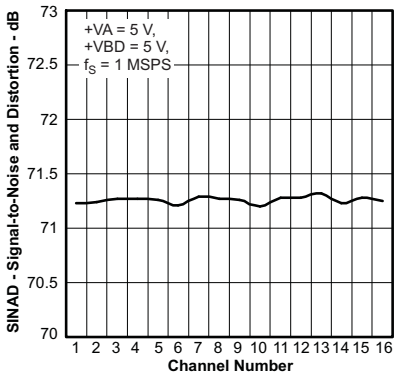


Figure 41. Signal-to-Noise + Distortion Variation Across Channels

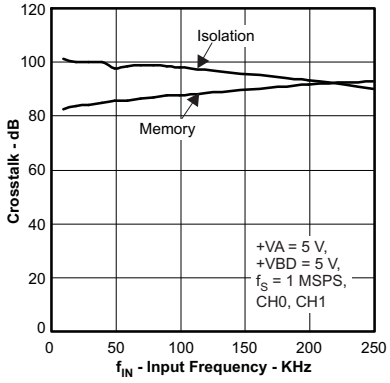


Figure 42. Crosstalk vs Input Frequency

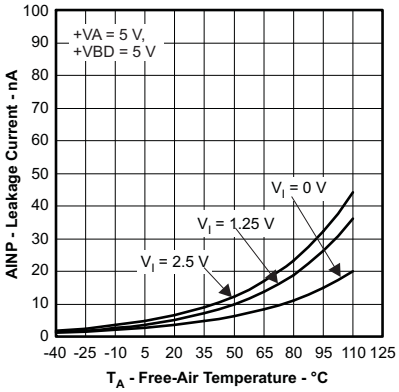


Figure 43. Input Leakage Current vs Free-Air Temperature

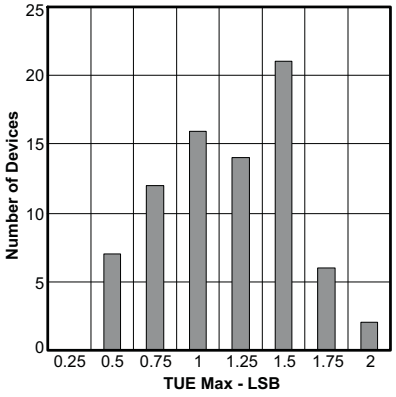


Figure 44. Total Unadjusted Error (TUE Maximum)

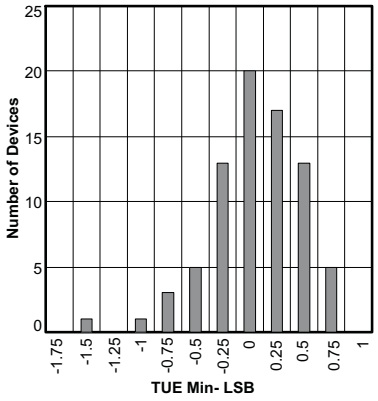


Figure 45. Total Unadjusted Error (TUE Minimum)

7.12 Typical Characteristics (12-Bit Devices Only)

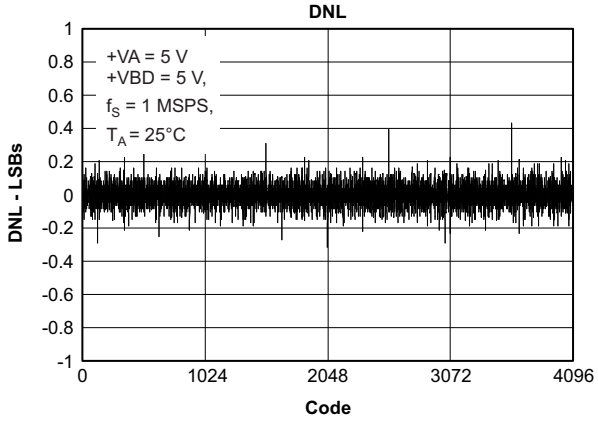


Figure 46. Typical DNL for All Codes

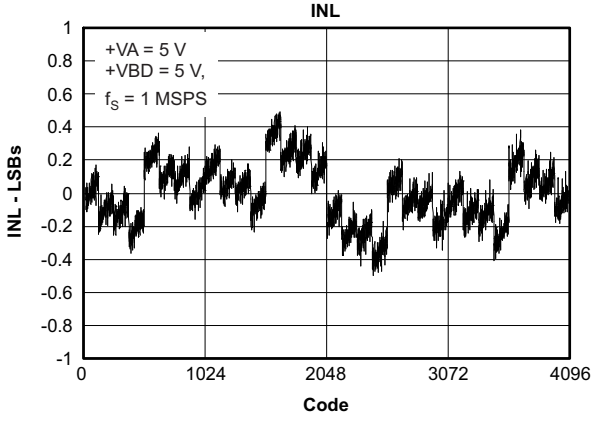


Figure 47. Typical INL for All Codes

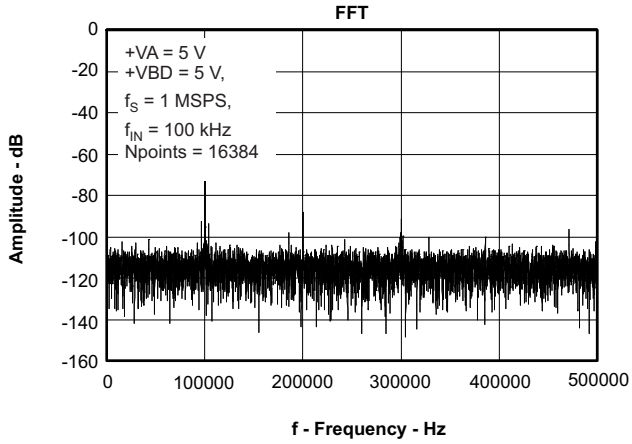


Figure 48. Typical FFT Plot

8 Detailed Description

8.1 Overview

The ADS7950 to ADS7961 are 12-, 10-, 8-bit multichannel pin-compatible devices. The ADS79xx is a family of 12-, 10-, 8-bit, high-speed, low-power, successive approximation register (SAR) analog-to-digital converter (ADC) that uses an external reference. The architecture is based on charge redistribution, which inherently includes a sample/hold function. The analog inputs to the ADS79xx are provided to CHX input channels. All input channels share a common analog ground AGND. ADS79xx has multiplexer breakout feature which allows user to connect the signal conditioning circuit between multiplexer output (MXO) and ADC input (AINP). This feature enables use of common signal conditioning block for the input signal which exhibit similar performance characteristics. ADS79xx can be programmed to select a channel manually or can be programmed into the auto channel select mode to sweep through the input channels automatically

Figure 1, Figure 2, Figure 3, and Figure 4 show device operation timing. Device operation is controlled with $\overline{CS}$, SCLK, and SDI. The device outputs its data on SDO.

Each frame begins with the falling edge of $\overline{CS}$. With the falling edge of $\overline{CS}$, the input signal from the selected channel is sampled, and the conversion process is initiated. The device outputs data while the conversion is in progress. The 16-bit data word contains a 4-bit channel address, followed by a 12-bit conversion result in MSB first format. There is an option to read the GPIO status instead of the channel address. (Refer to Table 1, Table 2, and Table 5 for more details.)

The device selects a new multiplexer channel on the second SCLK falling edge. The acquisition phase starts on the fourteenth SCLK rising edge. On the next $\overline{CS}$ falling edge the acquisition phase will end, and the device starts a new frame.

The TSSOP packaged devices have four *General Purpose IO* (GPIO) pins while QFN versions have only one GPIO. These four pins can be individually programmed as GPO or GPI. It is also possible to use them for preassigned functions, refer to Table 11. GPO data can be written into the device through the SDI line. The device refreshes the GPO data on the $\overline{CS}$ falling edge as per the SDI data written in previous frame.

Similarly the device latches GPI status on the $\overline{CS}$ falling edge and outputs the GPI data on the SDO line (if GPI read is enabled by writing DI04=1 in the previous frame) in the same frame starting with the $\overline{CS}$ falling edge.

The falling edge of $\overline{CS}$ clocks out DO15 (first bit of the four bit channel address), and remaining address bits are clocked out on every falling edge of SCLK until the third falling edge. The conversion result MSB is clocked out on the 4th SCLK falling edge and LSB on the 15th/13th/11th falling edge respectively for 12/10/8-bit devices. On the 16th falling edge of SCLK, SDO goes to the 3-state condition. The conversion ends on the 16th falling edge of SCLK. CS can be asserted (pulled high) only after 16 clocks have elapsed

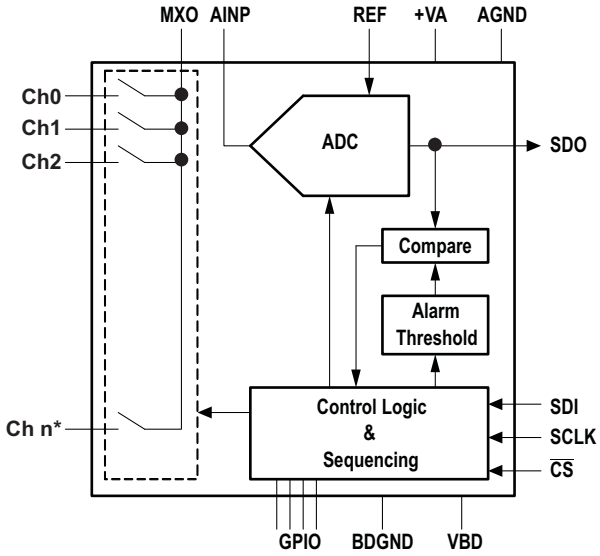
The device reads a sixteen bit word on the SDI pin while it outputs the data on the SDO pin. SDI data is latched on every rising edge of SCLK starting with the 1st clock as shown in Figure 2, Figure 3, and Figure 4.

$\overline{CS}$ can be asserted (pulled high) only after 16 clocks have elapsed.

The device has two (high and low) programmable alarm thresholds per channel. If the input crosses these limits; the device flags out an alarm on GPIO0/GPIO1 depending on the GPIO program register settings (refer to Table 11). The alarm is asserted (under the alarm conditions) on the 12th falling edge of SCLK in the same frame when a data conversion is in progress. The alarm output is reset on the 10th falling edge of SCLK in the next frame.

The device offers a power-down feature to save power when not in use. There are two ways to powerdown the device. It can be powered down by writing DI05 = 1 in the mode control register (refer to Table 1, Table 2, and Table 5); in this case the device powers down on the 16th falling edge of SCLK in the next data frame. Another way to powerdown the device is through GPIO in the case of the TSSOP packaged devices. GPIO3 can act as the $\overline{PD}$ input (refer to Table 11 to assign this functionality to GPIO3). This is an asynchronous and active low input. The device powers down instantaneously after GPIO3 ($\overline{PD}$) = 0. The device will power up again on the $\overline{CS}$ falling edge with DI05 = 0 in the mode control register and GPIO3 ($\overline{PD}$) = 1.

8.2 Functional Block Diagram



NOTE: n* is number of channels (16,12,8, or 4) depending on the device from the ADS79xx product family.

NOTE: There are 4 GPIOs in the TSSOP package and 1 GPIO in the QFN package..

8.3 Feature Description

8.3.1 Reference

The ADS79xx can operate with an external 2.5-V ± 10-mV reference. A clean, low noise, well-decoupled reference voltage on the REFP pin is required to ensure good performance of the converter. A low noise band-gap reference like the REF5025 can be used to drive this pin. A 10-µF ceramic decoupling capacitor is required between the REFP and REFM pins of the converter. The capacitor should be placed as close as possible to the pins of the device.

8.3.2 Power Saving

The ADS79xx devices offer a power-down feature to save power when not in use. There are two ways to power down the device. It can be powered down by writing DI05 = 1 in the Mode Control register (refer to Table 1, Table 2 and Table 5); in this case the device powers down on the 16th falling edge of SCLK in the next data frame. Another way to powerdown the device is through GPIO. GPIO3 can act as a $\overline{PD}$ input (refer to Table 11, for assigning this functionality to GPIO3). This is an asynchronous and active low input. The device powers down instantaneously after GPIO3 ($\overline{PD}$) = 0. The device will powerup again on the $\overline{CS}$ falling edge while DI05 = 0 in the Mode Control register and GPIO3 ($\overline{PD}$) = 1.

8.4 Device Functional Modes

8.4.1 Channel Sequencing Modes

There are three modes for channel sequencing, namely *Manual mode*, *Auto-1 mode*, *Auto-2 mode*. Mode selection is done by writing into the *Mode Control Register* (refer to Table 1, Table 2, and Table 5). A new multiplexer channel is selected on the second falling edge of SCLK (as shown in Figure 1) in all three modes.

Manual mode: When configured to operate in Manual mode, the next channel to be selected is programmed in each frame and the device selects the programmed channel in the next frame. On powerup or after reset the default channel is 'Channel-0' and the device is in Manual mode.

Auto-1 mode: In this mode the device scans pre-programmed channels in ascending order. A new multiplexer channel is selected every frame on the second falling edge of SCLK. There is a separate Program Register for pre-programming the channel sequence. Table 3 and Table 4 show Auto-1 ‘program register’ settings.

Device Functional Modes (continued)

Once programmed the device retains ‘Program Register settings until the device is powered down, reset, or reprogrammed. It is allowed to exit and re-enter the Auto-1 mode any number of times without disturbing ‘program register’ settings.

The Auto-1 program register is reset to FFFF/FFF/FF/F hex for the 16-, 12-, 8-, 4 channel devices respectively upon device powerup or reset; implying the device scans all channels in ascending order.

Auto-2 mode: In this mode the user can configure the program register to select the last channel in the scan sequence. The device scans all channels from channel 0 up to and including the last channel in ascending order. The multiplexer channel is selected every frame on the second falling edge of SCLK. There is a separate ‘program register’ for pre-programming of the last channel in the sequence (multiplexer depth). Table 6 lists the ‘Auto-2 prog’ register settings for selection of the last channel in the sequence.

Once programmed the device retains program register settings until the device is powered down, reset, or reprogrammed. It is allowed to exit and re-enter Auto-2 mode any number of times, without disturbing the ‘program register’ settings.

On powerup or reset the bits D9-D6 of the Auto-2 program register are reset to F/B/7/3 hex for the 16/12/8/4 channel devices respectively; implying the device scans all channels in ascending order.

8.4.2 Device Programming and Mode Control

The following section describes device programming and mode control. These devices feature two types of registers to configure and operate the devices in different modes. These registers are referred as ‘Configuration Registers’. There are two types of ‘Configuration Registers’ namely ‘Mode Control Registers’ and ‘Program Registers’.

8.4.2.1 Mode Control Register

A ‘Mode Control Register’ is configured to operate the device in one of three channel sequencing modes, namely Manual mode, Auto-1 Mode, Auto-2 Mode. It is also used to control user programmable features like range selection, device power-down control, GPIO read control, and writing output data into the GPIO.

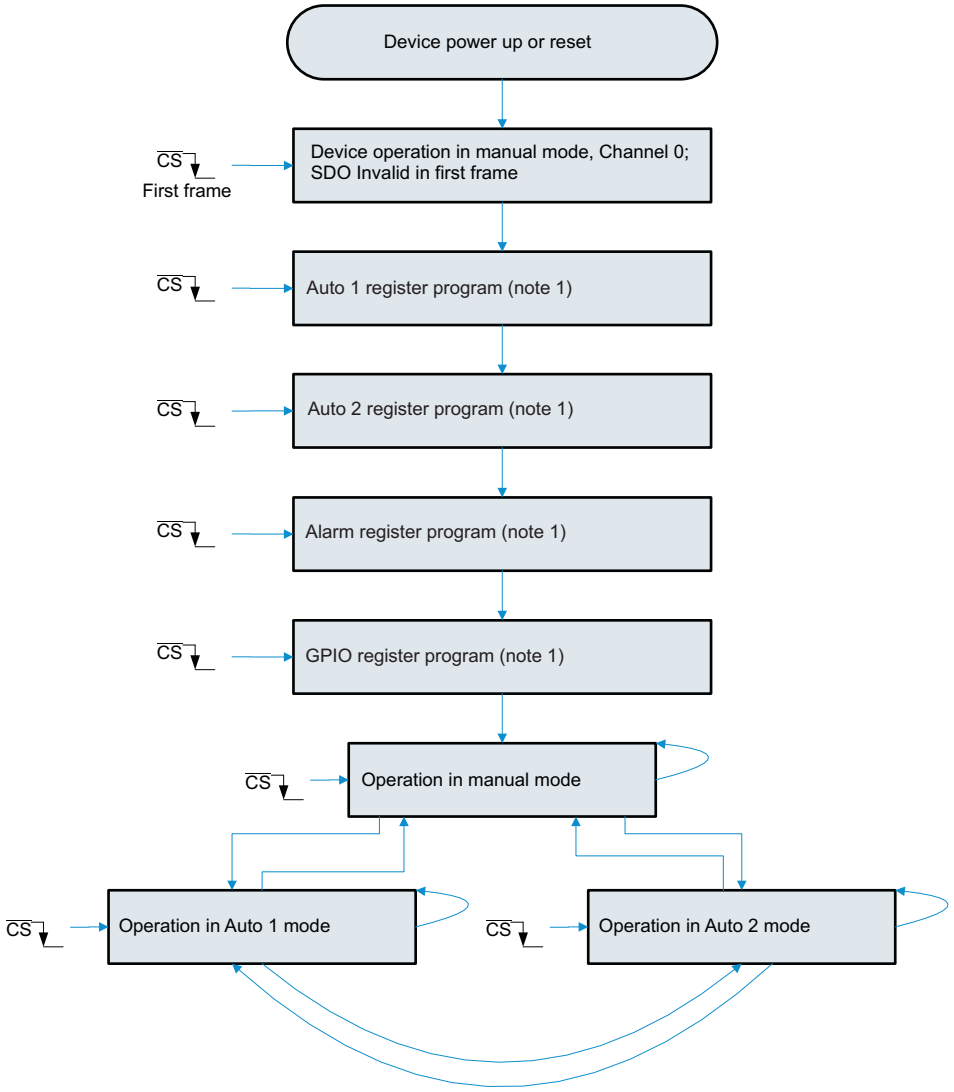
8.4.2.2 Program Registers

The 'Program Registers’ are used for device configuration settings and are typically programmed once on powerup or after device reset. There are different program registers such as ‘Auto-1 mode programming’ for pre-programming the channel sequence, ‘Auto-2 mode programming’ for selection of the last channel in the sequence, ‘Alarm programming’ for all 16 channels (or 12, 8, 4 channels depending on the device) and GPIO for individual pin configuration as GPI or GPO or a pre-assigned function.

8.4.3 Device Power-Up Sequence

The device power-up sequence is shown in Figure 49. By default, the Mode Control Register is configured for manual mode and the default channel is channel 0. As explained previously, these devices offer Program Registers to configure user programmable features like GPIOs, Alarms, and to pre-program the channel sequence for Auto modes. At ‘power up or on reset’ these registers are set to the default values listed in Table 1 to Table 11. On power up or after reset It is required to program Mode Control Register and Program Register to required mode of operation. Once configured; the device is ready to use in any of the three channel sequencing modes namely Manual, Auto-1, and Auto-2.

Device Functional Modes (continued)



(1) The device continues its operation in manual mode channel 0 throughout the programming sequence and outputs valid conversion results. It is possible to change channel, range, GPIO by inserting extra frames in between two programming blocks. It is also possible to bypass any programming block if the user does not intend to use that feature.

(2) It is possible to reprogram the device at any time during operation, regardless of what mode the device is in. During programming the device continues its operation in whatever mode it is in and outputs valid data.

Figure 49. Device Power-Up Sequence

8.4.4 Operating in Manual Mode

The flowchart in Figure 50 illustrates the steps involved in operating in manual channel sequencing mode. Table 1 lists the mode control register settings for manual mode. There are no program registers in manual mode.

Device Functional Modes (continued)

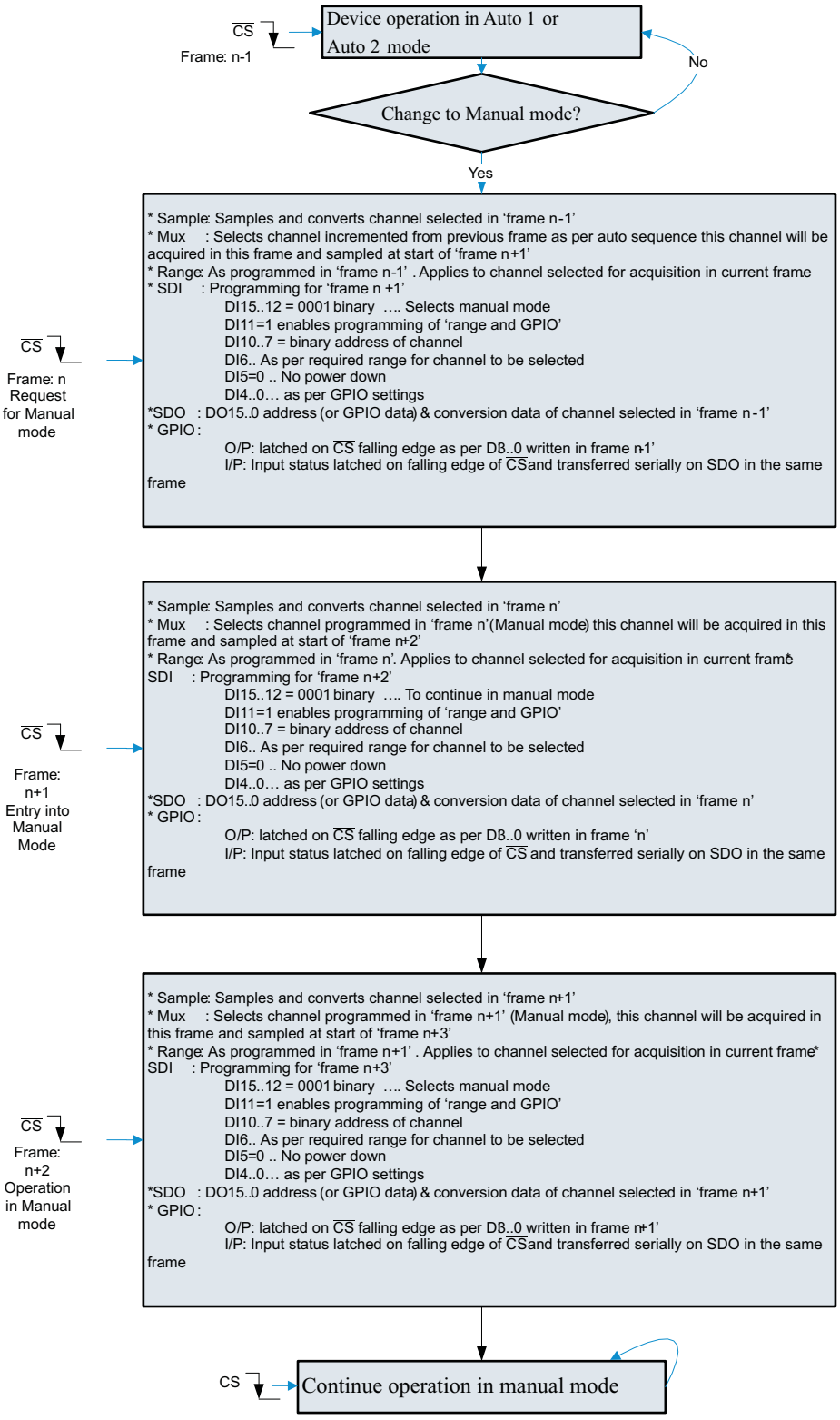


Figure 50. Entering and Running in Manual Channel Sequencing Mode

Device Functional Modes (continued)

Figure 51 shows an example in which manual mode is used to scan channels 4, 7, and 9. The command to select channel 4 (CH4) is issued in the Nth frame and the data corresponding to CH4 is available in the (N + 2)th frame. Internally, the SDI command is parsed and on the rising edge of $\overline{CS}$ of the (N+1)th frame and the MUX switches accordingly on the second falling edge of SCLK in this frame. On the rising edge of $\overline{CS}$ of the (N+2)th frame, the input signal for CH4 is sampled and the ADC sends the conversion data in this third frame. The device follows the same steps and the ADC sends the conversion data for CH7 and CH9 in the subsequent two frames.

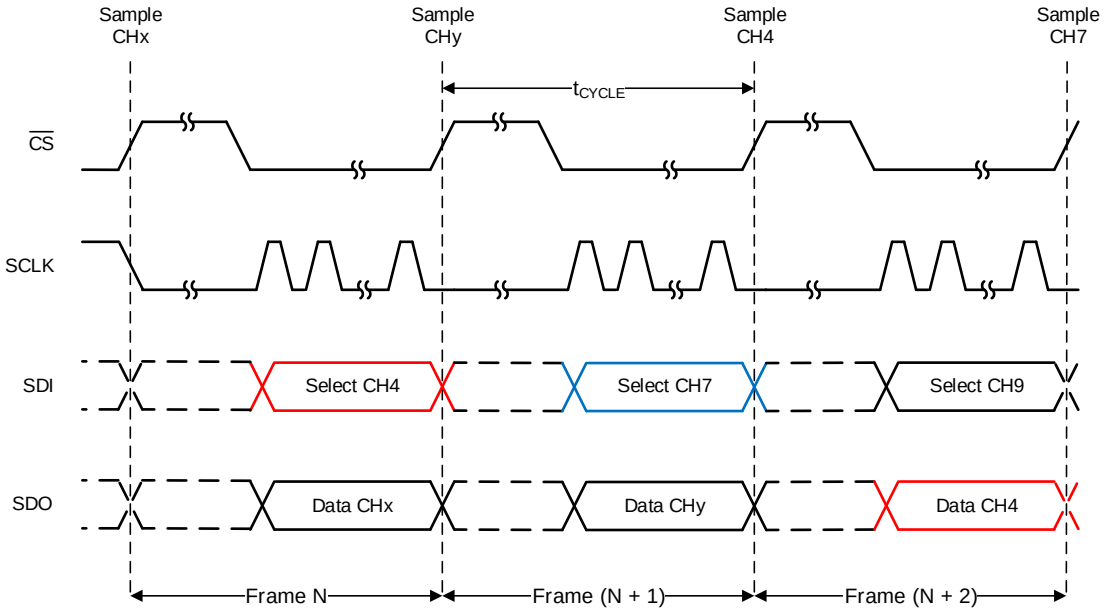


Figure 51. Example Manual Mode Timing Diagram

Table 1. Mode Control Register Settings for Manual Mode

BITS	RESET STATE	LOGIC STATE	FUNCTION			
DI15-12	0001	0001	Selects Manual Mode			
DI11	0	1	Enables programming of bits DI06-00.			
		0	Device retains values of DI06-00 from the previous frame.			
DI10-07	0000	This four bit data represents the address of the next channel to be selected in the next frame. DI10: MSB and DI07: LSB. For example, 0000 represents channel- 0, 0001 represents channel-1 and so forth.				
DI06	0	0	Selects 0 to V_{REF} input range (Range 1)			
		1	Selects 0 to $2xV_{REF}$ input range (Range 2)			
DI05	0	0	Device normal operation (no powerdown)			
		1	Device powers down on 16th SCLK falling edge			
DI04	0	0	SDO outputs current channel address of the channel on DO15..12 followed by 12 bit conversion result on DO11..00.			
		1	GPIO3-GPIO0 data (both input and output) is mapped onto DO15-DO12 in the order shown below. Lower data bits DO11-DO00 represent 12-bit conversion result of the current channel.			
			DOI5	DOI4	DOI3	DOI2
			GPIO3(1)	GPIO2(1)	GPIO1(1)	GPIO0(1)
DI03-00	0000	GPIO data for the channels configured as output. Device will ignore the data for the channel which is configured as input. SDI bit and corresponding GPIO information is given below				
			DI03	DI02	DI01	DI00
			GPIO3(1)	GPIO2(1)	GPIO1(1)	GPIO0(1)

(1) GPIO 1 to 3 are available only in TSSOP packaged devices. QFN device offers GPIO 0 only.

8.4.5 Operating in Auto-1 Mode

Figure 52 illustrates the steps involved in entering and operating in Auto-1 Channel Sequencing mode. Table 2 lists the Mode Control Register settings for Auto-1 mode.

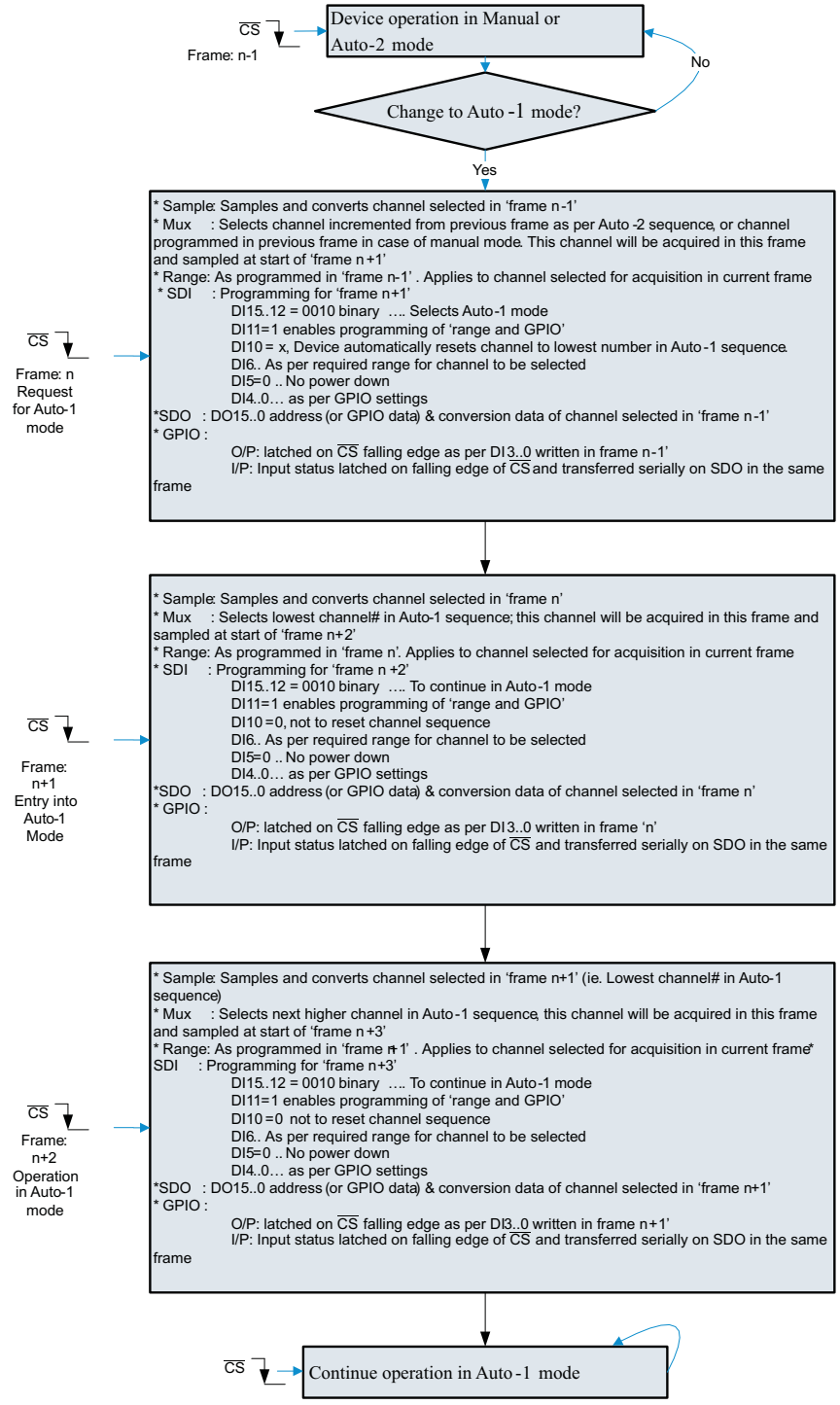


Figure 52. Entering and Running in Auto-1 Channel Sequencing Mode

Consider a case where Auto-1 mode is selected to scan channels 2 (CH2), 5 (CH5), and 6 (CH6) as represented in Figure 53. The program register for Auto-1 mode must be programmed as described in Figure 53 before entering into this auto sequencing mode. The device enters into Auto-1 mode on receiving the Auto-1 mode command in the Nth frame. This step causes the device to find the first enabled channel in ascending order and switch the MUX for CH2 in the (N+1)th frame. In the (N+2)th frame, the ADC samples the signal on CH2, shifts out the conversion results, and the MUX also internally switches to CH5. In the (N+3)th frame, the ADC samples and shifts out the conversion result for CH5 and the MUX also internally switches to CH6. This process repeats until the last enabled channel is reached, in which case the process loops back to the first enabled channel. Entering Auto-1 mode from any other mode also causes the device to restart from the first enabled channel. However, modifying the contents of the Auto-1 mode program register while operating in Auto-1 mode causes the device to scan for the next enabled channel.

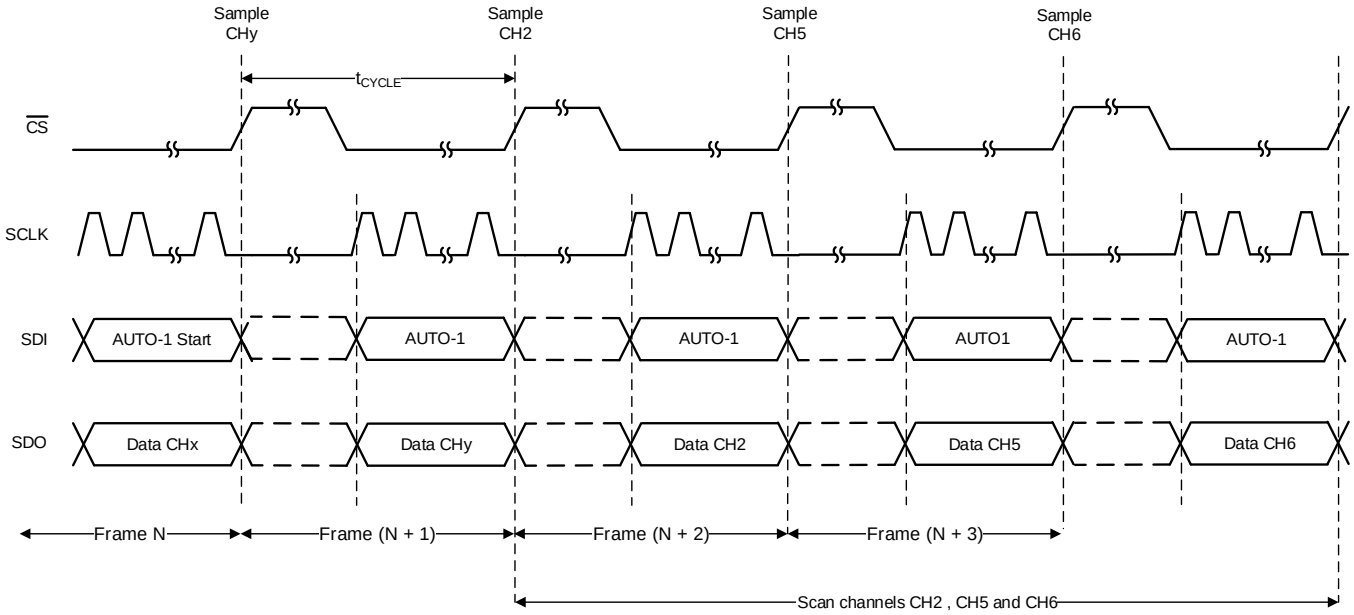


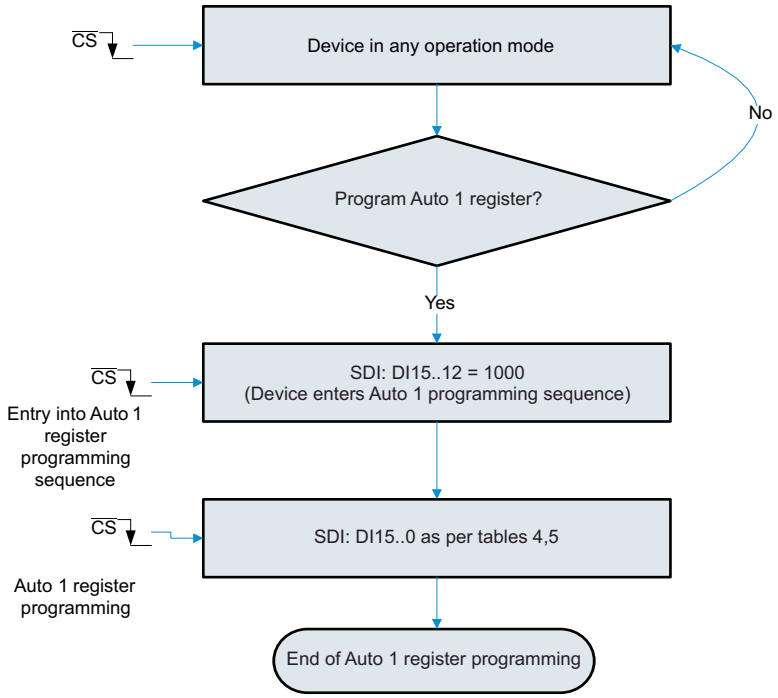
Figure 53. Example Auto-1 Mode Timing Diagram

Table 2. Mode Control Register Settings for Auto-1 Mode

BITS	RESET STATE	LOGIC STATE	FUNCTION			
DI15-12	0001	0010	Selects Auto-1 Mode			
DI11	0	1	Enables programming of bits DI10-00.			
		0	Device retains values of DI10-00 from previous frame.			
DI10	0	1	The channel counter is reset to the lowest programmed channel in the Auto-1 Program Register			
		0	The channel counter increments every conversion (No reset)			
DI09-07	000	xxx	Do not care			
DI06	0	0	Selects 0 to V_{REF} input range (Range 1)			
		1	Selects 0 to 2xV_{REF} input range (Range 2)			
DI05	0	0	Device normal operation (no powerdown)			
		1	Device powers down on the 16th SCLK falling edge			
DI04	0	0	SDO outputs current channel address of the channel on DO15..12 followed by 12-bit conversion result on DO11..00.			
		1	GPIO3-GPIO0 data (both input and output) is mapped onto DO15-DO12 in the order shown below. Lower data bits DO11-DO00 represent 12-bit conversion result of the current channel.			
			DO15	DO14	DO13	DO12
			GPIO3(1)	GPIO2(1)	GPIO1(1)	GPIO0(1)
DI03-00	0000	GPIO data for the channels configured as output. Device will ignore the data for the channel which is configured as input. SDI bit and corresponding GPIO information is given below				
			DI03	DI02	DI01	DI00
			GPIO3(1)	GPIO2(1)	GPIO1(1)	GPIO0(1)

(1) GPIO 1 to 3 are available only in TSSOP packaged devices. QFN device offers GPIO 0 only.

The Auto-1 Program Register is programmed (once on powerup or reset) to pre-select the channels for the Auto-1 sequence. Auto-1 Program Register programming requires two $\overline{CS}$ frames for complete programming. In the first $\overline{CS}$ frame the device enters the Auto-1 register programming sequence and in the second frame it programs the Auto-1 Program Register. Refer to Table 2, Table 3, and Table 4 for complete details.



NOTE: The device continues its operation in selected mode during programming. SDO is valid, however it is not possible to change the range or write GPIO data into the device during programming.

Figure 54. Auto-1 Register Programming Flowchart

Table 3. Program Register Settings for Auto-1 Mode

BITS	RESET STATE	LOGIC STATE	FUNCTION
FRAME 1			
DI15-12	NA	1000	Device enters Auto-1 program sequence. Device programming is done in the next frame.
DI11-00	NA	Do not care	
FRAME 2			
DI15-00	All 1s	1 (individual bit)	A particular channel is programmed to be selected in the channel scanning sequence. The channel numbers are mapped one-to-one with respect to the SDI bits; for example, DI15 → Ch15, DI14 → Ch14 … DI00 → Ch00
		0 (individual bit)	A particular channel is programmed to be skipped in the channel scanning sequence. The channel numbers are mapped one-to-one with respect to the SDI bits; for example DI15 → Ch15, DI14 → Ch14 … DI00 → Ch00

Table 4. Mapping of Channels to SDI Bits for 16, 12, 8, 4 Channel Devices

Device(1)	SDI BITS															
	DI15	DI14	DI13	DI12	DI11	DI10	DI09	DI08	DI07	DI06	DI05	DI04	DI03	DI02	DI01	DI00
16 Chan	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
12 Chan	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
8 Chan	X	X	X	X	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
4 Chan	X	X	X	X	X	X	X	X	X	X	X	X	1/0	1/0	1/0	1/0

(1) When operating in Auto-1 mode, the device only scans the channels programmed to be selected.

8.4.6 Operating in Auto-2 Mode

Figure 55 illustrates the steps involved in entering and operating in Auto-2 channel sequencing mode. Table 5 lists the mode control register settings for Auto-2 mode.

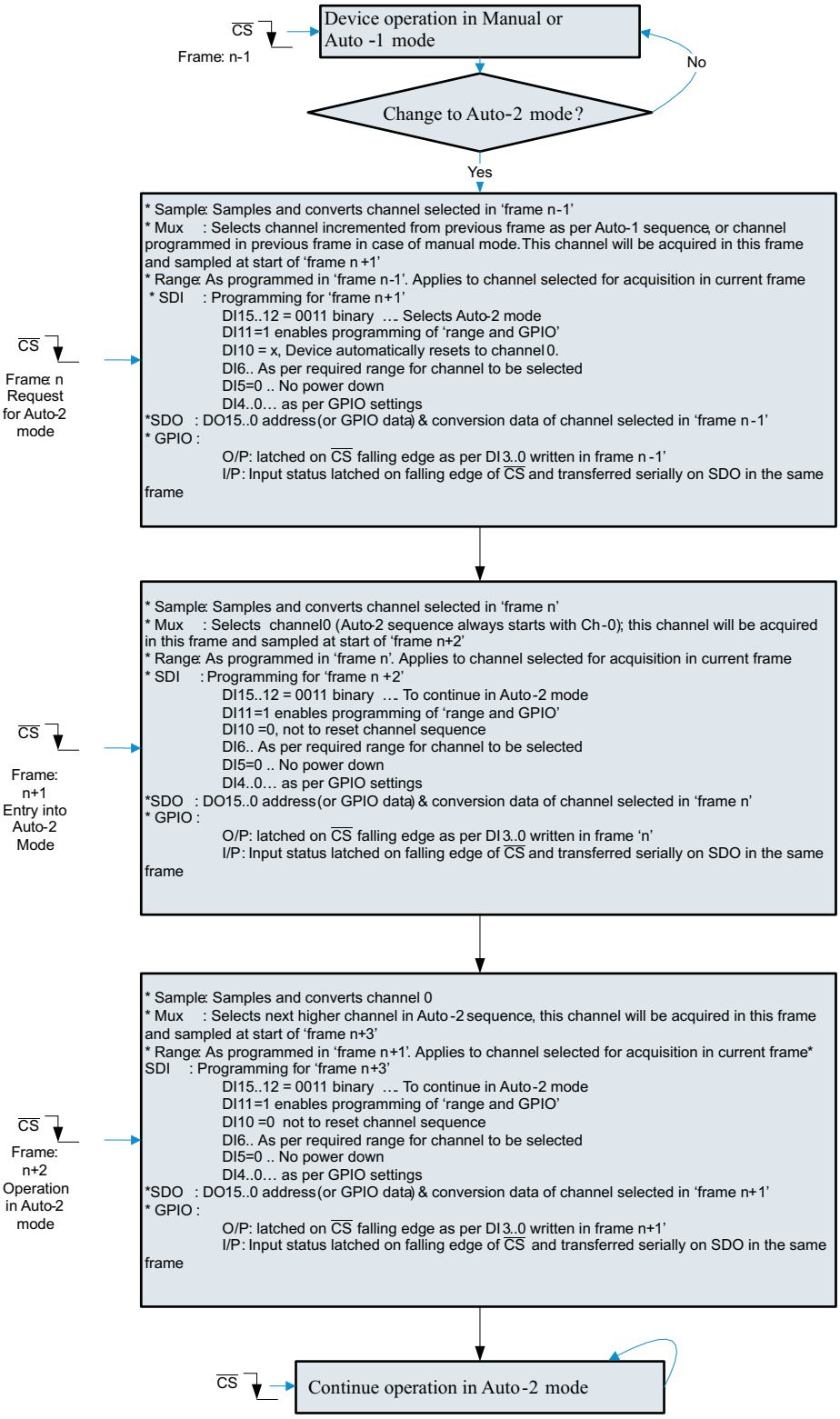


Figure 55. Entering and Running in Auto-2 Channel Sequencing Mode

Figure 56 shows an example in which Auto-2 mode is used to scan channels 0, 1, and 2. Auto-2 mode is selected to scan all channels until channel 2 (CH2) in ascending order by programming the Auto-2 register as described in Figure 56. The device enters Auto-2 mode on receiving the Auto-2 mode command in the Nth frame. This step causes the MUX to switch to CH0 in the (N+1)th frame. In the (N+2)th frame, the ADC samples and shifts out the conversion results for CH0 because the MUX internally switches to CH1. In the (N+3)th frame, the ADC samples and the shifts out the conversion result for CH1 and the MUX also switches to CH2, and so on. When this process reaches the maximum selected channel, CH2 in this case, the device returns to CH0 and repeats the cycle as long as the device remains in Auto-2 mode. Entering Auto-2 mode from any other mode also causes the device to restart from CH0. Additionally, modifying the contents of the for Auto-2 program register while operating in Auto-2 also causes the device to scan for restart from CH0.

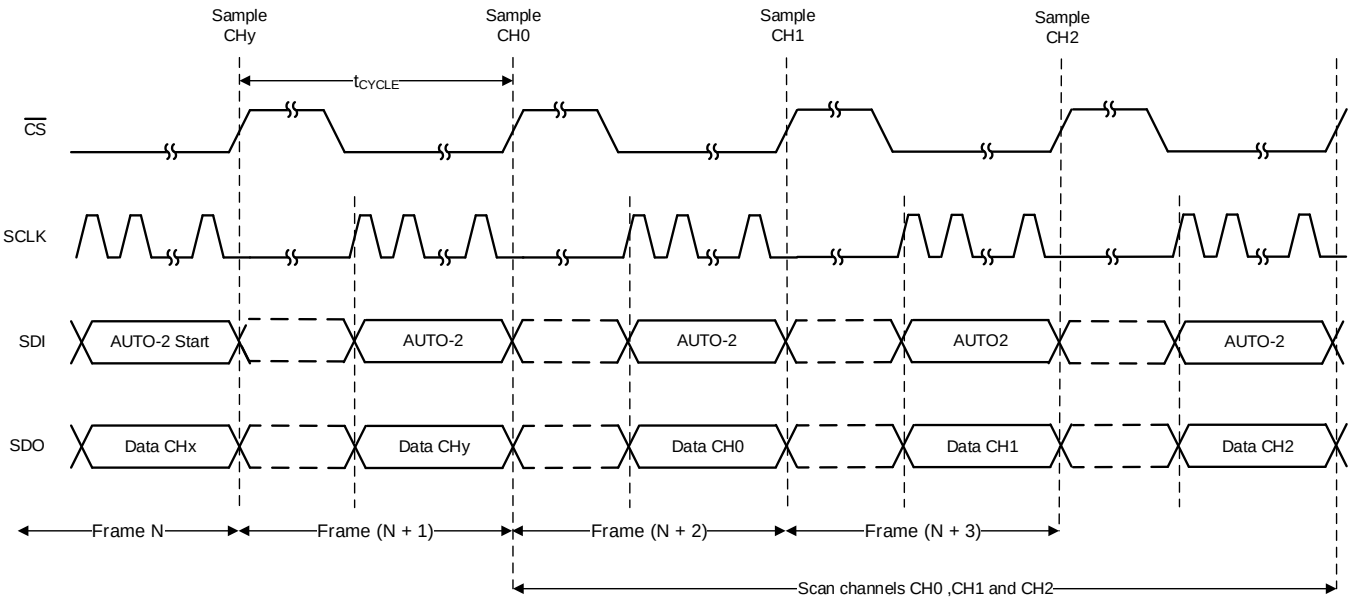


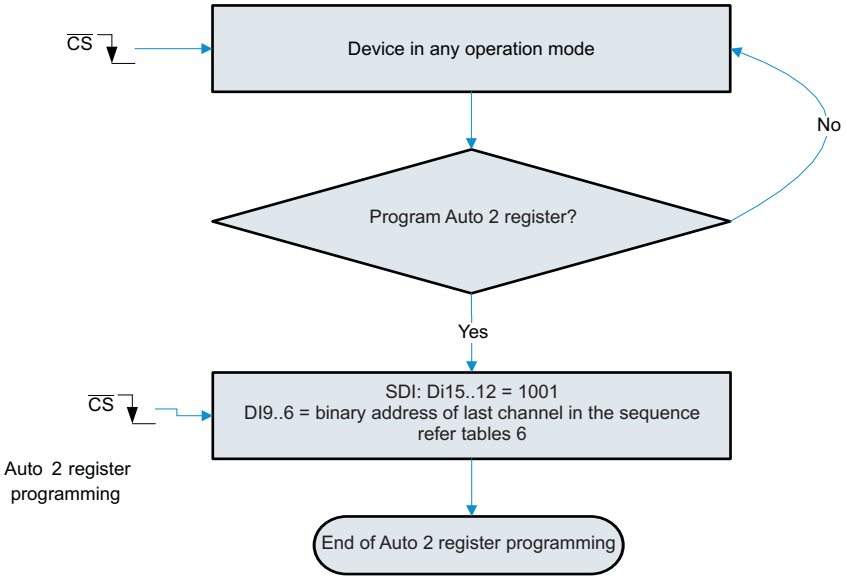
Figure 56. Example Auto-2 Mode Timing Diagram

Table 5. Mode Control Register Settings for Auto-2 Mode

BITS	RESET STATE	LOGIC STATE	FUNCTION			
DI15-12	0001	0011	Selects Auto-2 Mode			
DI11	0	1	Enables programming of bits DI10-00.			
		0	Device retains values of DI10-00 from the previous frame.			
DI10	0	1	Channel number is reset to Ch-00.			
		0	Channel counter increments every conversion.(No reset).			
DI09-07	000	xxx	Do not care			
DI06	0	0	Selects V_{REF} i/p range (Range 1)			
		1	Selects $2xV_{REF}$ i/p range (Range 2)			
DI05	0	0	Device normal operation (no powerdown)			
		1	Device powers down on the 16th SCLK falling edge			
DI04	0	0	SDO outputs the current channel address of the channel on DO15..12 followed by the 12-bit conversion result on DO11..00.			
		1	GPIO3-GPIO0 data (both input and output) is mapped onto DO15-DO12 in the order shown below. Lower data bits DO11-DO00 represent the 12-bit conversion result of the current channel.			
			DO15	DO14	DO13	DO12
			GPIO3(1)	GPIO2(1)	GPIO1(1)	GPIO0(1)
DI03-00	0000	GPIO data for the channels configured as output. Device ignores data for the channel which is configured as input. SDI bit and corresponding GPIO information is given below				
			DI03	DI02	DI01	DI00
			GPIO3(1)	GPIO2(1)	GPIO1(1)	GPIO0(1)

(1) GPIO 1 to 3 are available only in TSSOP packaged devices. QFN device offers GPIO 0 only.

The Auto-2 Program Register is programmed (once on powerup or reset) to pre-select the last channel (or sequence depth) in the Auto-2 sequence. Unlike Auto-1 Program Register programming, Auto-2 Program Register programming requires only 1 $\overline{CS}$ frame for complete programming. See Figure 57 and Table 6 for complete details.



NOTE: The device continues its operation in the selected mode during programming. SDO is valid, however it is not possible to change the range or write GPIO data into the device during programming.

Figure 57. Auto-2 Register Programming Flowchart

Table 6. Program Register Settings for Auto-2 Mode

BITS	RESET STATE	LOGIC STATE	FUNCTION
DI15-12	NA	1001	Auto-2 program register is selected for programming
DI11-10	NA	Do not care	
DI09-06	NA	aaaa	This 4-bit data represents the address of the last channel in the scanning sequence. During device operation in Auto-2 mode, the channel counter starts at CH-00 and increments every frame until it equals “aaaa”. The channel counter roles over to CH-00 in the next frame.
DI05-00	NA	Do not care	

8.4.7 Continued Operation in a Selected Mode

Once a device is programmed to operate in one of the modes, the user may want to continue operating in the same mode. Mode Control Register settings to continue operating in a selected mode are detailed in Table 7.

Table 7. Continued Operation in a Selected Mode

BITS	RESET STATE	LOGIC STATE	FUNCTION
DI15-12	0001	0000	The device continues to operate in the selected mode. In Auto-1 and Auto-2 modes the channel counter increments normally, whereas in the Manual mode it continues with the last selected channel. The device ignores data on DI11-DI00 and continues operating as per the previous settings. This feature is provided so that SDI can be held low when no changes are required in the Mode Control Register settings.
DI11-00	All '0'	Device ignores these bits when DI15-12 is set to 0000 logic state	

8.5 Programming

8.5.1 Digital Output

As discussed previously in *Overview*, the digital output of the ADS79xx devices is SPI compatible. The following tables list the output codes corresponding to various analog input voltages.

Table 8. Ideal Input Voltages for 12-Bit Devices and Output Codes for 12-Bit Devices (ADS7950/51/52/53)

DESCRIPTION		ANALOG VALUE	DIGITAL OUTPUT	
Full scale range	Range 1 → V_{REF}	Range 2 → 2×V_{REF}	STRAIGHT BINARY	
Least significant bit (LSB)	V_{REF} / 4096	2V_{REF} / 4096	BINARY CODE	HEX CODE
Full scale	V_{REF} – 1 LSB	2V_{REF} – 1 LSB	1111 1111 1111	FFF
Midscale	V_{REF} / 2	V_{REF}	1000 0000 0000	800
Midscale – 1 LSB	V_{REF} / 2 – 1 LSB	V_{REF} – 1 LSB	0111 1111 1111	7FF
Zero	0 V	0 V	0000 0000 0000	000

Table 9. Ideal Input Voltages for 10-Bit Devices and Digital Output Codes for 10-Bit Devices (ADS7954/55/56/57)

DESCRIPTION		ANALOG VALUE	DIGITAL OUTPUT	
Full scale range	Range 1 → V_{REF}	Range 2 → 2×V_{REF}	STRAIGHT BINARY	
Least significant bit (LSB)	V_{REF} / 1024	2V_{REF} / 1024	BINARY CODE	HEX CODE
Full scale	V_{REF} – 1 LSB	2V_{REF} – 1 LSB	0011 1111 1111	3FF
Midscale	V_{REF} / 2	V_{REF}	0010 0000 0000	200
Midscale – 1 LSB	V_{REF} / 2 – 1 LSB	V_{REF} – 1 LSB	0001 1111 1111	1FF
Zero	0 V	0 V	0000 0000 0000	000

Table 10. Ideal Input Voltages for 8-Bit Devices and Digital Output Codes for 8-Bit Devices (ADS7958/59/60/61)

DESCRIPTION		ANALOG VALUE	DIGITAL OUTPUT	
Full scale range	Range 1 → V_{REF}	Range 2 → 2×V_{REF}	STRAIGHT BINARY	
Least significant bit (LSB)	V_{REF} / 256	2V_{REF} / 256	BINARY CODE	HEX CODE
Full scale	V_{REF} – 1 LSB	2V_{REF} – 1 LSB	1111 1111	FF
Midscale	V_{REF} / 2	V_{REF}	1000 0000	80
Midscale – 1 LSB	V_{REF} / 2 – 1 LSB	V_{REF} – 1 LSB	0111 1111	7F
Zero	0 V	0 V	0000 0000	00

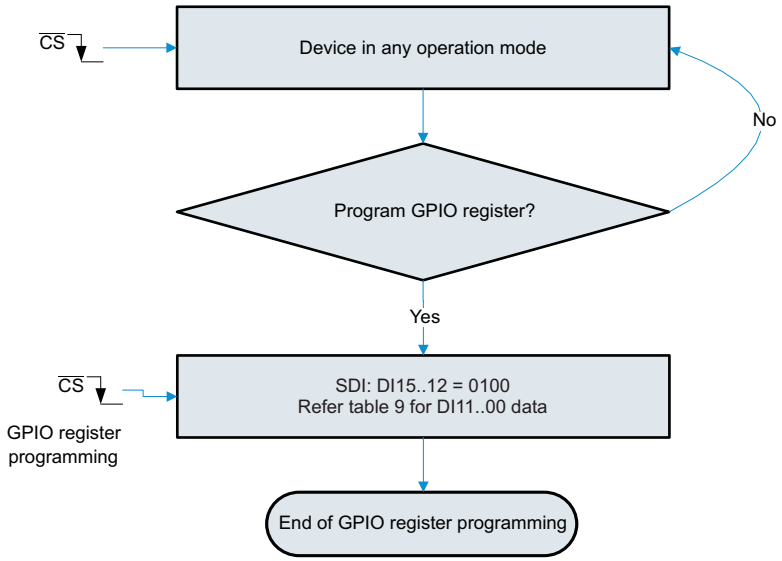
8.5.2 GPIO Registers

NOTE

GPIO 0, 1, 2, and 3 are available in the TSSOP packages. Only GPIO 0 is available in the VQFN packages.

The device has four general purpose input and output (GPIO) pins. Each of the four pins can be independently programmed as general purpose output (GPO) or general purpose input (GPI). It is also possible to use the GPIOs for some pre-assigned functions (refer to Table 11 for details). GPO data can be written into the device through the SDI line. The device refreshes the GPO data on every $\overline{CS}$ falling edge as per the SDI data written in the previous frame. Similarly, the device latches GPI status on the $\overline{CS}$ falling edge and outputs it on SDO (if GPI is read enabled by writing DI04 = 1 during the previous frame) in the same frame starting on the $\overline{CS}$ falling edge.

The details regarding programming the GPIO registers are illustrated in the flowchart in Figure 58. Table 11 lists the details regarding GPIO Register programming settings.



NOTE: The device continues its operation in selected mode during programming. SDO is valid, however it is not possible to change the range or write GPIO data into the device during programming.

Figure 58. GPIO Program Register Programming Flowchart

Table 11. GPIO Program Register Settings

BITS	RESET STATE	LOGIC STATE	FUNCTION
DI15-12	NA	0100	Device selects GPIO Program Registers for programming.
DI11-10	00	00	Do not program these bits to any logic state other than '00'
DI09	0	1	Device resets all registers in the next $\overline{CS}$ frame to the reset state shown in the corresponding tables (it also resets itself).
		0	Device normal operation
DI08	0	1	Device configures GPIO3 as the device power-down input.
		0	GPIO3 remains general purpose I or O. Program 0 for QFN packaged devices.
DI07	0	1	Device configures GPIO2 as device range input.
		0	GPIO2 remains general purpose I or O. Program 0 for QFN packaged devices.
DI06-04	000	000	GPIO1 and GPIO0 remain general purpose I or O. Valid setting for QFN packaged devices.
		xx1	Device configures GPIO0 as 'high or low' alarm output. This is an active high output. GPIO1 remains general purpose I or O. Valid setting for QFN packaged devices.
		010	Device configures GPIO0 as high alarm output. This is an active high output. GPIO1 remains general purpose I or O. Valid setting for QFN packaged devices.
		100	Device configures GPIO1 as low alarm output. This is an active high output. GPIO0 remains general purpose I or O. Setting not allowed for QFN packaged devices.
		110	Device configures GPIO1 as low alarm output and GPIO0 as a high alarm output. These are active high outputs. Setting not allowed for QFN packaged devices.
Note: The following settings are valid for GPIO which are not assigned a specific function through bits DI08..04			
DI03	0	1	GPIO3 pin is configured as general purpose output. Program 1 for QFN packaged devices.
		0	GPIO3 pin is configured as general purpose input. Setting not allowed for QFN packaged devices.
DI02	0	1	GPIO2 pin is configured as general purpose output. Program 1 for QFN packaged devices.
		0	GPIO2 pin is configured as general purpose input. Setting not allowed for QFN packaged devices.
DI01	0	1	GPIO1 pin is configured as general purpose output. Program 1 for QFN packaged devices.
		0	GPIO1 pin is configured as general purpose input. Setting not allowed for QFN packaged devices.
DI00	0	1	GPIO0 pin is configured as general purpose output. Valid setting for QFN packaged devices.
		0	GPIO0 pin is configured as general purpose input. Valid setting for QFN packaged devices.

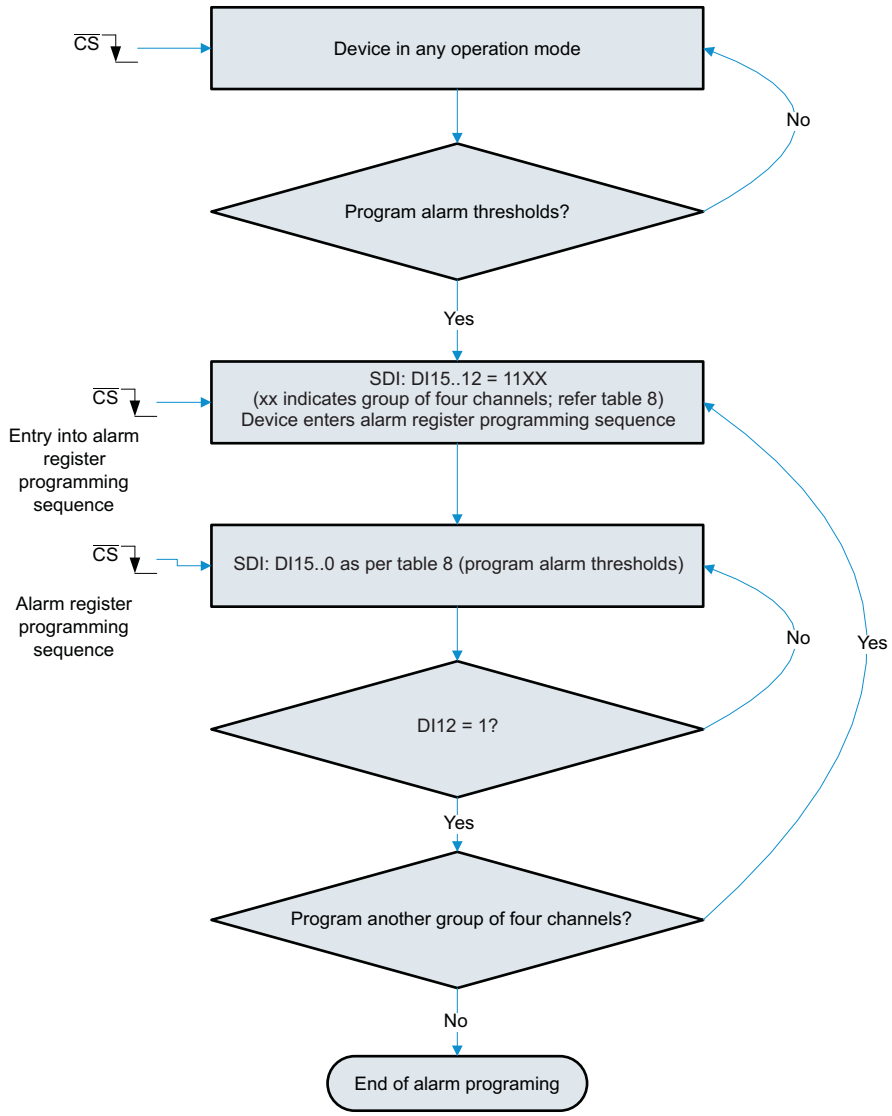
8.5.3 Alarm Thresholds for GPIO Pins

Each channel has two alarm program registers, one for setting the high alarm threshold and the other for setting the low alarm threshold. For ease of programming, two alarm programming registers per channel, corresponding to four consecutive channels, are assembled into one group (a total eight registers). There are four such groups for 16 channel devices and 3/2/1 such groups for 12/8/4 channel devices respectively. The grouping of the various channels for each device in the ADS79xx family is listed in Table 12. The details regarding programming the alarm thresholds are illustrated in the flowchart in Figure 59. Table 13 lists the details regarding the Alarm Program Register settings.

Table 12. Grouping of Alarm Program Registers

GROUP NO.	REGISTERS	APPLICABLE FOR DEVICE
0	High and low alarm for channel 0, 1, 2, and 3	ADS7953..50, ADS7957..54, ADS7961..58
1	High and low alarm for channel 4, 5, 6, and 7	ADS7953..51, ADS7957..55, ADS7961..59
2	High and low alarm for channel 8, 9, 10, and 11	ADS7953 and 52, ADS7957 and 56, ADS7961 and 60
3	High and low alarm for channel 12, 13, 14, and 15	ADS7953, ADS7957, ADS7961

Each alarm group requires 9 $\overline{CS}$ frames for programming their respective alarm thresholds. In the first frame the device enters the programming sequence and in each subsequent frame it programs one of the registers from the group. The device offers a feature to program less than eight registers in one programming sequence. The device exits the alarm threshold programming sequence in the next frame after it encounters the first 'Exit Alarm Program' bit high.



NOTE: The device continues its operation in selected mode during programming. SDO is valid, however it is not possible to change the range or write GPIO data into the device during programming.

Figure 59. Alarm Program Register Programming Flowchart

Table 13. Alarm Program Register Settings

BITS	RESET STATE	LOGIC STATE	FUNCTION
FRAME 1			
DI15-12	NA	1100	Device enters ‘alarm programming sequence’ for group 0
		1101	Device enters ‘alarm programming sequence’ for group 1
		1110	Device enters ‘alarm programming sequence’ for group 2
		1111	Device enters ‘alarm programming sequence’ for group 3
Note: DI15-12 = 11bb is the alarm programming request for group bb. Here ‘bb’ represents the alarm programming group number in binary format.			
DI11-14	NA	Do not care	
FRAME 2 AND ONWARDS			
DI15-14	NA	cc	Where “cc” represents the lower two bits of the channel number in binary format. The device programs the alarm for the channel represented by the binary number “bbcc”. “bb” is programmed in the first frame.
DI13	NA	1	High alarm register selection
		0	Low alarm register selection
DI12	NA	0	Continue alarm programming sequence in next frame
		1	Exit Alarm Programming in the next frame. Note: If the alarm programming sequence is not terminated using this feature then the device will remain in the alarm programming sequence state and all SDI data will be treated as alarm thresholds.
DI11-10	NA	xx	Do not care
DI09-00	All ones for high alarm register and all zeros for low alarm register	This 10-bit data represents the alarm threshold. The 10-bit alarm threshold is compared with the upper 10-bit word of the 12-bit conversion result. The device sets off an alarm when the conversion result is higher (High Alarm) or lower (Low Alarm) than this number. For 10-bit devices, all 10 bits of the conversion result are compared with the set threshold. For 8-bit devices, all 8 bits of the conversion result are compared with DI09 to DI02 and DI00, 01 are 'do not care'.	

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

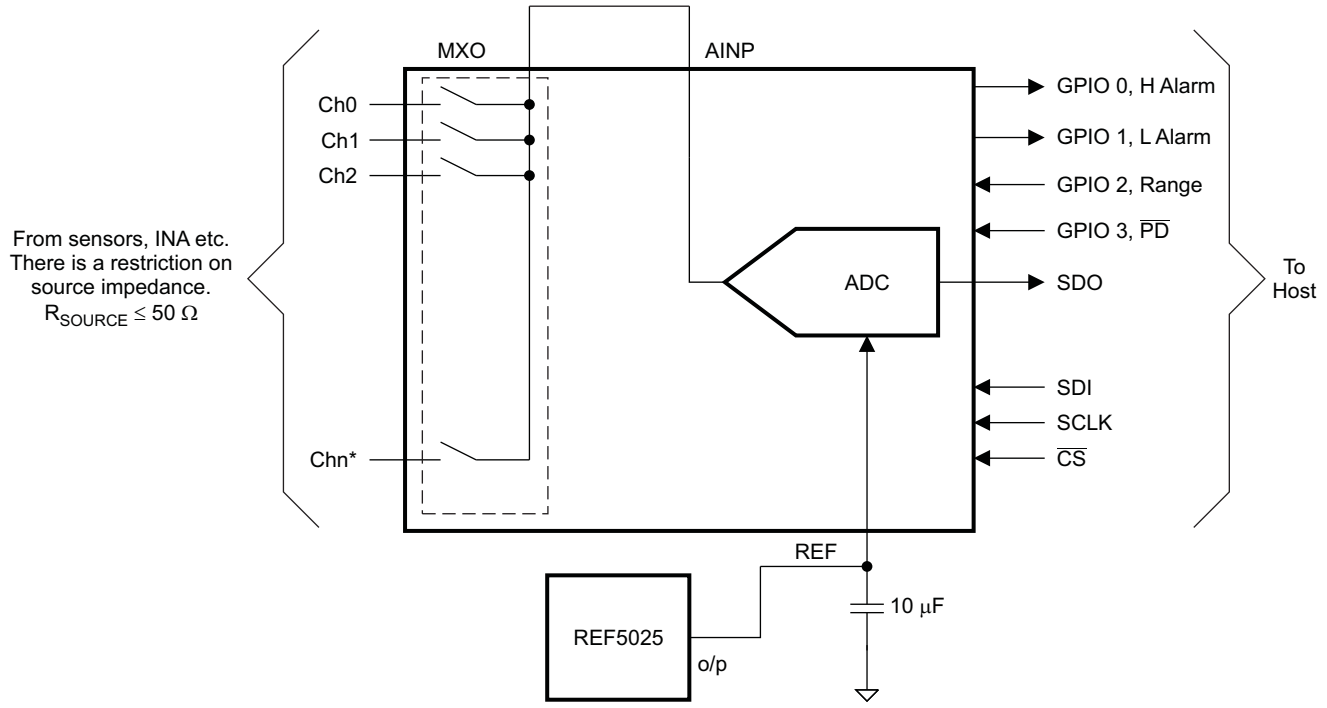
9.1 Application Information

In general applications, when the internal multiplexer is updated, the previously converted channel charge is stored in the 15-pF internal input capacitance that disturbs the voltage at the newly selected channel. This disturbance is expected to settle to 1 LSB during sampling (acquisition) time to avoid degrading converter performance. The initial absolute disturbance error at the channel input must be less than 0.5 V to prevent source current saturation or slewing that causes significantly long settling times. Fortunately, significantly reducing disturbance error is easy to accomplish by simply placing a large enough capacitor at the input of each channel. Specifically, with a 150-pF capacitor, instantaneous charge distribution keeps disturbance error less than 0.46 V because the internal input capacitance can only hold up to 75 pC (or 5 V × 15 pF). The remaining error must be corrected by the voltage source at each input, with impedance low enough to settle within 1 LSB. The following application examples explain the considerations for the input source impedance (R_{SOURCE}).

9.1.1 Analog Input

The ADS79xx device family offers 12/10/8-bit ADCSs with 16/12/8/4 channel multiplexers for analog input. The multiplexer output is available on the MXO pin. AINP is the ADC input pin. The devices offers flexibility for a system designer as both signals are accessible externally.

Typically it is convenient to short MXO to the AINP pin so that signal input to each multiplexer channel can be processed independently. In this condition, TI recommends limiting source impedance to 50 Ω or less. Higher source impedance may affect the signal settling time after a multiplexer channel change. This condition can affect linearity and total harmonic distortion.



GPIO 0,1,2 and 3 are available only in TSSOP packaged devices. QFN device offers 'GPIO 0' only. As a result all references related to 'GPIO 0' only are valid in case of QFN package devices.

Figure 60. Typical Application Diagram Showing MXO Shorted to AINP

Application Information (continued)

Another option is to add a common ADC driver buffer between the MXO and AINP pins. This relaxes the restriction on source impedance to a large extent. Refer to *Typical Characteristics (All ADS79xx Family Devices)* for the effect of source impedance on device performance. The typical characteristics show that the device has respectable performance with up to 1kΩ source impedance. This topology (including a common ADC driver) is useful when all channel signals are within the acceptable range of the ADC. In this case the user can save on signal conditioning circuit for each channel.

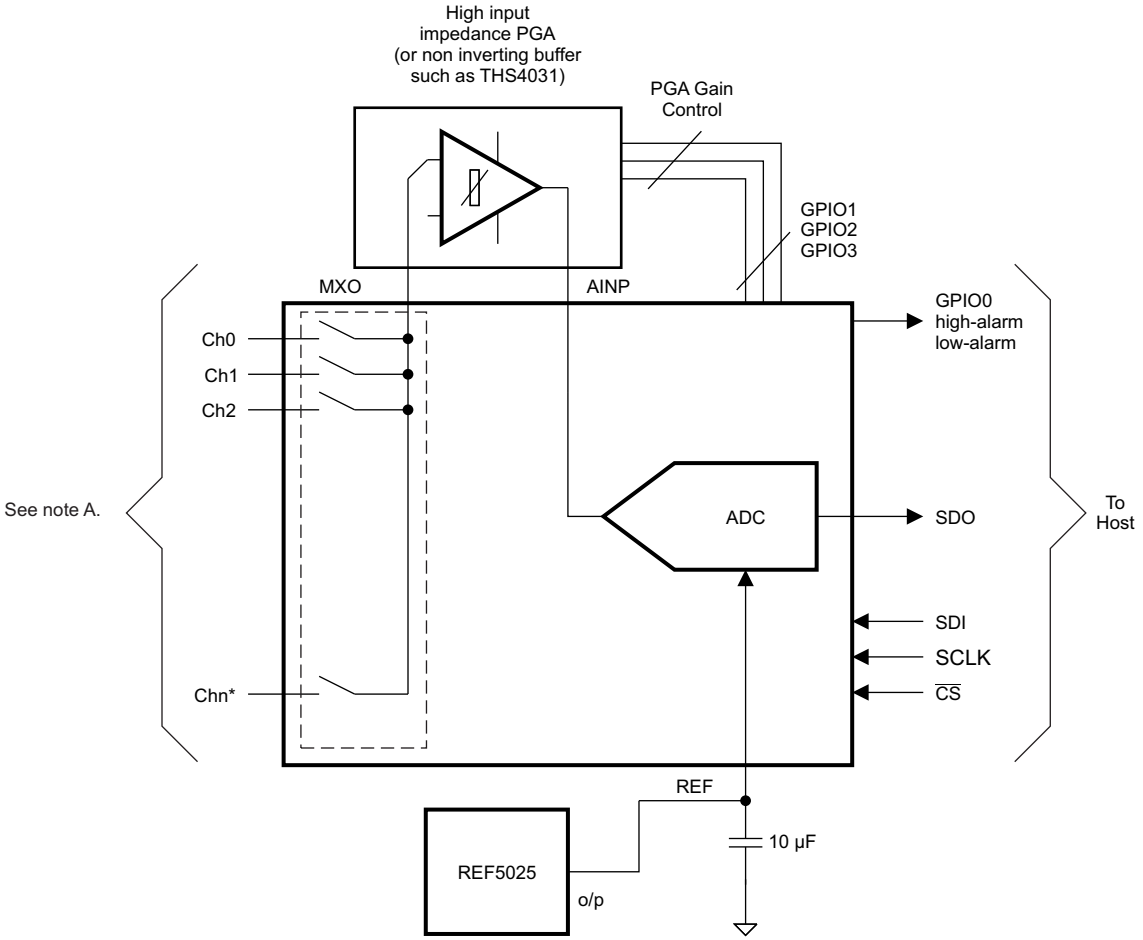


Figure 61. Typical Application Diagram Showing Common Buffer/PGA for All Channels

When the converter samples an input, the voltage difference between AINP and AGND is captured on the internal capacitor array. The (peak) input current through the analog inputs depends upon a number of factors: sample rate, input voltage, and source impedance. The current into the ADS79xx charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. When the converter goes into hold mode, the input impedance is greater than 1 GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain linearity of the converter, the Ch0 .. Chn and AINP inputs should be within the limits specified. Outside of these ranges, converter linearity may not meet specifications.

Application Information (continued)

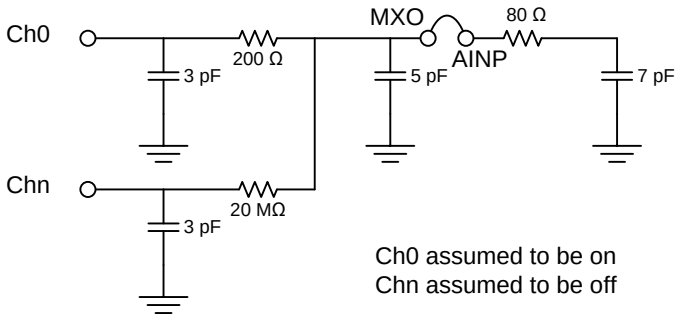
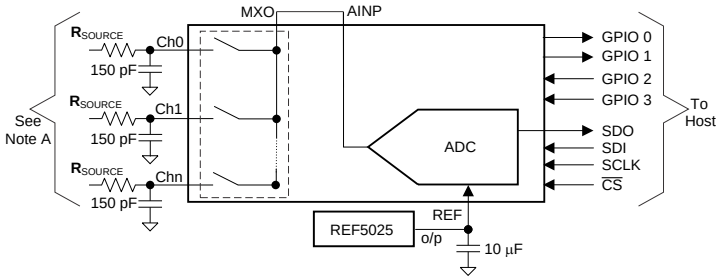


Figure 62. ADC and MUX Equivalent Circuit

9.2 Typical Applications

9.2.1 Unbuffered Multiplexer Output (MXO)

This application is the most typical application, but requires the lowest R_{SOURCE} for good performance. In this configuration, the $2xV_{REF}$ range allows larger source impedance than the $1xV_{REF}$ range because the $1xV_{REF}$ range LSB size is smaller, thus making it more sensitive to settling error.



A. A restriction on the source impedance exists. $R_{SOURCE} \leq 100\ \Omega$ for the $1xV_{REF}$ 12-bit settling at 1 MSPS or $R_{SOURCE} \leq 250\ \Omega$ for the $2xV_{REF}$ 12-bit settling at 1 MSPS.

Figure 63. Application Diagram for an Unbuffered MXO

9.2.1.1 Design Requirements

The design is optimized to show the input source impedance (R_{SOURCE}) from the 100 Ω to 10000 Ω required to meet the 1-LSB settling at 12-bit, 10-bit, and 8-bit resolutions at different throughput in $1xV_{REF}$ (2.5-V) and $2xV_{REF}$ (5-V) input ranges.

9.2.1.2 Detailed Design Procedure

Although the required input source impedance can be estimated assuming a 0.5-V initial error and exponential recovery during sampling (acquisition) time, this estimation over-simplifies the complex interaction between the converter and source, thus yielding inaccurate estimates. Thus, this design uses an iterative approach with the converter itself to provide reliable impedance values.

To determine the actual maximum source impedance for a particular resolution and sampling rate, two subsequent channels are set at least 95% of the full-scale range apart. With a $1xV_{REF}$ range and 2.5 V_{REF}, the channel difference is at least 2.375 V. With $2xV_{REF}$ and 2.5 V_{REF}, the difference is at least 4.75 V. With a source impedance from 100 Ω to 10,000 Ω, the conversion runs at a constant rate and a channel update is issued that captures the first couple samples after the update. This process is repeated at least 100 times to remove any noise and to show a clear settling error. The first sample after the channel update is then compared against the second one. If the first and second samples are more than 1 LSB apart, throughput rate is reduced until the settling error becomes 1 LSB, which then sets the maximum throughput for the selected impedance. The whole process is repeated for nine different impedances from 100 Ω to 10000 Ω.

Typical Applications (continued)

9.2.1.3 Application Curves

These curves show the R_{SOURCE} for an unbuffered MXO.

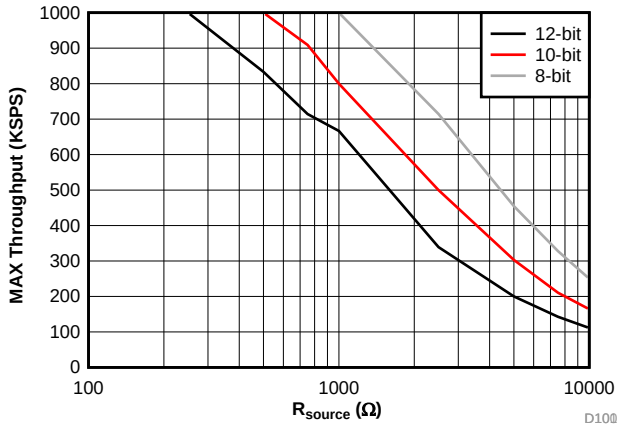


Figure 64. 2xV_{REF} Input Range Settling Without an MXO Buffer

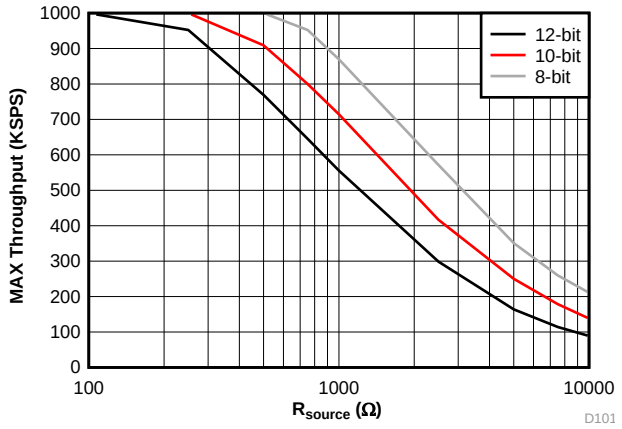
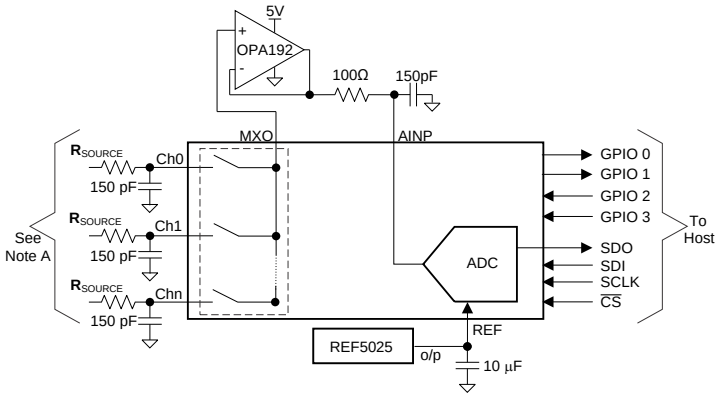


Figure 65. 1xV_{REF} Input Range Settling Without an MXO Buffer

Typical Applications (continued)

9.2.2 OPA192 Buffered Multiplexer Output (MXO)

The use of a buffer relaxes the R_{SOURCE} requirements to an extent. Charge from the sample-and-hold capacitor no longer dominates as a residual charge from a previous channel. Although having good performance is possible with a larger impedance using the OPA192, the output capacitance of the MXO also holds the previous channel charge and cannot be isolated, which limits how large the input impedance can finally be for good performance. In this configuration, the $1xV_{REF}$ range allows slightly higher impedance because the OPA192 (20 V/µs) slews approximately 2.5 V in contrast to the $2xV_{REF}$ range that requires the OPA192 to slew approximately 5 V.



A. Restriction on the source impedance exists. $R_{(SOURCE)} \leq 500\ \Omega$ for a 12-bit settling at 1 MSPS with both $1xV_{REF}$ and $2xV_{REF}$ ranges.

Figure 66. Application Diagram for an OPA192 Buffered MXO

9.2.2.1 Design Requirements

The design is optimized to show the input source impedance (R_{SOURCE}) from the 100 Ω to 10000 Ω required to meet a 1-LSB settling at 12-bit, 10-bit, and 8-bit resolutions at different throughput in $1xV_{REF}$ (2.5 V) and $2xV_{REF}$ (5 V) input ranges.

9.2.2.2 Detailed Design Procedure

The design procedure is similar to the unbuffered-MXO application, but includes an operation amplifier in unity gain as a buffer. The most important parameter for multiplexer buffering is slew rate. The amplifier must finish slewing before the start of sampling (acquisition) to keep the buffer operating in small-signal mode during sampling (acquisition) time. Also, between the buffer output and converter input (INP), there must be a capacitor large enough to keep the buffer in small-signal operation during sampling (acquisition) time. Because 150 pF is large enough to protect the buffer form hold charge from internal capacitors, this value selected along with the lowest impedance that allows the op amp to remain stable.

The converter allows the MXO to settle approximately 600 ns before sampling. During this time, the buffer slews and then enters small-signal operation. For a 5-V step change, slew rate stays constant during the first 4 V. The last 1 V includes a transition from slewing and non-slewing. Thus, the buffer cannot be assumed to keep a constant slew during the 600 ns available for MXO settling. Assuming that the last 1-V slew is reduced to half is recommended. For this reason, slew is 10 V/µs or (5 V_{ref} + 1 V) / 0.6 µs to account for the 1-V slow slew. The OPA192 has a 20-V/us slew, and is capable of driving 150 pF with more than a 50° phase margin with a 50-Ω or 100-Ω R_{iso}, making the OPA192 an ideal selection for the ADS79xx-Q1 family of converters.

Typical Applications (continued)

9.2.2.3 Application Curves

These curves show the R_{SOURCE} for an OPA192 buffered MXO.

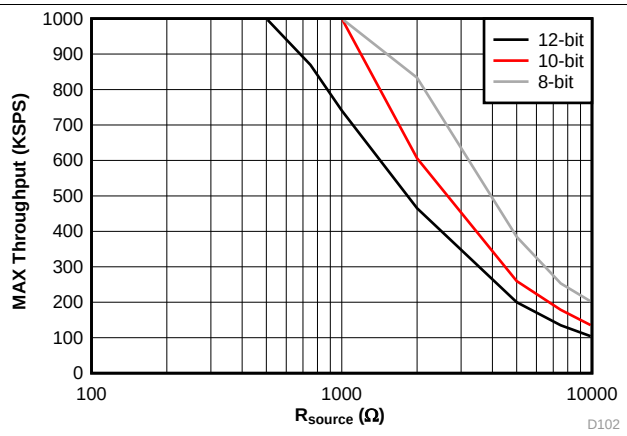


Figure 67. 2xV_{REF} Input Range Settling with an OPA192 MXO Buffer

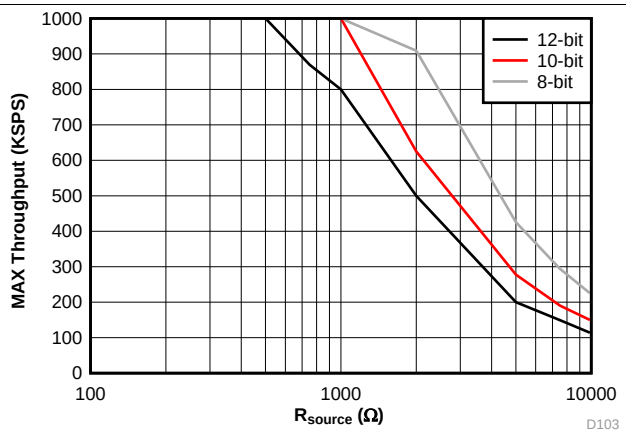


Figure 68. 1xV_{REF} Input Range Settling with an OPA192 MXO Buffer

10 Power Supply Recommendations

The devices are designed to operate from an analog supply voltage (+VA) range from 2.7 V to 5.25 V and a digital supply voltage (+VBD) range from 1.7 V to 5.25 V. Both supplies must be well regulated. The analog supply is always greater than or equal to the digital supply. A 1-µF ceramic decoupling capacitor is required at each supply pin and must be placed as close as possible to the device.

11 Layout

11.1 Layout Guidelines

- A copper fill area underneath the device ties the AGND, BDGND, AINM, and REFM pins together. This copper fill area must also be connected to the analog ground plane of the PCB using at least four vias.
- The power sources must be clean and properly decoupled by placing a capacitor close to each of the three supply pins, as shown in Figure 69 and Figure 70. To minimize ground inductance, ensure that each capacitor ground pin is connected to a grounding via by a very short and thick trace.
- The REFP pin requires a 10-µF ceramic capacitor to meet performance specifications. Place the capacitor directly next to the device. This capacitor ground pin must be routed to the REFM pin by a very short trace, as shown in Figure 69 and Figure 70.
- Do not place any vias between a capacitor pin and a device pin.

NOTE

The full-power bandwidth of the converter makes the ADC sensitive to high frequencies in digital lines. Organize components in the PCB by keeping digital lines apart from the analog signal paths. This design configuration is critical to minimize crosstalk. For example, in Figure 69, input drivers are expected to be on the left of the converter and the microcontroller on the right.

11.2 Layout Examples

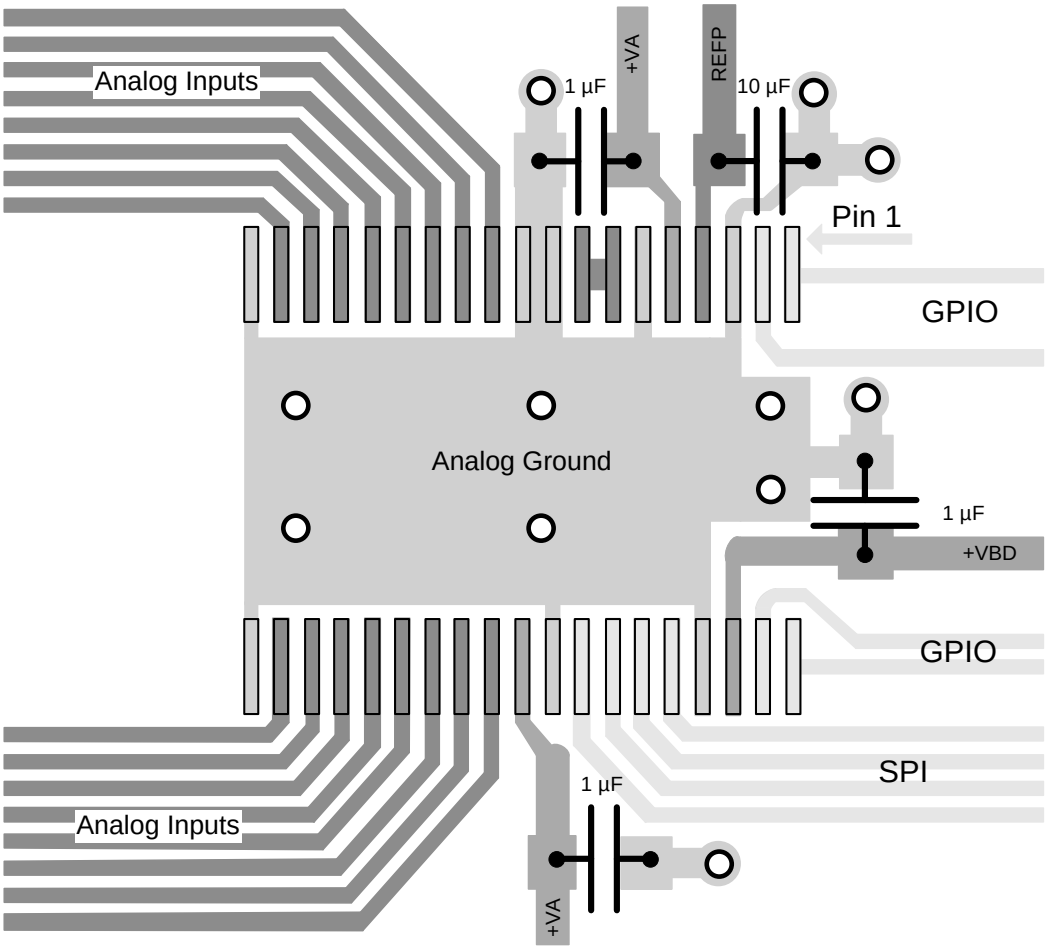


Figure 69. Recommended Layout for the TSSOP Packaged Device

Layout Examples (continued)

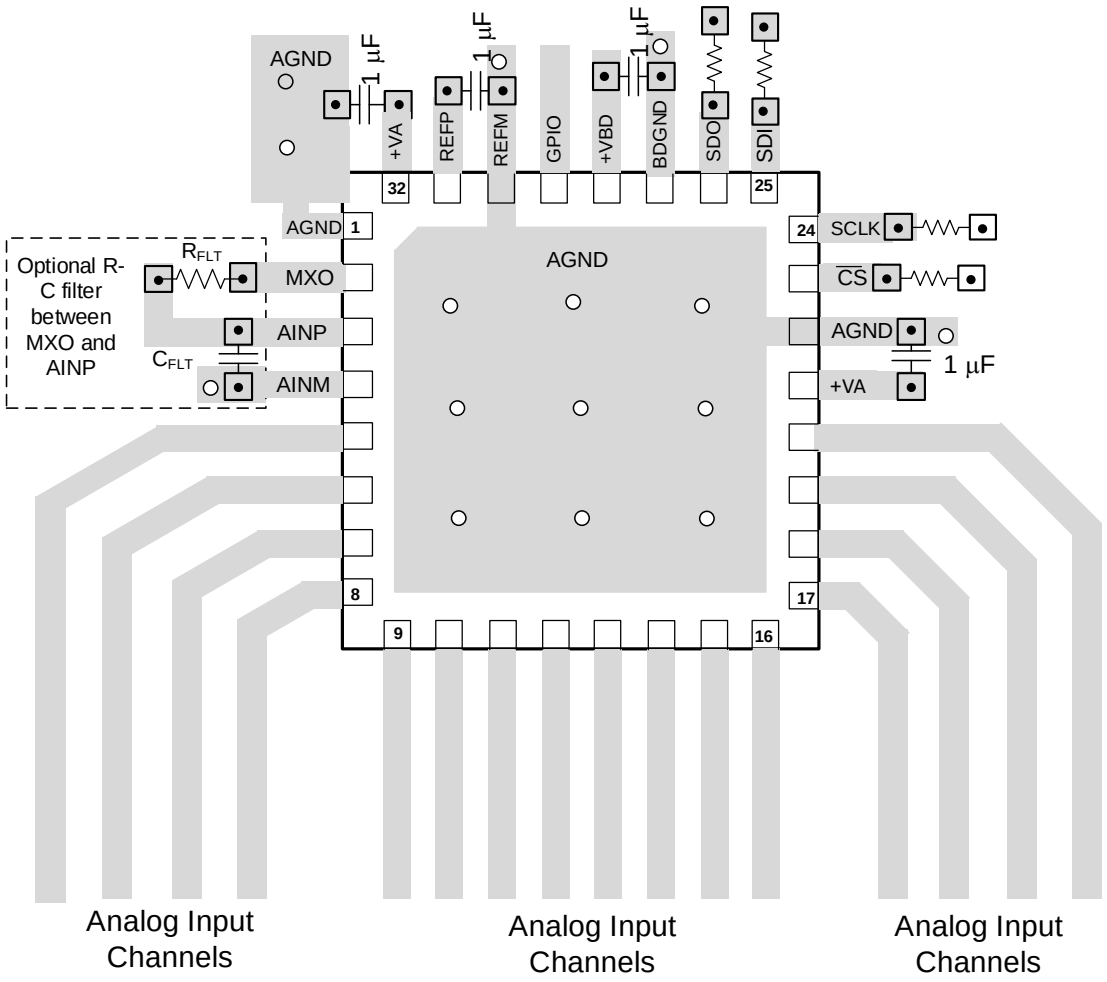


Figure 70. Recommended Layout for the VQFN Packaged Device

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference*
- *OPAx192 36-V, Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with e-trim™*

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 14. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ADS7950	Click here	Click here	Click here	Click here	Click here
ADS7951	Click here	Click here	Click here	Click here	Click here
ADS7952	Click here	Click here	Click here	Click here	Click here
ADS7953	Click here	Click here	Click here	Click here	Click here
ADS7954	Click here	Click here	Click here	Click here	Click here
ADS7955	Click here	Click here	Click here	Click here	Click here
ADS7956	Click here	Click here	Click here	Click here	Click here
ADS7957	Click here	Click here	Click here	Click here	Click here
ADS7958	Click here	Click here	Click here	Click here	Click here
ADS7959	Click here	Click here	Click here	Click here	Click here
ADS7960	Click here	Click here	Click here	Click here	Click here
ADS7961	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7950SBDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7950 B	Samples
ADS7950SBDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7950 B	Samples
ADS7950SBRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7950 B	Samples
ADS7950SBRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7950 B	Samples
ADS7950SDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7950	Samples
ADS7950SDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7950	Samples
ADS7950SRGER	NRND	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7950	
ADS7950SRGET	NRND	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7950	
ADS7951SBDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7951 B	Samples
ADS7951SBDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7951 B	Samples
ADS7951SBRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS 7951 B	Samples
ADS7951SBRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS 7951 B	Samples
ADS7951SDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7951	Samples
ADS7951SDBTG4	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7951	Samples
ADS7951SDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7951	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7951SRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS 7951	Samples
ADS7951SRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS 7951	Samples
ADS7952SBDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7952 B	Samples
ADS7952SBDBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7952 B	Samples
ADS7952SBDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7952 B	Samples
ADS7952SBRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7952 B	Samples
ADS7952SBRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7952 B	Samples
ADS7952SDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7952	Samples
ADS7952SDBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7952	Samples
ADS7952SDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7952	Samples
ADS7952SRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7952	Samples
ADS7952SRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7952	Samples
ADS7953SBDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7953 B	Samples
ADS7953SBDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7953 B	Samples
ADS7953SBRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7953 B	Samples
ADS7953SBRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7953 B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7953SDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7953	Samples
ADS7953SDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7953	Samples
ADS7953SRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7953	Samples
ADS7953SRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7953	Samples
ADS7954SDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7954	Samples
ADS7954SDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7954	Samples
ADS7954SRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7954	Samples
ADS7954SRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7954	Samples
ADS7955SDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7955	Samples
ADS7955SDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7955	Samples
ADS7955SRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7955	Samples
ADS7955SRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7955	Samples
ADS7956SDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7956	Samples
ADS7956SDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7956	Samples
ADS7956SRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7956	Samples
ADS7956SRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7956	Samples
ADS7957SDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7957	Samples
ADS7957SDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7957	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7957SRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7957	Samples
ADS7957SRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7957	Samples
ADS7958SDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7958	Samples
ADS7958SDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7958	Samples
ADS7958SRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7958	Samples
ADS7958SRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7958	Samples
ADS7959SDBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7959	Samples
ADS7959SDBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7959	Samples
ADS7959SRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7959	Samples
ADS7959SRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7959	Samples
ADS7960SDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7960	Samples
ADS7960SDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7960	Samples
ADS7960SRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7960	Samples
ADS7960SRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7960	Samples
ADS7961SDBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7961	Samples
ADS7961SDBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7961	Samples
ADS7961SDBTRG4	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS7961	Samples
ADS7961SRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7961	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7961SRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7961	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF ADS7950, ADS7951, ADS7952, ADS7953, ADS7954, ADS7955, ADS7956, ADS7957, ADS7958, ADS7959, ADS7960, ADS7961 :

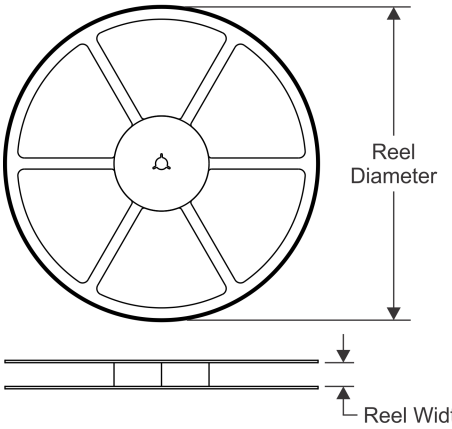
- Automotive: ADS7950-Q1, ADS7951-Q1, ADS7952-Q1, ADS7953-Q1, ADS7954-Q1, ADS7955-Q1, ADS7956-Q1, ADS7957-Q1, ADS7958-Q1, ADS7959-Q1, ADS7960-Q1, ADS7961-Q1

NOTE: Qualified Version Definitions:

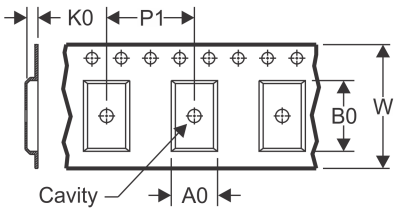
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

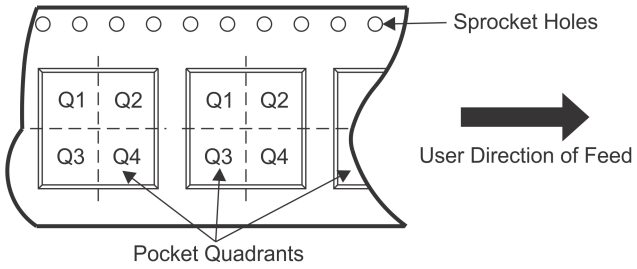


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

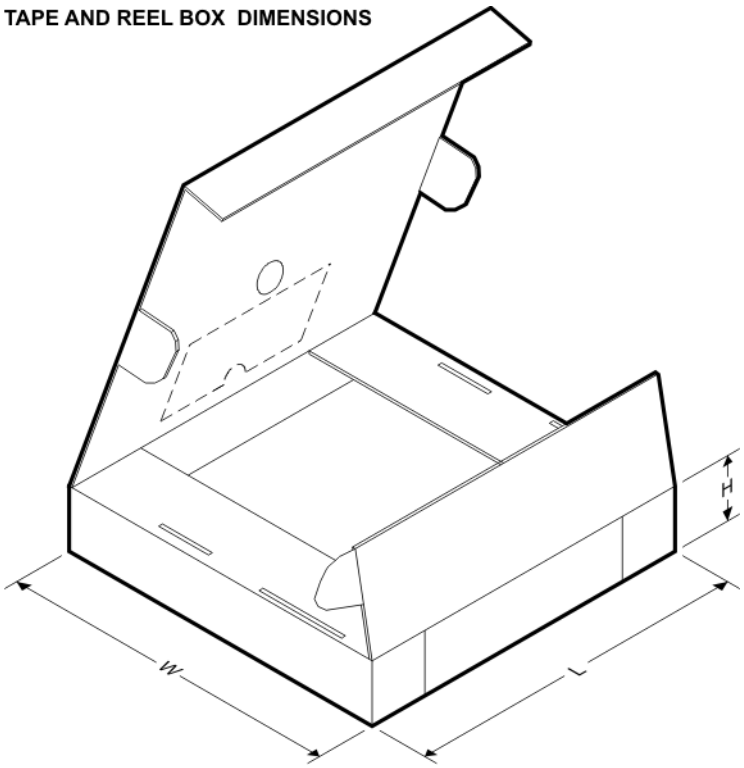


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7950SBDBTR	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
ADS7950SBRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS7950SBRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS7950SDBTR	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
ADS7950SRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS7950SRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS7951SBDBTR	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
ADS7951SBRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS7951SBRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS7951SDBTR	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
ADS7951SRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS7951SRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS7952SBDBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
ADS7952SBRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADS7952SBRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADS7952SDBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
ADS7952SRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADS7952SRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7953SBDBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
ADS7953SBRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADS7953SBRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADS7953SDBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
ADS7953SRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADS7953SRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADS7954SDBTR	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
ADS7954SRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS7954SRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS7955SDBTR	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
ADS7955SRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS7955SRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS7956SDBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
ADS7956SRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADS7956SRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADS7957SDBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
ADS7957SRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADS7957SRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADS7958SDBTR	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
ADS7958SRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS7958SRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS7959SDBTR	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
ADS7959SRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS7959SRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS7960SDBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
ADS7960SRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADS7960SRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADS7961SDBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
ADS7961SRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADS7961SRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

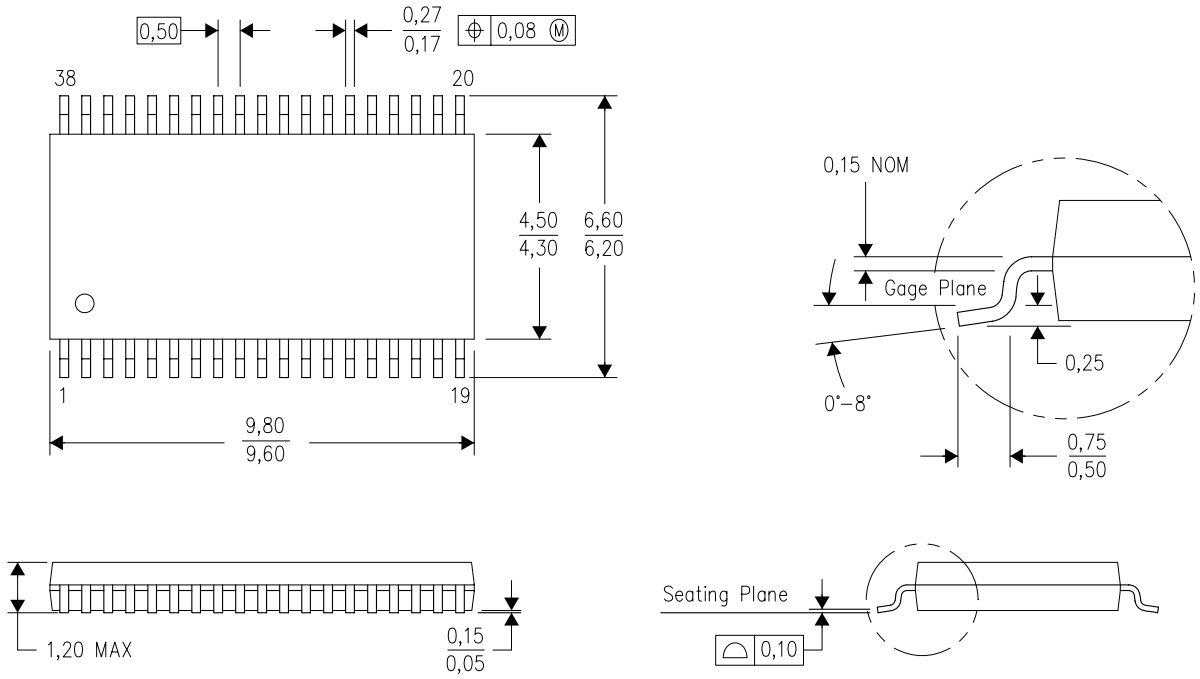


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7950SBDBTR	TSSOP	DBT	30	2000	367.0	367.0	38.0
ADS7950SBRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
ADS7950SBRGET	VQFN	RGE	24	250	210.0	185.0	35.0
ADS7950SDBTR	TSSOP	DBT	30	2000	367.0	367.0	38.0
ADS7950SRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
ADS7950SRGET	VQFN	RGE	24	250	210.0	185.0	35.0
ADS7951SBDBTR	TSSOP	DBT	30	2000	367.0	367.0	38.0
ADS7951SBRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
ADS7951SBRGET	VQFN	RGE	24	250	210.0	185.0	35.0
ADS7951SDBTR	TSSOP	DBT	30	2000	367.0	367.0	38.0
ADS7951SRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
ADS7951SRGET	VQFN	RGE	24	250	210.0	185.0	35.0
ADS7952SBDBTR	TSSOP	DBT	38	2000	367.0	367.0	38.0
ADS7952SBRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
ADS7952SBRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
ADS7952SDBTR	TSSOP	DBT	38	2000	367.0	367.0	38.0
ADS7952SRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
ADS7952SRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
ADS7953SBDBTR	TSSOP	DBT	38	2000	367.0	367.0	38.0
ADS7953SBRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7953SBRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
ADS7953SDBTR	TSSOP	DBT	38	2000	367.0	367.0	38.0
ADS7953SRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
ADS7953SRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
ADS7954SDBTR	TSSOP	DBT	30	2000	367.0	367.0	38.0
ADS7954SRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
ADS7954SRGET	VQFN	RGE	24	250	210.0	185.0	35.0
ADS7955SDBTR	TSSOP	DBT	30	2000	367.0	367.0	38.0
ADS7955SRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
ADS7955SRGET	VQFN	RGE	24	250	210.0	185.0	35.0
ADS7956SDBTR	TSSOP	DBT	38	2000	367.0	367.0	38.0
ADS7956SRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
ADS7956SRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
ADS7957SDBTR	TSSOP	DBT	38	2000	367.0	367.0	38.0
ADS7957SRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
ADS7957SRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
ADS7958SDBTR	TSSOP	DBT	30	2000	367.0	367.0	38.0
ADS7958SRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
ADS7958SRGET	VQFN	RGE	24	250	210.0	185.0	35.0
ADS7959SDBTR	TSSOP	DBT	30	2000	367.0	367.0	38.0
ADS7959SRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
ADS7959SRGET	VQFN	RGE	24	250	210.0	185.0	35.0
ADS7960SDBTR	TSSOP	DBT	38	2000	367.0	367.0	38.0
ADS7960SRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
ADS7960SRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
ADS7961SDBTR	TSSOP	DBT	38	2000	367.0	367.0	38.0
ADS7961SRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
ADS7961SRHBT	VQFN	RHB	32	250	210.0	185.0	35.0

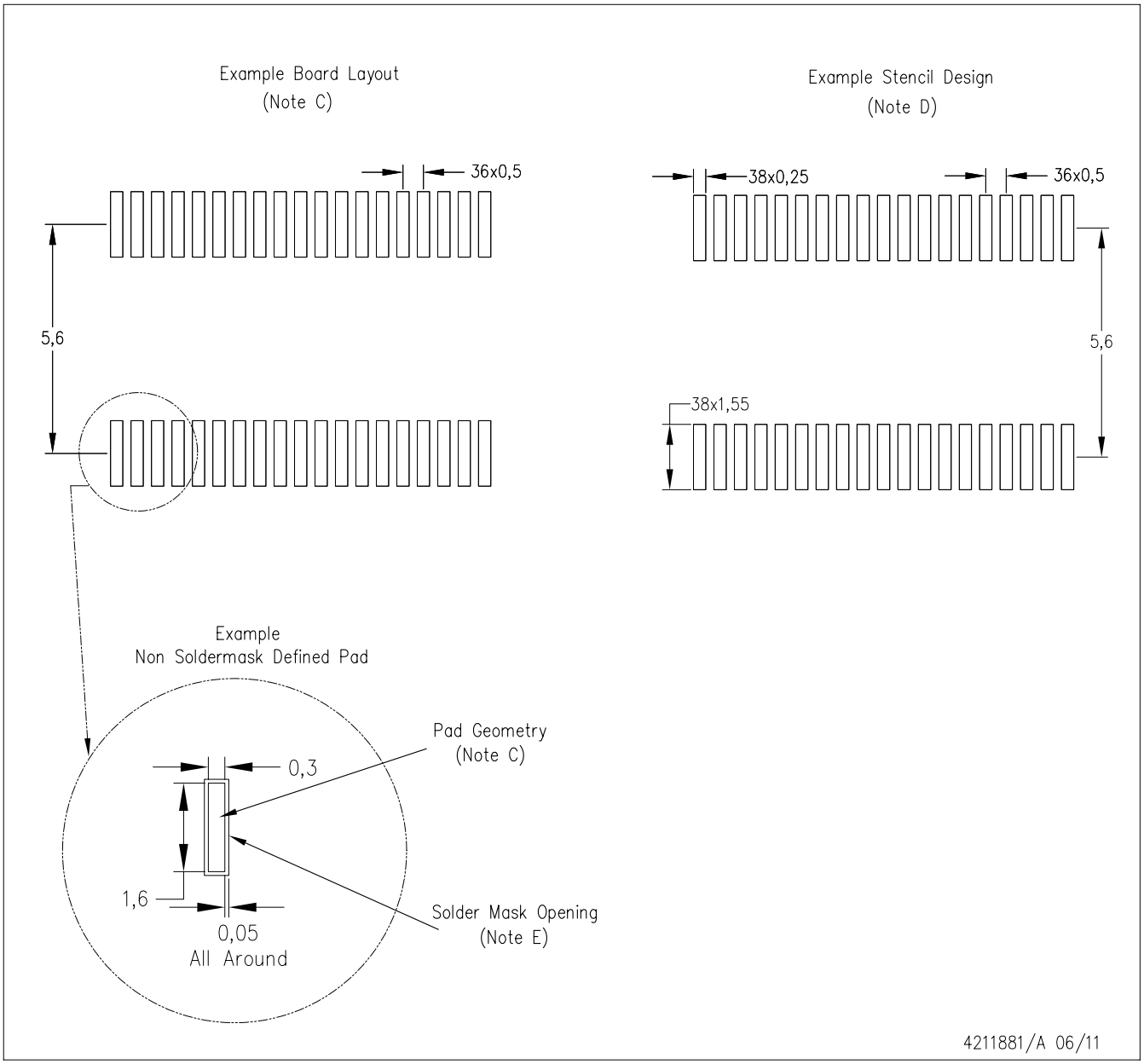
DBT (R–PDSO–G38) PLASTIC SMALL OUTLINE



4073252-6/I 03/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–153.

DBT (R–PDSO–G38) PLASTIC SMALL OUTLINE

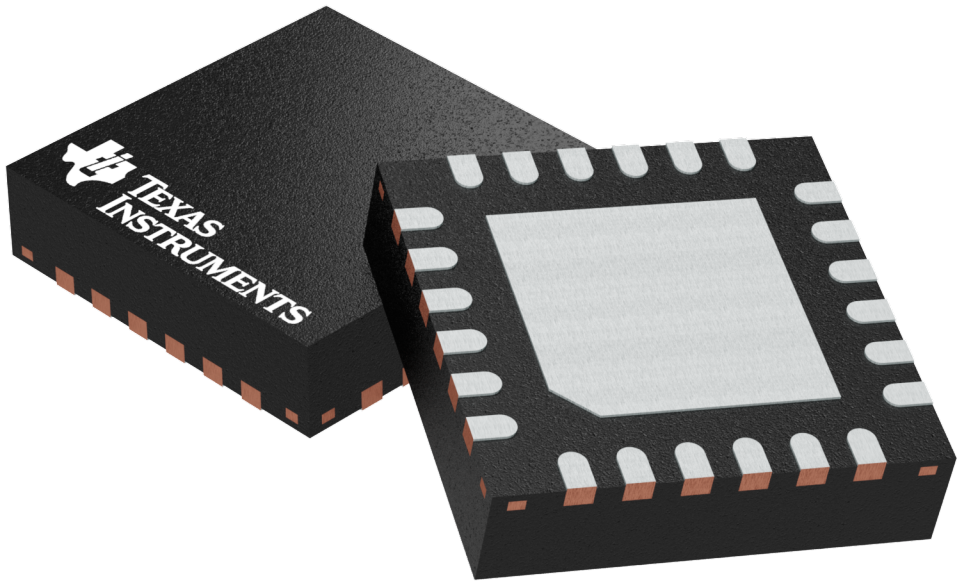


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

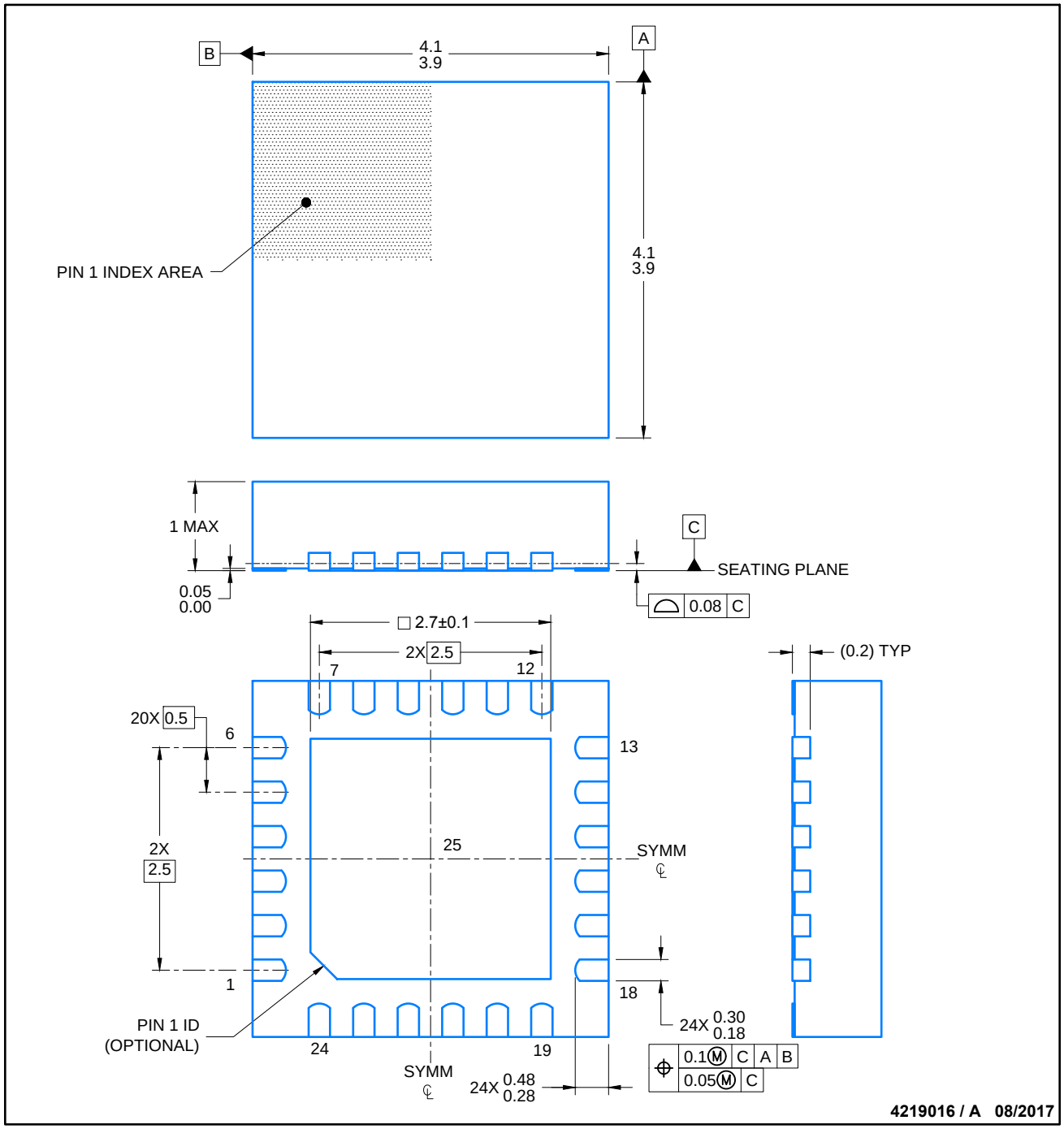
4204104/H

PACKAGE OUTLINE

RGE0024H

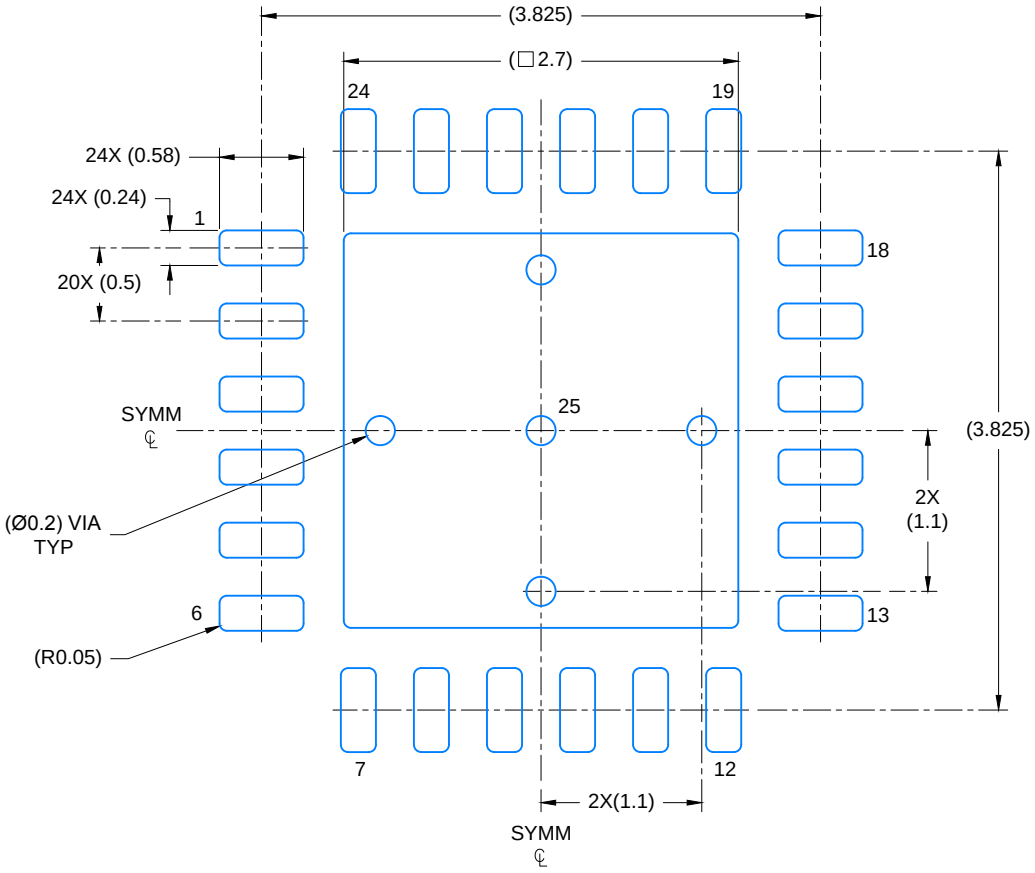
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



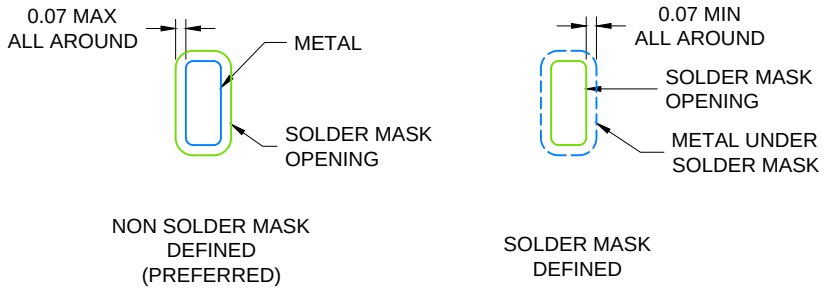
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X

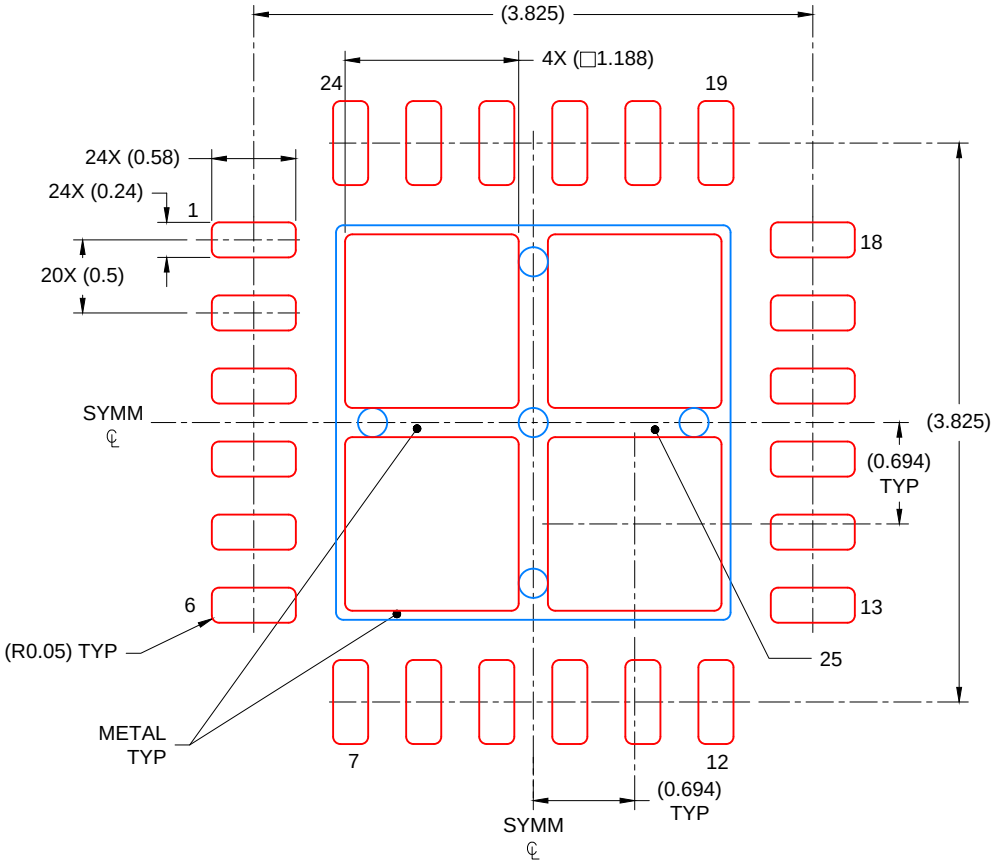


SOLDER MASK DETAILS

4219016 / A 08/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

4219016 / A 08/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

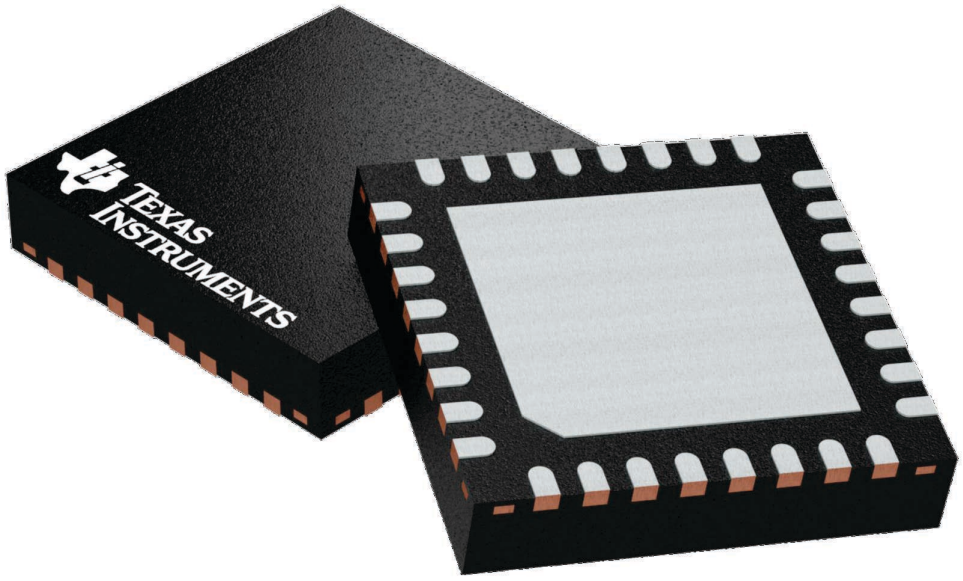
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

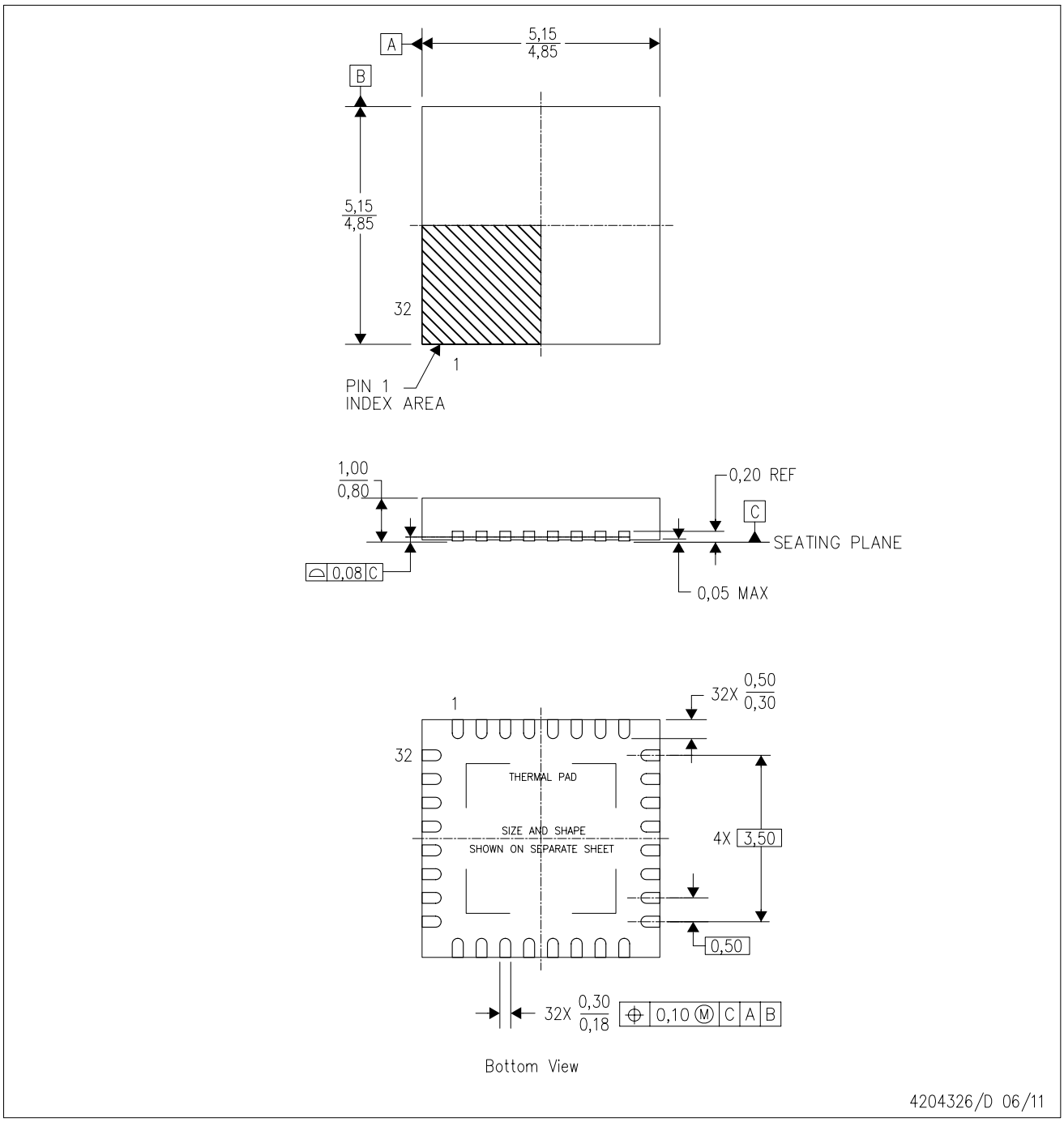
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

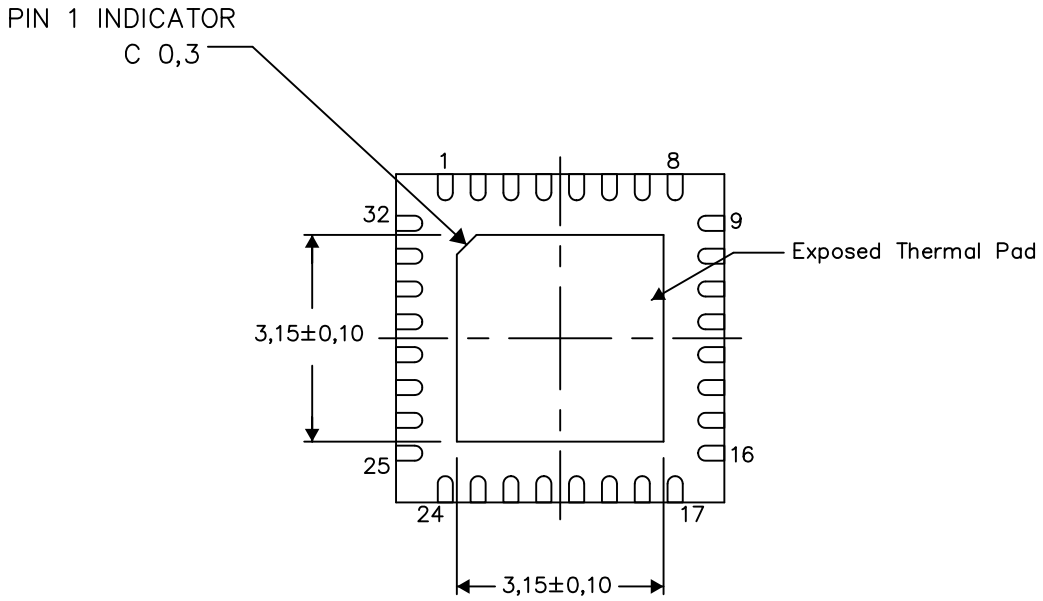
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



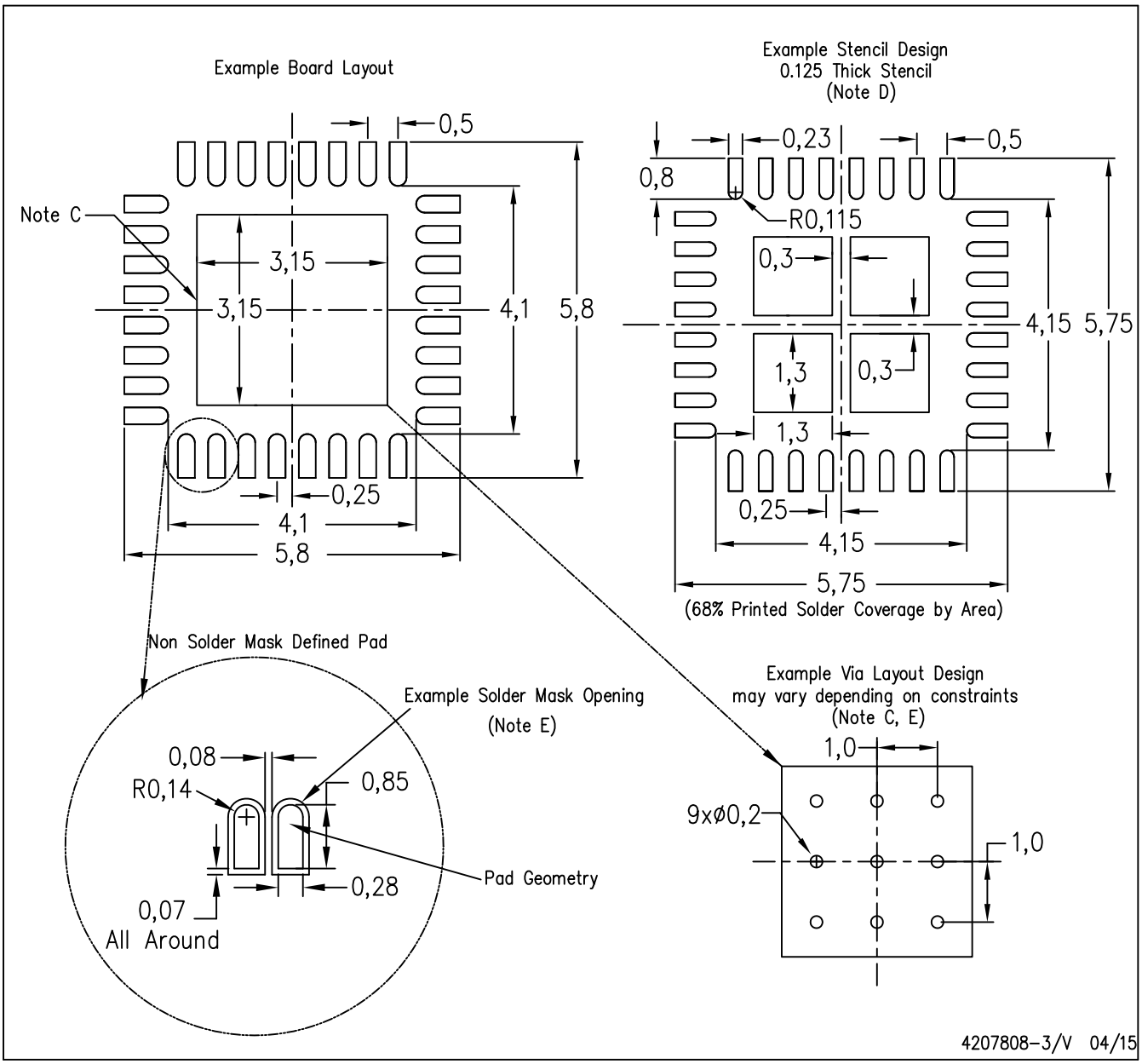
Bottom View

Exposed Thermal Pad Dimensions

4206356–3/AC 05/15

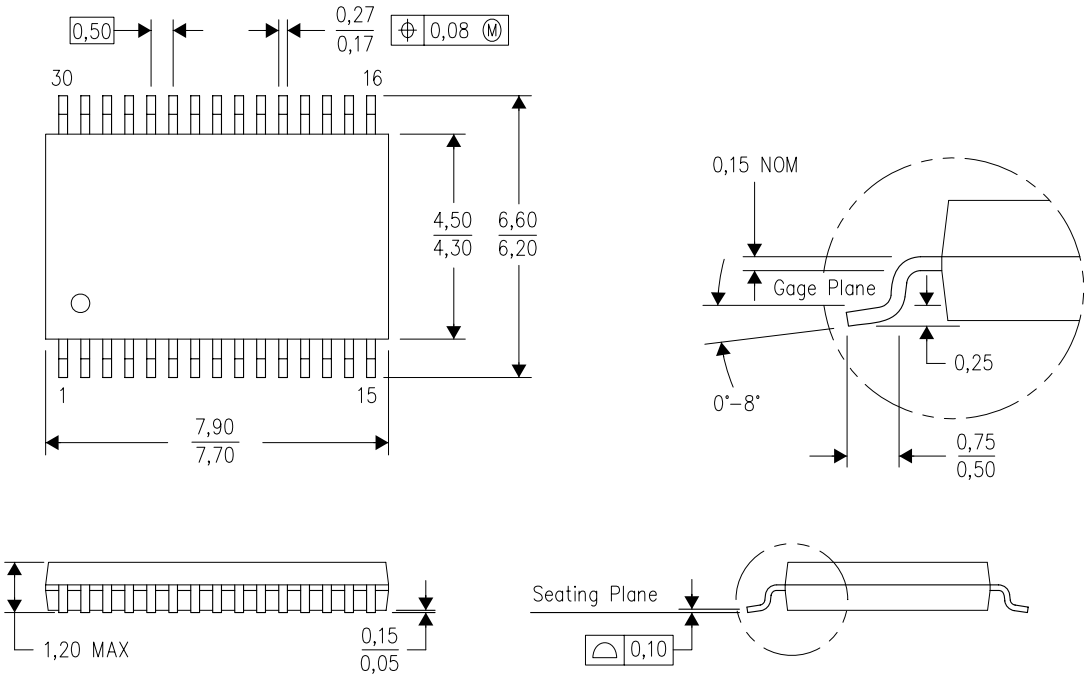
NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

DBT (R–PDSO–G30) PLASTIC SMALL OUTLINE



4073252–5/I 03/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–153.

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