PCN Number:	20190917000.2	**PCN Date:**	Sept 18, 2019
Title:	Qualification of DMOS6, CARZ as additional Fab site and Assembly/Test site options for select devices		
Customer Contact:	PCN Manager	**Phone:** +1(214)480-6037	**Dept:** Quality Services
***Proposed 1st Ship Date:**	Mar 18, 2020	**Estimated Sample Availability:**	Date Provided at Sample request

Change Type:

☒	Assembly Site	☐	Design	☐	Wafer Bump Site
☐	Assembly Process	☐	Data Sheet	☐	Wafer Bump Material
☒	Assembly Materials	☐	Part number change	☐	Wafer Bump Process
☐	Mechanical Specification	☒	Test Site	☒	Wafer Fab Site
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Materials
				☐	Wafer Fab Process

PCN Details

Description of Change:

This change notification is to announce the addition of DMOS6, CARZ as additional Fab site and Assembly/Test site options for select devices. Material differences as follows.

Fab Site:

	Current Site/Process	**Additional Site/Process**
Wafer Fab	DP1DM5 /LBC8 Process	DMOS6/LBC8 Process
Wafer Diam	8 inch	12 inch

Assembly & Test Site:

	UTAC	**CARZ**
Mold Compound	CZ0141	444566
Lead Finish	NiPdAu	NiPdAu (Top Side Roughened)

Test coverage, insertions, conditions will remain consistent with current testing and verified with test MQ.

Reason for Change:

Continuity of supply.

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

None

Anticipated impact on Material Declaration

☐	No Impact to the Material Declaration	☒	Material Declarations or Product Content reports are driven from production data and will be available following the production release. Upon production release the revised reports can be obtained at the site link below http://www.ti.com/quality/docs/materialcontentsearch.tsp

Changes to product identification resulting from this PCN:

Fab Site

Current Chip Site	Chip Site Code (20L)	Chip Country Code (21 L)
DP1DM5	CSO: DM5	USA
Additional Chip Site	Chip Site Code (20L)	Chip Country Code (21 L)
DMOS6	CSO: DM6	USA

Assembly Site

Current Assembly Site		
UTAC	Assembly Site Origin (22L)	ASO: NSE
Additional Assembly Site		
CARZ	Assembly Site Origin (22L)	ASO: CSZ

Sample Product Shipping Label (not actual product label)

G4

2DC: 2Q:

MSL 2 /260C/1 YEAR	SEAL DT
MSL 1 /235C/UNLIM	03/29/04

OPT:
ITEM: 39
LBL: 5A (L)TO:1750

(1P) SN74LS07NSR
(Q) 2000 (D) 0336
(31T)LOT: 3959047MLA
(4W) TKY(1T) 7523483SI2
(P)
(2P) REV: (V) 0033317
(20L) CSO: SHE (21L) CCO:USA
(22L) ASO: MLA (23L) ACO: MYS

Product Affected Devices

TMP451AQDQFRQ1	TMP451HQDQFRQ1	TMP451JQDQFRQ1
TMP451AQDQFTQ1	TMP451HQDQFTQ1	TMP451JQDQFTQ1

Qualification Report

Approved 19-Aug-2019

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS/Lot	Test Name / Condition	Duration	Qual Device: TMP451AQDQFRQ1	Qual Device: TMP451HQDQFRQ1	Qual Device: TMP451JQDQFRQ1	QBS Process Reference: LP87702ARHBRQ1
Test Group A – Accelerated Environment Stress Tests										
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Automotive Preconditioning Level 1	MSL1-260C	3/924/0	-	-	-
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST, 110C/85%RH	264 Hours	3/231/0	-	-	-
AC	A3	JEDEC JESD22-A102	3	77	Autoclave 121C	96 Hours	3/231/0	-	-	-
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle, -65/150C	500 Cycles	3/231/0	-	-	-
PTC	A5	JEDEC JESD22-A105	1	45	Power Temperature Cycle	1000 Cycles	N/A	N/A	N/A	-
HTSL	A6	JEDEC	1	45	High Temp Storage Bake	1000	1/45/0	-	-	-

Type	#	Test Spec	Min Lot Qty	SS/Lot	Test Name / Condition	Duration	Qual Device: TMP451AQDQFRQ1	Qual Device: TMP451HQDQFRQ1	Qual Device: TMP451JQDQFRQ1	QBS Process Reference: LP87702ARHBRQ1
		JESD22-A103			175C	Hours				
Test Group B – Accelerated Lifetime Simulation Tests										
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test, 125C	1000 Hours	3/231/0	-	-	-
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate, 125C	48 Hours	-	-	-	3/2400/0
EDR	B3	AEC Q100-005	3	77	NVM Endurance, Data Retention, and Operational Life	-	N/A	N/A	N/A	-
Test Group C – Package Assembly Integrity Tests										
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear (Cpk>1.67)	Minimum of 5 devices, 30 wires Cpk>1.67	3/240/0	-	-	-
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull (Cpk>1.67)	Minimum of 5 devices, 30 wires Cpk>1.67	3/240/0	-	-	-
SD	C3	JEDEC JESD22-B102	1	15	Surface Mount Solderability >95% Lead Coverage	Pb Free Solder	1/15/0	-	-	-
SD	C3	JEDEC JESD22-B102	1	15	Surface Mount Solderability >95% Lead Coverage	Pb Solder	1/15/0	-	-	-
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions (Cpk>1.67)	-	3/30/0	-	-	-
LI	C6	JEDEC JESD22-B105	1	50	Lead Integrity	-	-	-	-	-
Test Group D – Die Fabrication Reliability Tests										
EM	D1	JESD61	-	-	Electromigration	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDB	D2	JESD35	-	-	Time Dependant Dielectric Breakdown	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Injection Carrier	-	Completed Per Process Technology	Completed Per Process Technology	Completed Per Process Technology	Completed Per Process Technology

Type	#	Test Spec	Min Lot Qty	SS/Lot	Test Name / Condition	Duration	Qual Device: TMP451AQDQFRQ1	Qual Device: TMP451HQDQFRQ1	Qual Device: TMP451JQDQFRQ1	QBS Process Reference: LP87702ARHBRQ1
							Requirements	Requirements	Requirements	Requirements
NBTI	D4	-	-	-	Negative Bias Temperature Instability	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E – Electrical Verification Tests										
HBM	E2	AEC Q100-002	1	3	ESD - HBM - Q100	2000 V	1/3/0	-	-	-
CDM	E3	AEC Q100-011	1	3	ESD - CDM - Q100	750 V	1/3/0	-	-	-
LU	E4	AEC Q100-004	1	6	Latch-up	(Per AEC Q100-004)	1/6/0	-	-	-
ED	E5	AEC Q100-009	3	30	Auto Electrical Distributions	Cpk>1.67 Room, hot, and cold test	1/30/0	1/30/0	1/30/0	-

- QBS: Qual By Similarity
- Qual Device TMP451HQDQFRQ1 is qualified at LEVEL1-260C
- Qual Device TMP451JQDQFRQ1 is qualified at LEVEL1-260C
- Qual Device TMP451AQDQFRQ1 is qualified at LEVEL1-260C

A1 (PC): Preconditioning:
Performed for THB, Biased HAST, AC, uHAST, TC & PTC samples, as applicable.

Ambient Operating Temperature by Automotive Grade Level:
Grade 0 (or E): -40°C to +150°C
Grade 1 (or Q): -40°C to +125°C
Grade 2 (or T): -40°C to +105°C
Grade 3 (or I) : -40°C to +85°C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):
Room/Hot/Cold : HTOL, ED
Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
Room : AC/uHAST

Green/Pb-free Status:
Qualified Pb-Free(SMT) and Green

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