# Three-Phase Sinusoidal Sensorless Fan Controller

## FEATURES AND BENEFITS

- Automotive grade, AEC-Q100 qualified
- Sinusoidal drive for low vibration and noise
- Configurable closed loop speed curves
- RD output
- Quiet startup
- Proprietary high-efficiency control algorithm
- Automatic phase advance
- Windmill detection
- Fault output
- FG speed output
- Lock detection
- Overcurrent limit (OCL)
- Short-circuit protection (OCP)
- Direction input
- Brake input
- Adjustable gate drive

## DESCRIPTION

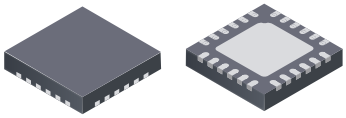
The A5932 three-phase motor controller incorporates sinusoidal drive to minimize audible noise and vibration for high-power fans.

A sinusoidal voltage profile is applied to the windings of the motor at startup to quietly start up and gradually ramp up the motor to desired speed.

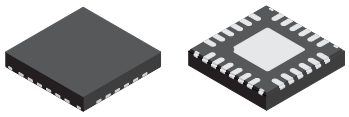
The motor speed is controlled by applying a duty cycle command to the speed (SPD) input. The SPD input is allowed to operate over a wide frequency range.

The A5932 is available in a 24-contact 4 mm × 4 mm QFN with exposed thermal pad (suffix ES), a 24-contact 4 mm × 4 mm QFN with exposed thermal pad and wettable flank (suffix ES, -J option), and a 24-lead TSSOP with exposed thermal pad (suffix LP). These packages are lead (Pb) free, with 100% matte-tin leadframe plating.

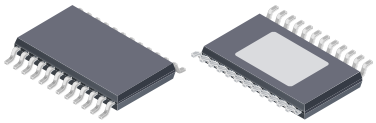
## PACKAGES: *Not to scale*



24-contact QFN
with exposed thermal pad
4 mm × 4 mm × 0.75 mm
(ES package)



24-contact QFN wettable flank
with exposed thermal pad
4 mm × 4 mm × 0.75 mm
(ES package, -J option)



24-lead TSSOP
with exposed thermal pad
(LP package)

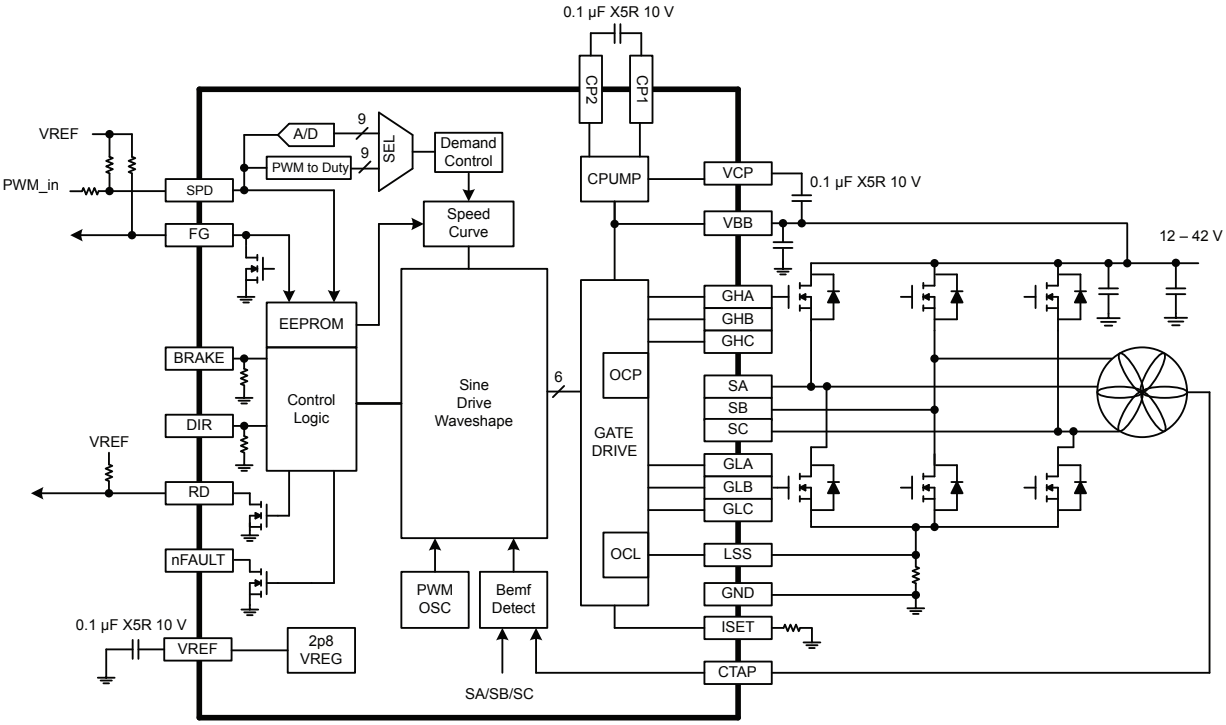



**Figure 1: Typical Application**

## SELECTION GUIDE

| Part Number | Operating Temperature Range ($T_A$) (°C) | Packaging | Packing |
|---|---|---|---|
| A5932GESSR-T | –40 to 105 | 24-contact QFN with exposed thermal pad | 6000 pieces per 13-inch reel |
| A5932KESSR-J | –40 to 150 | 24-contact QFN wettable flank with exposed thermal pad | contact factory |
| A5932GLPTR-T | –40 to 105 | 24-lead TSSOP with exposed thermal pad | 4000 pieces per 13-inch reel |
| A5932KLPTR-T | –40 to 150 | 24-lead TSSOP with exposed thermal pad | 4000 pieces per 13-inch reel |

## ABSOLUTE MAXIMUM RATINGS

| Characteristic | Symbol | Notes | Rating | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{BB}$ | | 50 | V |
| Logic Input Voltage Range | $V_{IN}$ | SPD, BRAKE, DIR | –0.3 to 6 | V |
| Logic Output | $V_O$ | FG (I < 5 mA), RD, nFAULT | 6 | V |
| LSS | $V_{LSS}$ | DC | ±500 | mV |
| | | $t_W$ < 500 ns | ±4 | V |
| Output Voltage | $V_{OUT}$ | SA, SB, SC | –2 to $V_{BB}$+2 | V |
| CTAP | $V_{CTAP}$ | DC | –0.6 to $V_{BB}$+0.6 | V |
| | | $t_W$ < 500 ns | –2 to $V_{BB}$+2 | V |
| GHx | $V_{GHx}$ | | $V_{Sx}$–0.3 to $V_{CP}$+0.3 | V |
| GLx | $V_{GLx}$ | | $V_{LSS}$–0.3 to 8.5 | V |
| VCP | $V_{CP}$ | | $V_{BB}$–0.3 to $V_{BB}$+8 | V |
| CP1 | $V_{CP1}$ | | –0.3 to $V_{BB}$+0.3 | V |
| CP2 | $V_{CP2}$ | | $V_{BB}$–0.3 to $V_{CP}$+0.3 | V |
| ISET | $V_{ISET}$ | | –0.3 to 5.5 | V |
| Maximum EEPROM Write Cycles | $EEPROM_{W(MAX)}$ | | 1000 | cycles |
| Junction Temperature | $T_J$ | | 150 | °C |
| Storage Temperature Range | $T_{stg}$ | | –55 to 150 | °C |
| Operating Temperature Range | $T_A$ | Range G | –40 to 105 | °C |
| | | Range K | –40 to 150 | °C |

## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Test Conditions* | Value | Unit |
|---|---|---|---|---|
| Package Thermal Resistance | $R_{\theta JA}$ | 24-contact QFN (package ES), on 2-sided PCB 1-in.$^2$ copper | 45 | °C/W |
| | | 24-lead TSSOP (package LP), on 2-sided PCB 1-in.$^2$ copper | 36 | °C/W |

*Additional thermal information available on the Allegro website.



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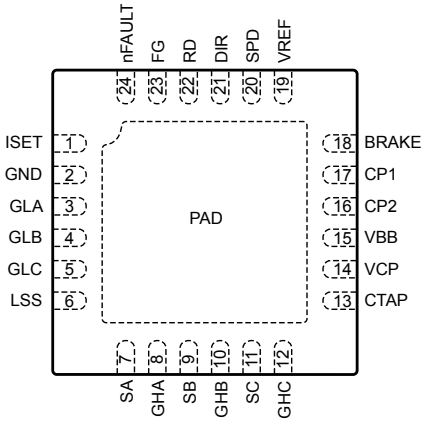
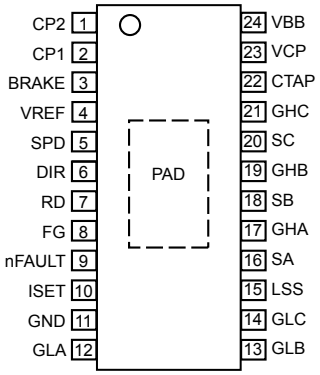
## PINOUT DIAGRAMS AND TERMINAL LIST TABLE




ES Package Pinouts




LP Package Pinouts

### Terminal List Table

| Terminal Number | | Name | Function |
|---|---|---|---|
| ES Package | LP Package | | |
| 16 | 1 | CP2 | Charge pump |
| 17 | 2 | CP1 | Charge pump |
| 18 | 3 | BRAKE | Logic input |
| 19 | 4 | VREF | Logic supply output |
| 20 | 5 | SPD | Speed input |
| 21 | 6 | DIR | Logic output |
| 22 | 7 | RD | Speed output |
| 23 | 8 | FG | Speed output |
| 24 | 9 | nFAULT | Logic output |
| 1 | 10 | ISET | Analog input |
| 2 | 11 | GND | Ground |
| 3 | 12 | GLA | Gate drive output |
| 4 | 13 | GLB | Gate drive output |
| 5 | 14 | GLC | Gate drive output |
| 6 | 15 | LSS | Low side source |
| 7 | 16 | SA | Motor output |
| 8 | 17 | GHA | Gate drive output |
| 9 | 18 | SB | Motor output |
| 10 | 19 | GHB | Gate drive output |
| 11 | 20 | SC | Motor output |
| 12 | 21 | GHC | Gate drive output |
| 13 | 22 | CTAP | Motor common |
| 14 | 23 | VCP | Charge pump |
| 15 | 24 | VBB | Power supply |
| PAD | PAD | PAD | Exposed pad for enhanced thermal dissipation |



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**ELECTRICAL CHARACTERISTICS [1]:** Valid for $T_A$ = –40°C to 105°C (G version) or –40°C to 150°C (K version), unless noted otherwise

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **GENERAL** | | | | | | |
| Load Supply Voltage Range | $V_{BB}$ | Driving | – | – | $V_{BBOV}$ | V |
| | | Operating | 5.5 | – | 50 | V |
| VBB Supply Current | $I_{BB}$ | $I_{VREF}$ = 0 mA | – | 11 | 15 | mA |
| | | Standby mode | – | 10 | 20 | µA |
| Reference Voltage | $V_{REF}$ | $I_{OUT}$ = 20 mA | 2.7 | 2.86 | 2.95 | V |
| VREF Current Limit | $I_{REFOCL}$ | $V_{REF}$ = 0 V | 25 | 50 | 80 | mA |
| Charge Pump | $V_{CP}$ | $V_{BB}$ = 8 V, relative to VBB | 6.5 | 6.8 | 7.5 | V |
| | | $V_{BB}$ = 5.5 V, I = 2 mA | 4.5 | 4.8 | – | V |
| **GATE DRIVE [2]** | | | | | | |
| High Side Gate Drive Output | $V_{GH}$ | $V_{BB}$ = 8 V | 6.5 | 6.8 | – | V |
| Low Side Gate Drive Output | $V_{GL}$ | $V_{BB}$ = 8 V | 7 | 7.5 | – | V |
| Gate Drive Source Current | $I_{SO}$ | $V_{BB}$ = 8 V, relative to target, $R_{ISET}$ = 15 to 60 kΩ | –25 | – | 25 | % |
| | | $V_{BB}$ = 8 V, $R_{ISET}$ = GND | 24 | 32.3 | 40 | mA |
| Gate Drive Sink Current | $I_{SI}$ | $V_{BB}$ = 8 V, relative to target, $R_{ISET}$ = 15 to 30 kΩ | –25 | – | 25 | % |
| | | $V_{BB}$ = 8 V, relative to target, $R_{ISET}$ = 30 to 60 kΩ | –36 | – | 36 | % |
| | | $V_{BB}$ = 8 V, $R_{ISET}$ = GND | 43 | 61.6 | 80 | mA |
| **MOTOR DRIVE** | | | | | | |
| PWM Duty On Threshold | $DC_{ON}$ | Relative to target | –0.5 | – | 0.5 | % |
| PWM Duty OFF Threshold | $DC_{OFF}$ | Relative to target | –0.5 | – | 0.5 | % |
| PWM Input Frequency Range | $f_{PWMIN}$ | | 6 [3] | – | 100 | kHz |
| SPD Standby Threshold (Analog) | $V_{SPDTH}$ | | 0.5 | 0.75 | 1 | V |
| SPD On Threshold | $V_{SPDON}$ | $DC_{ON}$ = 10% | 195 | 235 | 280 | mV |
| SPD Max | $V_{SPDMAX}$ | | – | 2.485 | – | V |
| SPD ADC Resolution | $V_{SPDADC}$ | | – | 4.89 | – | mV |
| SPD ADC Accuracy | | $V_{SPD}$ = 0.2 to 2.5 V, relative to equation | –8 | – | 8 | LSB |
| Speed Setpoint | $f_{SPD}$ | PWM mode | –4 | – | 4 | % |
| Dead Time | $t_{DT}$ | Code = 10 | – | 480 | – | ns |
| Motor PWM Frequency | $f_{PWM}$ | | 23.67 | 24.4 | 25.15 | kHz |

*Continued on next page...*

[1] Specified limits are tested at a single temperature and assured over temperature range by design and characterization.

[2] Gate drive output characteristics valid up to $V_{BBOV}$.

[3] Refer to description for SPD pin.



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**ELECTRICAL CHARACTERISTICS [1] (continued):** Valid for $T_A$ = –40°C to 105°C (G version) or –40°C to 150°C (K version), unless noted otherwise

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **PROTECTION** | | | | | | |
| VBB UVLO | $V_{BBUVLO}$ | $V_{BB}$ rising | – | 4.75 | 4.95 | V |
| VBB UVLO Hysteresis | $V_{BBHYS}$ | | 200 | 300 | 450 | mV |
| VBB Overvoltage Threshold | $V_{BBOV}$ | Relative to target | –4 | – | 4 | % |
| VBB Overvoltage Hysteresis | $V_{BBOVHYS}$ | | 1.7 | 2 | 2.3 | V |
| Overcurrent Threshold | $V_{OCL}$ | | 240 | 255 | 270 | mV |
| VREF UVLO | $V_{REFUVLO}$ | Falling | 2.52 | 2.6 | 2.68 | V |
| VCP UVLO | $V_{CPUVLO}$ | Falling | 3.6 | 3.95 | 4.2 | V |
| | | Rising | 4 | 4.25 | 4.5 | V |
| Lock Timing | $t_{LOCK}$ | Relative to target | –4 | – | 4 | % |
| Thermal Shutdown Temperature | $T_{JTSD}$ | Temperature increasing | 155 | 170 | 190 | °C |
| Thermal Shutdown Hysteresis | $\Delta T_J$ | Recovery = $T_{JTSD} - \Delta T_J$ | – | 20 | – | °C |
| **LOGIC / INPUT OUTPUT / I²C** | | | | | | |
| Input Current (SPD, FG) | $I_{IN}$ | $V_{IN}$ = 0 to 5.5 V | –5 | <1 | 5 | µA |
| Input Current (BRK, DIR) | $I_{IN}$ | $V_{IN}$ = 5 V | 35 | 50 | 75 | µA |
| Logic Input, Low Level | $V_{IL}$ | | 0 | – | 0.8 | V |
| Logic Input, High Level | $V_{IH}$ | | 2 | – | 5.5 | V |
| Logic Input Hysteresis | $V_{HYS}$ | | 150 | 300 | 600 | mV |
| Output Saturation Voltage | $V_{SAT}$ | I = 4 mA | – | – | 0.3 | V |
| FG, RD, nFAULT Output Leakage | $I_{FG}$ | V = 6 V | – | – | 1 | µA |
| SCL Clock Frequency | $f_{CLK}$ | | 3 | – | 400 | kHz |
| **I²C TIMING** | | | | | | |
| Bus Free Time Between Stop/Start | $t_{BUF}$ | | 1.3 | – | – | µs |
| Hold Time Start Condition | $t_{HD:STA}$ | | 0.6 | – | – | µs |
| Setup Time for Start Condition | $t_{SU:STA}$ | | 0.6 | – | – | µs |
| SCL Low Time | $t_{LOW}$ | | 1.3 | – | – | µs |
| SCL High Time | $t_{HIGH}$ | | 0.6 | – | – | µs |
| Data Setup Time | $t_{SU:DAT}$ | | 100 | – | – | ns |
| Data Hold Time | $t_{HD:DAT}$ | | 0 | – | 900 | ns |
| Setup Time for Stop Condition | $t_{SU:STO}$ | | 0.6 | – | – | µs |

[1] Specified limits are tested at a single temperature and assured over temperature range by design and characterization.



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## FUNCTIONAL DESCRIPTION

The A5932 targets high-speed server fan applications to meet the objectives of low audible noise, minimal vibration, and high efficiency. Allegro's proprietary control algorithm results in a sinusoidal current waveshape that adapts to a variety of motor characteristics to dynamically optimize efficiency across a wide range of speeds.

The speed of the fan is controlled by variable duty cycle PWM input. The PWM input duty is measured and converted to a 9-bit number. This 9-bit "demand" is applied to a PWM generator block to create the modulation profile. The modulation profile is applied to the three motor outputs, with 120 degree phase relationship, to create the sinusoidal current waveform as shown in Figure 2.

Protection features include lock detection with restart, motor output short circuit, supply undervoltage monitor, and thermal shutdown.

Standby mode can be achieved by holding SPD pin low for longer than the programmed Lock off-time. In specific speed curve options, the motor will never turn off with 0% duty cycle applied. In this type of configuration, standby mode is not available.

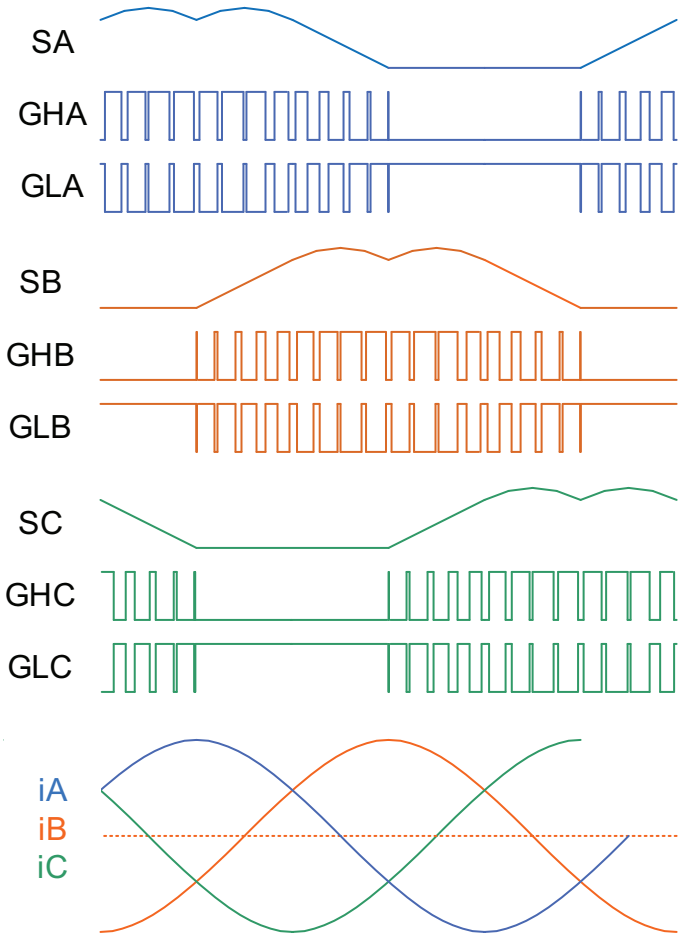


**Figure 2: Sinusoidal PWM (DIR = HI)**



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**VREF.** Voltage reference (2.8 V) to power internal digital logic and analog circuitry. Stabilize with 0.1 µF or greater ceramic capacitor. VREF can be used to power external circuitry with up to 20 mA bias current if desired. For high temperature applications, consider any added extra power dissipation due to regulator load.

$$P_{DISSBIAS} = V_{BB} \times (I_{BB} + I_{REFLOAD})$$

**FG.** Open drain output provides speed information to the system. The open drain output can be pulled up to $V_{REF}$ or external 3.3 or 5 V supply.

The FG output signal typically represents two periods per mechanical revolution. $f_{FGOUT}$ may not be same as electrical frequency:

$$f_{ELEC} = f_{FGOUT} \times NumberOfPolePairs \,/\, 2$$

$$f_{FGOUT} = f_{ELEC} \times 2 \,/\, NumberOfPolePairs$$

$$RPM = 30 \times f_{FGOUT}$$

$$RPM = f_{ELEC} \times 60 \,/\, NumberOfPolePairs$$

**RD.** Open drain output. Logic high indicates a rotor fault condition as defined by EEPROM variables. RD function can be disabled via EEPROM. When function is disabled, RD pin low to high transition indicates end of open-loop starting sequence.

**BRAKE.** Active-high signal turns on all low sides for braking function. Brake function will prevent IC from entering standby mode. Brake function overrides Speed control input. Care should be taken to avoid stress on the MOSFET when braking while motor is running. With braking, the current will be limited by $V_{BEMF}/R_{MOTOR}$.

BRAKE is pulled down internally with 100 kΩ resistor. To avoid any concern with PCB noise, it is recommended to connect pin to GND if brake function not used.

**DIR.** Logic Input to control motor direction. For logic high, motor phases are ordered A→B→C, and for logic low, A→C→B. If Direction input is changed while motor is running, motor will coast for a duration defined by $t_{COAST}$. After this delay, motor will then attempt to restart in desired direction.

DIR is pulled down internally with 100 kΩ resistor. To avoid any concern with PCB noise, it is recommended to connect pin to GND or VREF externally.

**ISET.** A resistor ($R_{ISET}$) to GND sets the magnitude of gate current. The sink and source current ratios are fixed at approximately 2:1. Resistor value $R_{ISET}$ should be in the range 15 to 60 kΩ.

The formula for gate drive current is as follows:

$$I_{GATE\_SRC}\,(\text{mA}) = 2.25 + 900 \,/\, R_{ISET}\,(\text{k}\Omega)$$

$$I_{GATE\_SNK}\,(\text{mA}) = 6.1 + 1666 \,/\, R_{ISET}\,(\text{k}\Omega)$$

If pin ISET is connected to GND, the circuit will default to a level equivalent to approximately 30 kΩ. If ISET is open, the motor outputs will be disabled.

**CTAP.** This analog input is an optional connection for motor common (Wye motors). If not used, as in case of Delta wound motor, then pin must be left open circuit.

**SPD.** Speed Demand input pin. Choice of analog voltage control or PWM duty control is determined by EEPROM selection.

*Duty cycle control.* The input Duty cycle signal is measured with logic circuit. The calculated output number is translated to a speed Demand signal with a resolution of 0.2%.

The maximum input PWM frequency is 100 kHz. To avoid interaction with the I²C circuitry, which share the FG and SPD inputs, the minimum PWM frequency may be limited based on the maximum frequency of the speed output pin FG.

$f_{PWM(min)}$ is the larger number of 2.5 × $f_{FGOUT(max)}$ or 100 Hz.

$f_{FGOUT(max)}$ is the maximum speed under all operating conditions.

Note: $f_{FGOUT}$ (Hz) depends on selection of pole-pair in EEPROM, typically equals RPM / 30.

*Analog control.* Voltage applied will increase speed demand. An internal 9 bit A/D converter will translate the input to a speed demand.

$$Code = V_{IN(SPD)} \,/\, 4.89\ \text{mV} + 3 \text{ where code} = [0\ldots511]$$

$$Applied\ Duty\ (\%) = Code \,/\, 511.$$

**Standby Mode.** A low-power mode is activated if SPD pin is held low. Standby Mode will turn off all circuitry including charge pump and VREF. Upon power up, the A5932 will immediately wake up. If SPD remains low for the programmed lock time, standby mode will be activated. Standby mode can be disabled via EEPROM bit.

**Lock Detect.** A logic circuit monitors the motor position to determine if motor is running as expected. If a fault is detected, the motor drive will be disabled for $t_{LOCK}$ before an auto-restart is attempted.

**OCP.** Overcurrent protection is intended to protect the IC from application conditions of shorted load, motor short to ground, and motor short to battery. The OCP protection monitors the drain to source voltage ($V_{DS}$) across any source or sink driver when the output is turned on. The OCP level can be set to 1 V or 2 V via EEPROM bit VDSTH. If the OCP threshold is exceeded for



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640 ns, all drivers are shut off. This fault mode can be reset by PWM ON/OFF or timeout of $t_{LOCK}$, depending on EEPROM bit OCPOPT.

**Current Limit.** Maximum load current can be set by choice of external sense resistor connected between LSS terminal and GND.

Current limit has an internal blanking filter of approximately 640 ns. Current limit function can be disabled by connecting LSS to power ground on the PCB.

$$I_{LIM} = V_{OCL} / R_{SENSE}$$

**Thermal Shutdown (TSD).** The A5932 protects itself from overheating with an internal thermal monitoring circuit. If the junction temperature exceeds the upper threshold $T_{TSD}$, the outputs will be disabled. Device temperature must fall below the hysteresis level, $T_{HYS}$, to allow a normal restart sequence.

**nFAULT.** The following signals will bring output nFAULT low:

1. $V_{BB}$ undervoltage
2. Thermal shutdown
3. Charge pump UVLO
4. $V_{BB}$ overvoltage
5. Output $V_{DS}$ fault (OCP)
6. Loss of synchronization (rotor lock detected)

**Table 1: Fault Signals and Actions**

| Fault | Fault Action | Latched | Readback / Reg[Bit] |
|---|---|---|---|
| $V_{BB}$ Undervoltage | Disable outputs | N | 147[8] |
| TSD | Disable outputs | N | 147[6] |
| Charge Pump | Disable outputs | N | 147[7] |
| $V_{BB}$ Overvoltage | Disable outputs or disabled outputs and set Lock detect | N | 147[9] |
| VDS Fault | Choose by EEPROM bit OCPOPT | if OCPOPT = 1 | 147[5:0] |
| Loss of Sync | Set Lock detect timeout | N | 148[6:0] |



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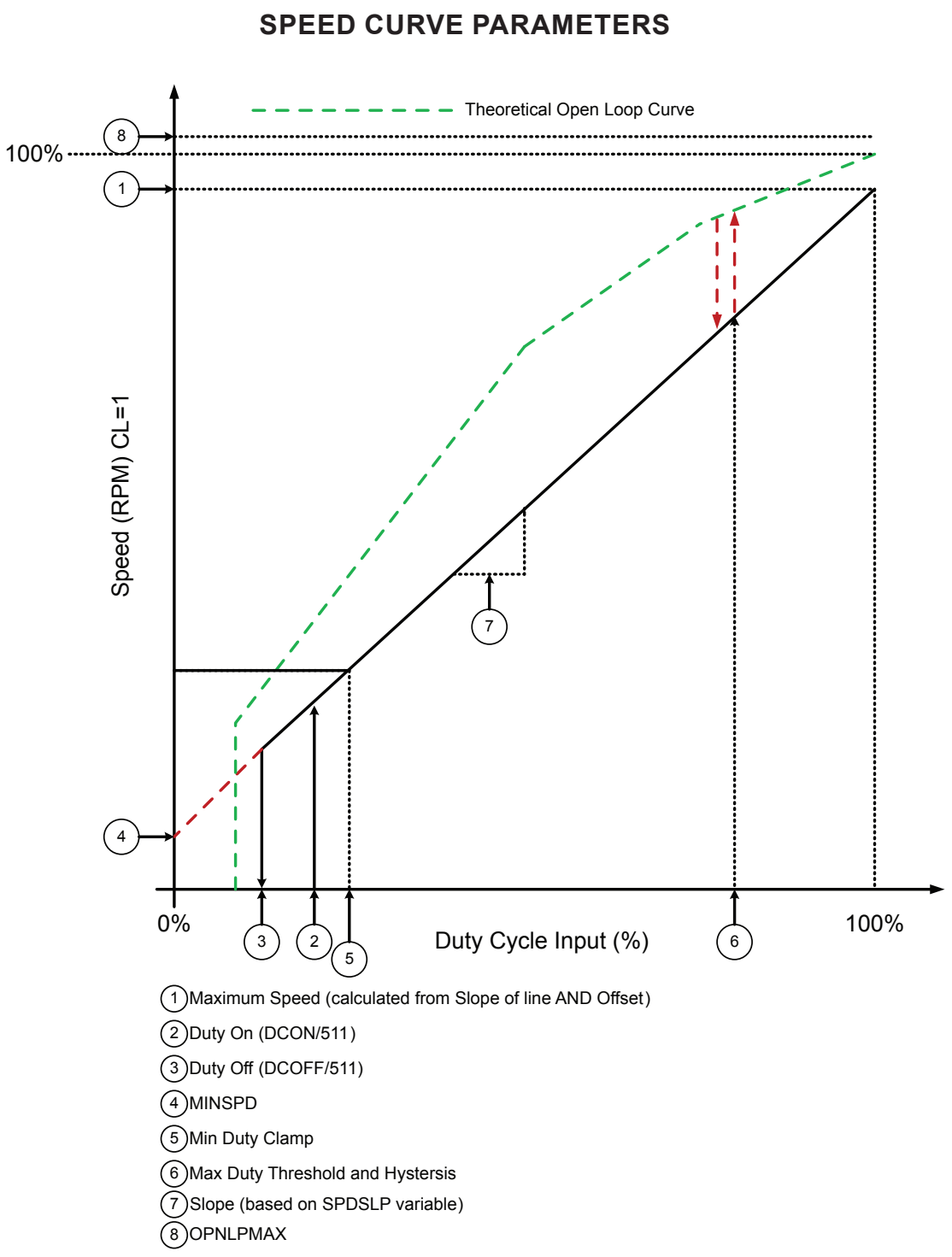


**Figure 3: Speed Curve Options**



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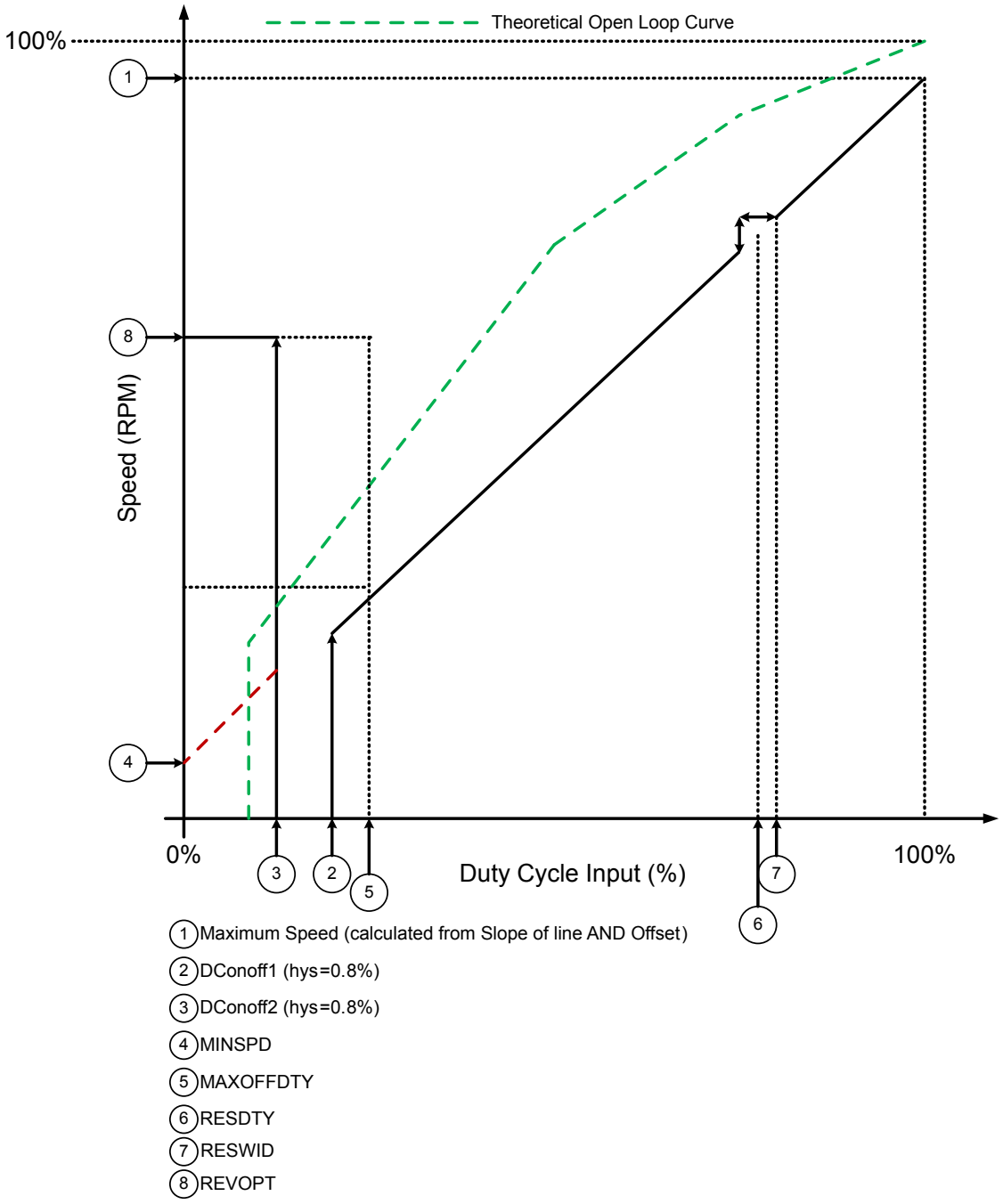


**Figure 4: Speed Curve Options – 2**



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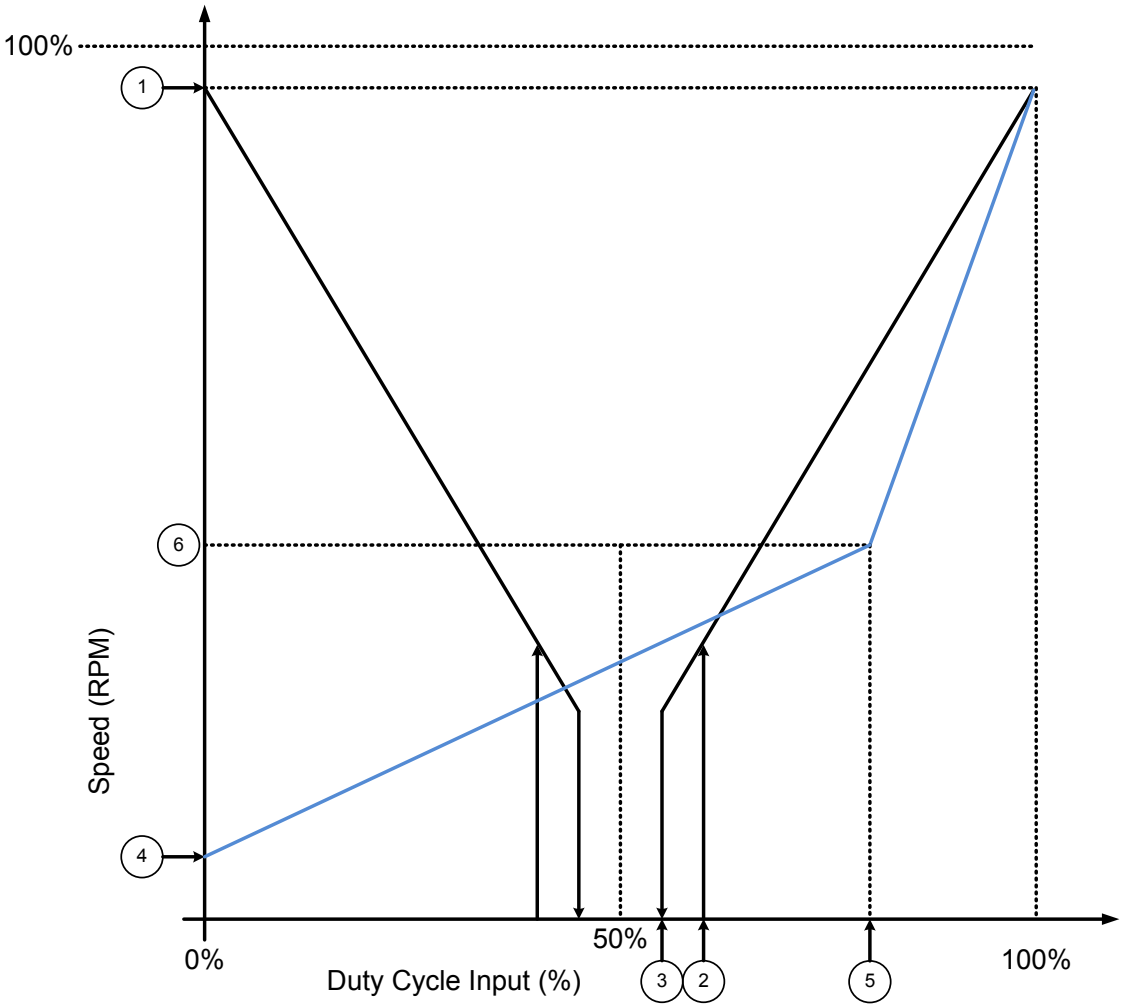


1 Maximum Speed (calculated from Slope of line AND Offset)
2 DCON
3 DCOFF
4 MINSPD
5 SLPSWDTY
6 SLPSWRPM

**Figure 5: Speed Curve Options – 3**



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## Speed Curve Parameters

Refer to Figure 3, Figure 4, and Figure 5 for items below.

**Minimum Speed Setpoint.** The minimum speed is defined by the value stored in EEPROM variable MINSPD. The resolution is 1 rpm.

MINSPD (rpm) = 0..4095

**Maximum Speed Setpoint.** The A5932 calculates the maximum speed based on line equation $y = mx + B$. The maximum speed is defined as the speed with input duty = 100%.

The desired maximum speed is used to set the EEPROM variable SPDSLP.

$$SPDSLP = 64 \times (Maximum\ Speed\ (rpm) - MINSPD) / 511$$

Example: Max Speed = 25000, Min Speed = 3000.

$$SPDSLP = 64 \times 22000 / 511 = 2755$$

where SPDSLP = 0..16383

$$Motor\ Speed\ (rpm) = Slope \times DutyIN + MINSPD.$$

where Slope = SPDSLP × 511 / 64 and DutyIN expressed in %.

**Duty In Enable Threshold.** EEPROM variable DCON defines the input duty signal that enables the drive. DCON is an 8-bit number with resolution of 0.2%, which results in a maximum setting of 49.9%.

$$Duty\ On\ (\%) = 100 \times DCON / 511$$

If DCON is set to "0", motor will turn on with 0% duty cycle input.

**Duty In Disable Threshold.** EEPROM variable DCOFF defines the input duty signal that disables the drive. DCOFF is an 8-bit number with resolution of 0.2%, which results in a maximum setting of 49.9%.

$$Duty\ Off(\%) = DCOFF / 511$$

DCOFF should always be set to a lower number than DCON.

**ON/Off Control Option.** If ONOFFCNTRL bit is set to "1", then the motor will run if duty is between the values set by DCON and DCOFF. A fixed value of 0.8% hysteresis is applied. In this option, if the duty is below DCOFF, then the motor will be enabled with a PWM level set by variable MAXDTYOFF (see Figure 4).

Additionally, if duty is below DCOFF, the motor direction can be made to be reverse if REVOPT is set to "1".

**Duty Cycle Invert.** To create mirror image of speed curve, set duty cycle invert bit to "1".

**Minimum Duty Clamp.** Minimum speed can be clamped to a value to allow motor to run at defined low-level speed. This is achieved by ignoring the duty cycle input if below the programmed MINDTY level.

$$Min\ Duty\ Clamp\ (\%) = 100 \times MINDTY / 511$$

Therefore the minimum speed will be defined by:

$$MinSpeedClamp(rpm) = Slope \times MinDutyClamp + MINSPD$$

Setting MINDTY to 0 disables the function.

MINDTY = 0..255.

**Maximum Duty Clamp.** EEPROM variable DTYMAX defines a duty level at which the motor will change operation from closed-loop curve. The change of operation would depend on MAXDTYOPT setting. If MAXDTYOP = 0, open-loop operation will result. If MAXDTYOPT = 1, then operation will remain closed-loop; however, the speed will be clamped at the value calculated by DTYMAX level.

Four bits are used for this setting at resolution of 1.6% to cover the range 76.5% to 100%.

$$Maximum\ Duty\ (\%) = 100 \times (511 - MAXDTY \times 8) / 511$$

MAXDTY = 0..15; if MAXDTY = 0, then function is disabled.

Hysteresis is needed to prevent motor from going back and forth between open- and closed-loop mode.

MAXDTYHYS = 0...15.

Hys(%) = (MAXDTYHYS + 1) × 0.4

**50% Duty Option.** If bit DIR50 is set to 1, the motor direction can be controlled by duty cycle level (see Figure 5).

For this setting, the motor enable and disable functions will be set by:

DCONnew = 50% ±DCON

DCOFFnew = 50% ±DCOFF

Since the duty cycle reference changes from 100% scale to 50% scale, the slope of the curve is now 2× compared to normal (DIR50 = 0) setting. When duty changes to switch direction, the motor will coast for time programmed via TCOAST variable before attempting to startup in opposite direction. Care should be taken to minimize stress on the MOSFETs when switching direction.



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**Dual Slope Option.** Two different slopes can be selected by setting variable SLPSWDTY greater than 0.

*Slope2 = (MAXSPEED – SLPSWRPM) / (100% – SLPSWDTY)*

*Slope1 = (SLPSWRPM – MINSPEED) / SLPSWDTY*

**Resonance Option** (see Figure 5)**.** To avoid any issues with mechanical resonance at a particular speed band, variable RESWID and RESDTY are provided to allow skipping over a defined RPM.

RESDTY: defines duty cycle that is center of band.

RESWID: defines width of band relative to center duty value.

**Open Loop Maximum Limit.** When the speed curve is set to open loop mode, it is possible to limit the speed to prevent fan speed overshoot. RPM is monitored and the demand will be clamped at level that results in max limit.

OPNLPMAX variable has no effect in closed loop mode.



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## EEPROM MAP

**Table 2: EEPROM Map. Refer to application note and user interface for additional detail.**

| I²C Register | EEPROM Address | Bits | Name | Description | Default Setting | Default Value (decimal) |
|---|---|---|---|---|---|---|
| 64 | 0 | 15:0 | Dev1 | Allegro Reserved | n/a | n/a |
| 65 | 1 | 15:0 | Dev1 | Allegro Reserved | n/a | n/a |
| 66 | 2 | 15:0 | Dev1 | Allegro Reserved | n/a | n/a |
| 67 | 3 | 15:0 | Dev1 | Allegro Reserved | n/a | n/a |
| 68 | 4 | 15:0 | Dev1 | Allegro Reserved | n/a | n/a |
| 69 | 5 | 15:0 | Dev1 | Allegro Reserved | n/a | n/a |
| 70 | 6 | 15:0 | Dev1 | Unused – Can be used by customer | n/a | n/a |
| 71 | 7 | 15:0 | Dev1 | Unused – Can be used by customer | n/a | n/a |
| 72 | 8 | 3:0 | MAXDTYCLP | Range = 100% to 76.5%, LSB = 1.6% | 0 | 0 |
| | | 7:4 | MAXDTYHYS | Range = 0 to 5.9%, LSB = 0.4% | 0 | 0 |
| | | 14:8 | MINDTYCLP | Range = 0 to 49.7%, LSB = 0.4% | 0 | 0 |
| | | 15 | Unused | | | |
| 73 | 9 | 8:0 | STRTDMD | LSB = VBBRNG / 511 | 0.8 V | 17 |
| | | 15:9 | DMDPOST | Range = 0 to 100%, LSB = 0.8% | 79.5% | 202 |
| 74 | 10 | 7:0 | ALIGNT | Range = 0 to 20.4 s, LSB = 100 ms | 0.5 s | 6 |
| | | 15:8 | ASLOPE | Range = 160 ms to 40 s | 0.16 s | 255 |
| 75 | 11 | 7:0 | STRTF | Range = 0 to 15.94 Hz, LSB = 0.0625 mHz | 0.19 Hz | 3 |
| | | 15:8 | ACCEL | Range = 0 to 99.6 Hz/s, LSB = 0.78 | 41.8 Hz | 107 |
| 76 | 12 | 7:0 | ACCELT | Range = 0 to 10.2 s, LSB = 40 ms | 480 ms | 12 |
| | | 15:8 | MAXOFFDTY | Range = 100% to 76.5%, LSB = 0.4% | 100% | 0 |
| 77 | 13 | 3:0 | DMDRMPAL | Range = 3.8 to 63.8 ms/count, LSB = 3.8 | 27.8 ms/count | 6 |
| | | 7:4 | DMDRMPAH | Range = 3.8 to 63.8 ms/count, LSB = 3.8 | 15.8 ms/count | 3 |
| | | 11:8 | DMDRMPDL | Range = 3.8 to 63.8 ms/count, LSB = 3.8 | 27.8 ms/count | 6 |
| | | 15:12 | DMDRMPDH | Range = 3.8 to 63.8 ms/count, LSB = 3.8 | 27.8 ms/count | 6 |
| 78 | 14 | 8:0 | RESDTY | Range = 0 to 100%, LSB = 0.2% | Disabled | 0 |
| | | 15:9 | RESWID | Range = 0 to 50%, LSB = 0.4% | n/a | 0 |
| 79 | 15 | 7:0 | MAXSPD | Maximum Electrical Frequency | 509 Hz | 24 |
| | | 15:8 | TLOCK | 0 to 25.5 s | 5 s | 50 |
| 80 | 16 | 7:0 | RDLOW | Range = 0 to 4095, LSB = 16 RPM | 0 | 0 |
| | | 15:8 | RDHIGH | Range = 0 to 4095, LSB = 16 RPM | 0 | 0 |
| 81 | 17 | 7:0 | RDBLK | Range = 0 to 25.5 s, LSB = 100 ms | 0 | 0 |
| | | 11:8 | RDDLY | Range = 0 to 15 s, LSB = 1 s | 0 | 0 |
| | | 12 | Unused | | | |
| | | 13 | DITHDT | 0 = 1.28 ms, 1 = 5.12 ms/step | 0 | 0 |
| | | 14 | DITHSTP | 0 = 16 steps, 1 = 32 steps | 0 | 0 |
| | | 15 | DITHENB | 1 = Enable | disabled | 0 |

*Continued on next page...*



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## EEPROM MAP (continued)

| I²C Register | EEPROM Address | Bits | Name | Description | Default Setting | Default Value (decimal) |
|---|---|---|---|---|---|---|
| 82 | 18 | 11:0 | PHASLP | Calculated Slope for Linear Phase Advance | 12.7 degrees | 98 |
| | | 15:12 | SOWLIN | Window Width With Linear Phase Advance | 28.2 degrees | 15 |
| 83 | 19 | 0 | PCDLY | Post Coast delay 0 = 100 ms, 1 = 500 ms | 500 ms | 1 |
| | | 1 | STBYDIS | Standby Mode 0 = Enable, 1 = Disable | 1 | 1 |
| | | 3:2 | PWMF | Motor PWM Selection | 24/48 kHz | 2 |
| | | 5:4 | BEMFFILT | Bemf comp filter | 4 µs | 0 |
| | | 6 | TCENB | Temperature Compensation 0: Off, 1:On | 0 | 0 |
| | | 8:7 | WINDM | Windmill Option | 0 | 0 |
| | | 12:9 | SPDCLP | Minimum clamp is speed control mode | 4.6% | 2 |
| | | 14:13 | PHARNG | 0: > 32 kRPM, 1: 16-32 kRPM, 2: 8-16 kRPM, 3: < 8 kRPM | 8-16 kRPM | 2 |
| | | 15 | OCLOPT | 0 = Cycle by cycle, 1: Reduce demand | 1 | 1 |
| 84 | 20 | 0 | CL | Speed Control Mode 0 = Open Loop, 1 = Closed | Enabled | 1 |
| | | 1 | PHA | Running Mode 0 = Auto, 1=Linear Phase Advance | 0 | 0 |
| | | 2 | LOCKEVT | Rd Function Mode select | 0 | 0 |
| | | 3 | SPDSEL | Speed Control Select 0 = PWM Duty, 1 = Analog | 0 | 0 |
| | | 6:4 | PP | Pole Pair = PP + 1 | 2 pp | 1 |
| | | 7 | NOCOAST | 1 = NOCOAST, 0 = Coast | No coast | 1 |
| | | 8 | ALIGNMODE | 0 = Align, 1 = One Cycle | Align | 0 |
| | | 9 | QCKSTRT | 0 = Disable, 1 = Enable | disable | 0 |
| | | 10 | OVPOPT | 0 = Disable, 1 = Lock detect | TLOCK | 1 |
| | | 11 | FGSTRT | 0 = FG disabled during Startup, 1 = FG Enabled | 0 | 0 |
| | | 13:12 | BEMFHYS | Bemf Hys Level for Startup | 40 mV | 1 |
| | | 14 | SOWAUTO | Initial Value of Window | 21° | 1 |
| | | 15 | OCPOPT | 0 = Reset after TLOCK, 1 = After PWM on/off | TLOCK | 0 |
| 85 | 21 | 7:0 | KP | Closed Loop | 16 | 16 |
| | | 15:8 | KI | Closed Loop | 2 | 2 |
| 86 | 22 | 7:0 | SLPSWDTY | Duty at which slope changes | Disabled | 0 |
| | | 14:8 | TRAPSWDTY | Duty to switch to trap | Disabled | 0 |
| | | 15 | TRAPENB | 1 = Enable | Disabled | 0 |
| 87 | 23 | 14:0 | SLPSWRPM | Range 0 to 16384, LSB = 1 RPM | Disabled | 0 |
| 88 | 24 | 13:0 | SPDSLP2 | Calculated Slope | 0 | 0 |
| | | 15:14 | Unused | | | |

*Continued on next page...*



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## EEPROM MAP (continued)

| I²C Register | EEPROM Address | Bits | Name | Description | Default Setting | Default Value (decimal) |
|---|---|---|---|---|---|---|
| 89 | 25 | 0 | DUTYINV | 0 = Normal, 1 = Invert | 0 | 0 |
| | | 1 | MAXDTYOPT | 0 = Run at Open Loop, 1 = Run at MAXDTYCLP | 0 | 0 |
| | | 2 | ONOFFCNTL | 0 = Normal hysteretic on/off , 1 = Motor Off between DC_ON and DC_OFF | 0 | 0 |
| | | 3 | DIR50 | 1 = enable direction change based on 50% duty | 0 | 0 |
| | | 4 | REVOPT | 1 = reverse when duty < dc_off and ONOFFCNTL = 1 | 0 | 0 |
| | | 5 | BRKOFF | 0 = Coast, 1 = Brake when PWM off state after $t_{COAST}$ | 0 | 0 |
| | | 6 | n/a | Set bit to 0 | 0 | 0 |
| | | 8:7 | PIOPT | 0 = 1×, 1 = 2×, 2 = 4×, 4 = 8× | 0 | 0 |
| | | 15:9 | Unused | | | |
| 90 | 26 | 7:0 | TCOAST | Coast time for brake or direction change | 3 s | 30 |
| | | 15:8 | OPNLPMAX | Max speed limit for open loop mode | 30208 | 118 |
| 91 | 27 | 11:0 | MINSPD | Minimum Speed (y intercept) | 1000 | 1000 |
| | | 13:12 | OVPSEL | 18/28/38/48 V | 28 | 1 |
| | | 14 | VBBRNG | 0 = 24 V, 1 = 48 V | 24 | 0 |
| | | 15 | Unused | | | |
| 92 | 28 | 13:0 | SPDSLP1 | Calculated Slope of Speed Curve | 1378 | 1378 |
| | | 15:14 | Unused | | | |
| 93 | 29 | 7:0 | DCON | Range = 0 to 49.9%, LSB = 0.2% | 10% | 51 |
| | | 15:8 | DCOFF | Range = 0 to 49.9%, LSB = 0.2% | 7.4% | 38 |
| 94 | 30 | 3:0 | DT | Deadtime | 480 ns | 10 |
| | | 4 | VDSTH | OCP VDS Threshold 0 = 1 V, 1 = 2 V | 1 V | 0 |
| | | 5 | OCPDIS | OCP Disable 0 = Enabled, 1 = Disabled | Enabled | 0 |
| | | 7:6 | n/a | Allegro Reserved – set to 0 | n/a | 0 |
| | | 15:8 | n/a | Allegro Reserved – set to 0x59 | n/a | 89 |
| 95 | 31 | 15:0 | n/a | Allegro Reserved | n/a | n/a |



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## SERIAL PORT CONTROL OPTION

Normally, the IC is controlled by duty cycle input and uses the EEPROM data that is stored to create the speed curve profile. However, it is possible to use direct serial port control to avoid programming EEPROM.

When using direct control, the input duty cycle command is replaced by writing a 9-bit number to register 165.

Example:

REGADDR[data]: (in decimal)

165[511] → Duty = 100%

165[102] → Duty = 102 / 511 = 20%

Upon power up, the IC defaults to duty cycle input mode. To use serial port mode, the internal registers should be programmed before turning the part on. The sequence to use serial port mode is:

1. Drive FG and SPD pins low. *
2. Power-up IC.
3. Program registers for parameter setting that correspond to each of the EEPROM memory locations.
   A. REGADDR = 64 + EEPROM ADDR.
   B. Program register addresses 72 to 94 corresponding to EEPROM addresses 8 to 30.
   C. It may be helpful to use the GUI text file to help define the hex data for each of the EEPROM addresses.
4. Write to register 165 to start motor.

* Note: If SPD is not driven low before power up, motor will try to start immediately as the default high value will demand 100% on signal.



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## Serial Port

The A5932 uses standard fast mode I²C serial port format to program the EEPROM or to control the IC speed serially. The SPD pin functions as the clock (SCL) input, and the FG pin is the data line (SDA). No special sequence is needed to begin transferring data. If the motor is running, the FG pin may then pull the data line low while trying to initialize into serial port mode. Once an I²C command is sent, the SPD input is ignored and the motor will turn off as if a PWM duty command of 0% was sent.

The A5932 7-bit slave address is 0x55.

## I²C Timing Diagrams

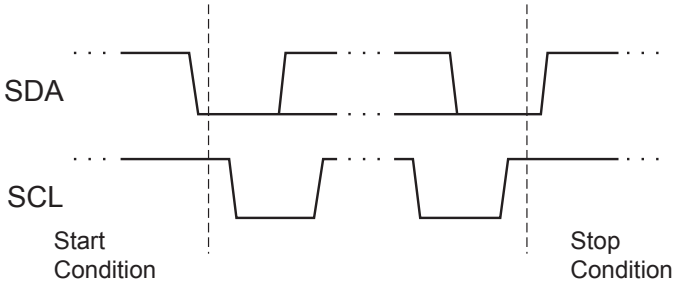


**Figure 6: Start and Stop Conditions**

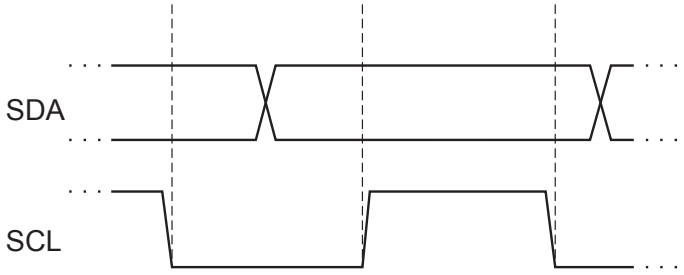


**Figure 7: Clock and Data Bit Synchronization**

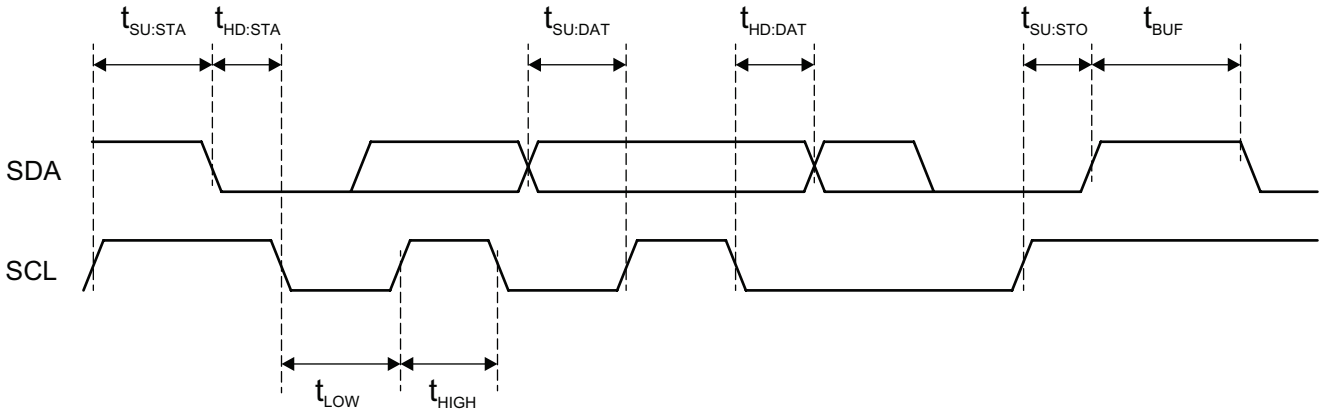


**Figure 8: I²C-Compatible Timing Requirements**



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## Write Command

1. Start Condition
2. 7-bit I²C Slave Address (Device ID) 1010101, R/W Bit = 0
3. Internal Register Address
4. 2 data bytes, MSB first
5. Stop Condition

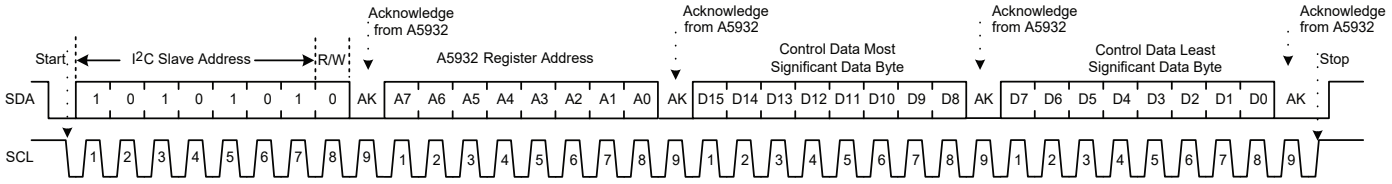


**Figure 9: Write Command**

## Read Command

1. Start Condition
2. 7-bit I²C Slave Address (Device ID) 1010101, R/W Bit = 0
3. Internal Register Address to be read
4. Stop Condition
5. Start Condition
6. 7-bit I²C Slave Address (Device ID) 1010101, R/W Bit = 1
7. Read 2 data bytes
8. Stop Condition

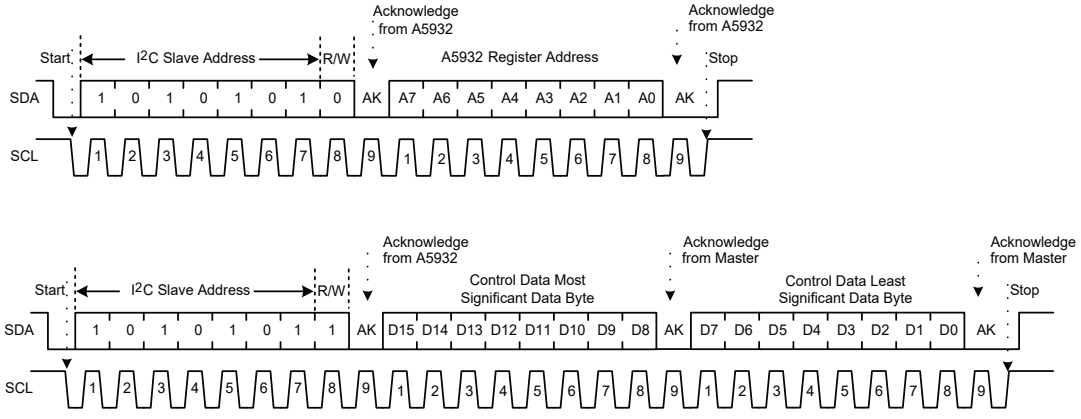


**Figure 10: Read Command**



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## Programming EEPROM

The A5932 contains 32 words of 16-bit length. The EEPROM is controlled with the following I²C registers. Refer to application note for EEPROM definition.

**Table 3: EEPROM Control – Register 161 (Used to control programming of EEPROM)**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RD | WR | ER | EN |

| Bit | Name | Description |
|---|---|---|
| 0 | EN | Set EEPROM voltage required for writing or erasing |
| 1 | ER | Sets mode to erase |
| 2 | WR | Sets mode to write |
| 3 | RD | Sets mode to read |
| 15:4 | n/a | Do not use; always set to zero during programming process |

**Table 4: EEPROM Address – Register 162 (Used to set the EEPROM address to be altered)**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | eeADDRESS | | | | |

| Bit | Name | Description |
|---|---|---|
| 4:0 | eeADDRESS | Used to specify EEPROM address to be changed. |
| 15:5 | n/a | Do not use; always set to zero during programming process |

**Table 5: EEPROM DataIn – Register 163 (Used to set the EEPROM new data to be programmed)**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| eeDATAin | | | | | | | | | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 15:0 | eeDATAin | Used to specify the new EEPROM data to be changed |



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**Table 6: DataOUT – Register 164 (Used for read operations)**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| eeDATAout | | | | | | | | | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 15:0 | eeDATAout | Used to readback EEPROM data from address defined in register 162 |

There are 3 basic commands: Read, Erase, and Write. To change the contents of a memory location, the word must be first erased. The EEPROM programming process (writing or erasing) takes 10 ms per word.

Each word must be written individually.

Example #1: Write EEPROM address 5 to 261 (0x0105)

1) Erase the word

| | | |
|---|---|---|
| | I²C Write REGADDR[Data] | ; comment |
| a. | 162[5] | ; set EEPROM address to erase |
| b. | 163[0] | ; set 0000 as Data In |
| c. | 161[3] | ; set control to Erase and trigger high-voltage pulse |
| d. | Wait 15 ms | ; wait for pulse to end |
| e. | 161[0] | ; clear voltage |

2) Write the new data

| | | |
|---|---|---|
| a. | 162[5] | ; set EEPROM address to write |
| b. | 163[261] | ; set Data In = 261 |
| c. | 161[5] | ; set control to Write and trigger high-voltage pulse |
| d. | Wait 15 ms | ; wait for pulse to end |
| e. | 161[5] | ; clear voltage |

Example #2: Read EEPROM address 5 to confirm correct data properly programmed

1) Read the word

| | | |
|---|---|---|
| a. | 5[I²C Read] | ; read register 5; this will be the contents of EEPROM |



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## PIN DIAGRAMS

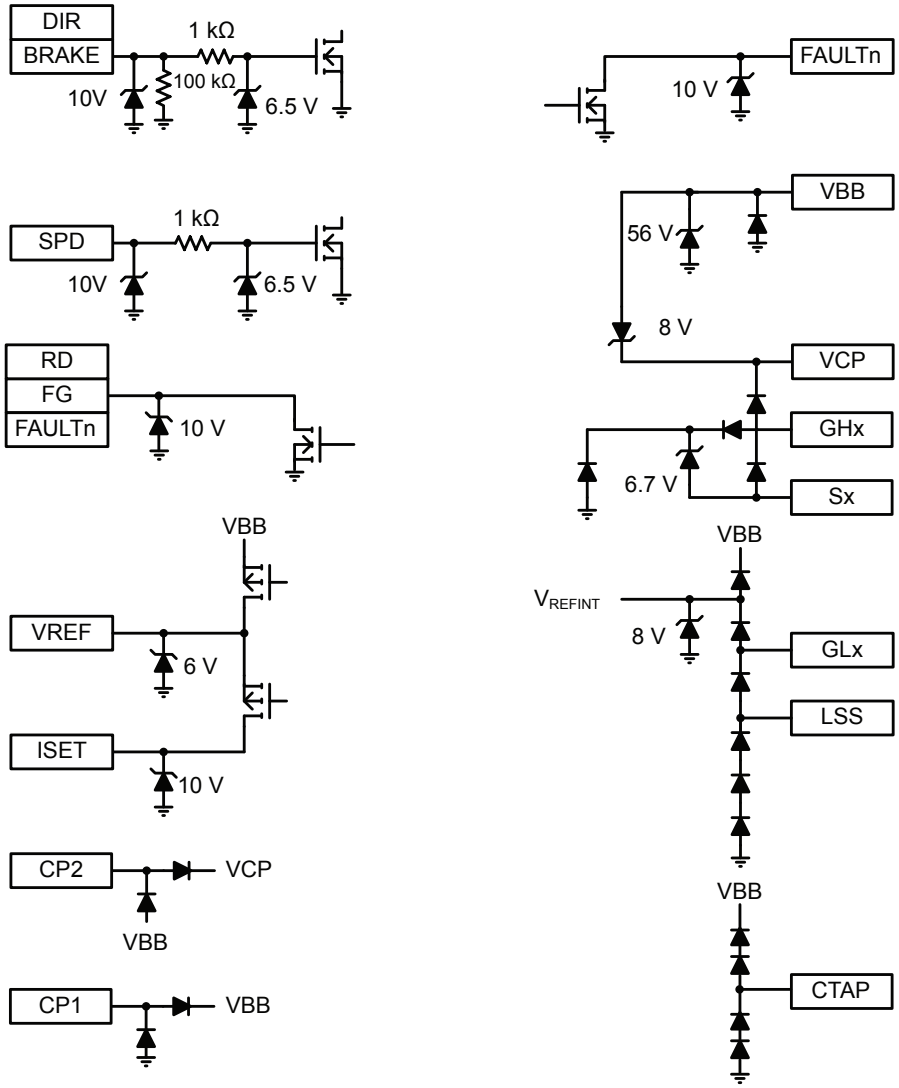


**Figure 11: Pin Diagrams**



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## PACKAGE OUTLINE DRAWING

**For Reference Only – Not for Tooling Use**

Reference Allegro DWG-2871 (Rev. A) or JEDEC MO-220WGGD-11.
Dimensions in millimeters – NOT TO SCALE.
Exact case and lead configuration at supplier discretion within limits shown.

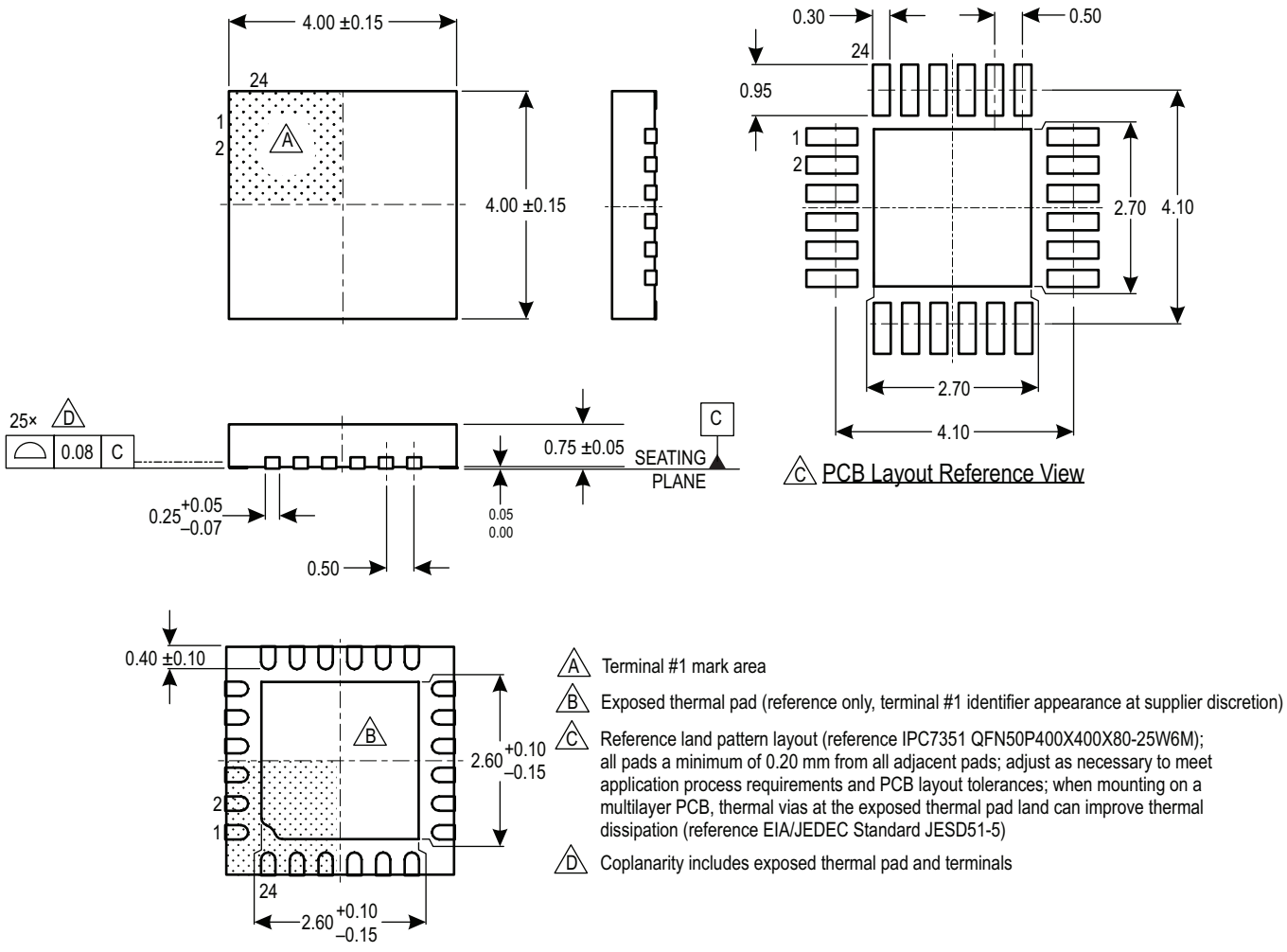


**Figure 12: Package ES, 24-Contact QFN with Exposed Pad**



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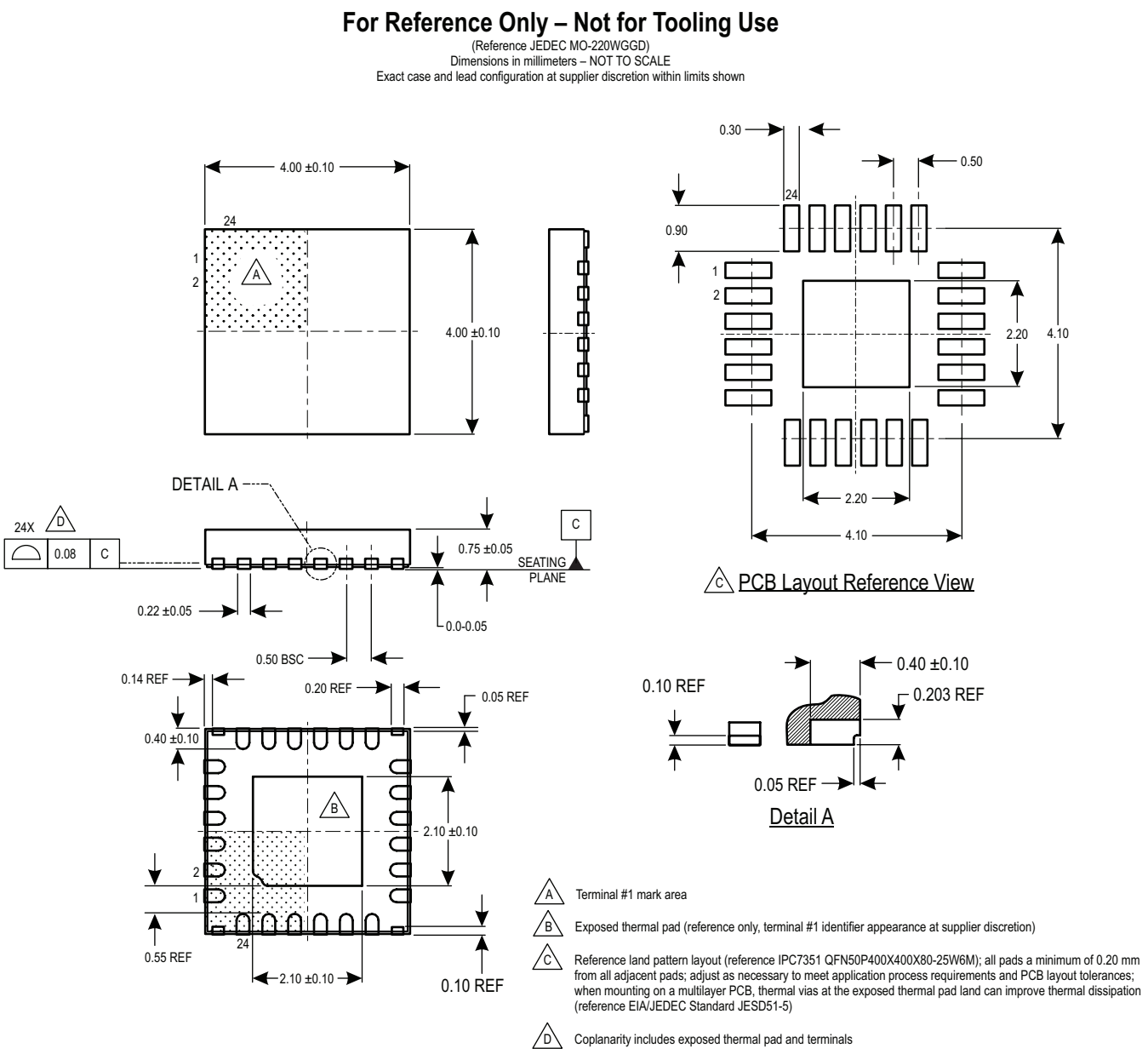


**Figure 13: Package ES, -J option, 24-Contact QFN Wettable Flank with Exposed Pad**



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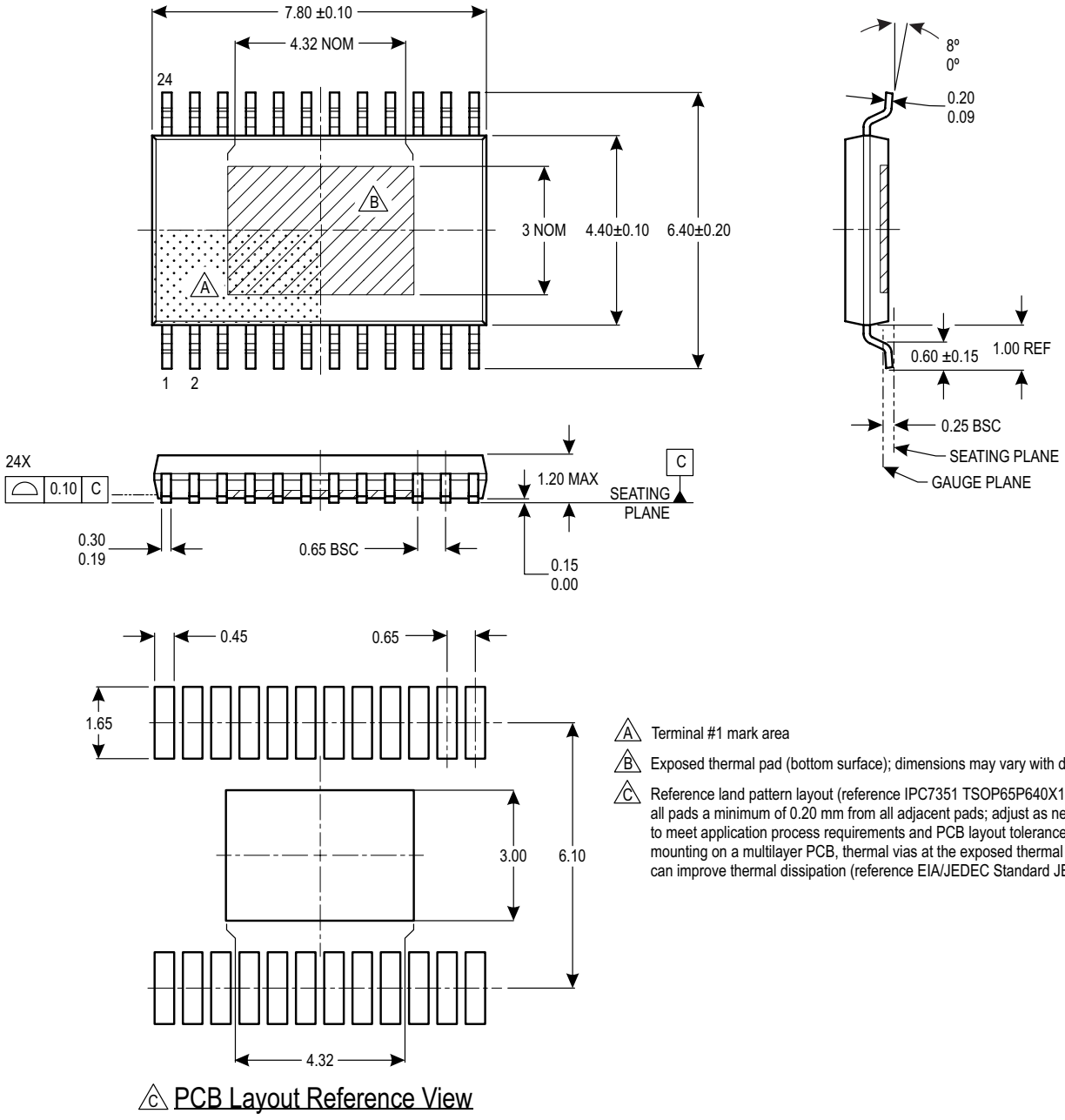
(Reference MO-153 ADT)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown




A Terminal #1 mark area

B Exposed thermal pad (bottom surface); dimensions may vary with device

C Reference land pattern layout (reference IPC7351 TSOP65P640X120-25M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

**Figure 14: Package LP, 24-Lead TSSOP with Exposed Pad**



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## Revision History

| Number | Date | Description |
|---|---|---|
| – | June 19, 2017 | Initial release |
| 1 | December 12, 2017 | Added automotive temperature range part variant, wettable flank package option |
| 2 | October 24, 2018 | Updated PWM Input Frequency Range min value (page 5), FG and SPD functional description sections (page 8); minor editorial updates |
| 3 | November 2, 2018 | Updated PWM Input Frequency Range (page 5), VREG, BRAKE, and DIR functional description sections (page 8); added Thermal Shutdown functional description (page 9); minor editorial updates |
| 4 | November 15, 2018 | Updated VREF and SPD functional description sections (page 8). |
| 5 | July 25, 2019 | Minor editorial updates; initial release to web |





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