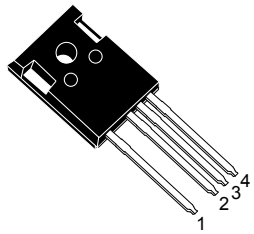
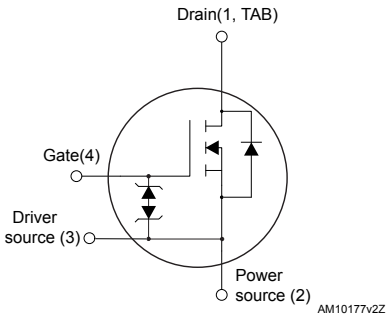
# N-channel 600 V, 32 mΩ typ., 72 A, MDmesh™ M6 Power MOSFET in a TO247-4 package




**TO247-4**




## Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ |
|---|---|---|---|
| STW75N60M6-4 | 600 V | 36 mΩ | 72 A |

- Reduced switching losses
- Lower $R_{DS(on)}$ per area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected
- Excellent switching performance thanks to the extra driving source pin

## Applications

- Switching applications
- LLC converters
- Boost PFC converters

## Description

The new MDmesh™ M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent $R_{DS(on)}$ per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.

| Product status link |
|---|
| STW75N60M6-4 |

| Product summary | |
|---|---|
| **Order code** | STW75N60M6-4 |
| **Marking** | 75N60M6 |
| **Package** | TO247-4 |
| **Packing** | Tube |

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{GS}$ | Gate-source voltage | ±25 | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 72 | A |
| | Drain current (continuous) at $T_C$ = 100 °C | 45 | A |
| $I_{DM}$(1) | Drain current (pulsed) | 288 | A |
| $P_{TOT}$ | Total power dissipation at $T_C$ = 25 °C | 446 | W |
| dv/dt(2) | Peak diode recovery voltage slope | 15 | V/ns |
| dv/dt(3) | MOSFET dv/dt ruggedness | 100 | |
| $T_{stg}$ | Storage temperature range | -55 to 150 | °C |
| $T_J$ | Operating junction temperature range | | |

1. *Pulse width is limited by safe operating area.*
2. *$I_{SD}$ ≤ 72 A, di/dt = 400 A/µs, $V_{DS(peak)}$ < $V_{(BR)DSS}$, $V_{DD}$ = 400 V*
3. *$V_{DS}$ ≤ 480 V*

**Table 2. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case | 0.28 | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient | 50 | °C/W |

**Table 3. Avalanche characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive (pulse width limited by $T_{Jmax}$) | 11 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_J$ = 25 °C, $I_D$ = $I_{AR}$, $V_{DD}$ = 50 V) | 1.4 | J |

# 2 Electrical characteristics

($T_C$ = 25 °C unless otherwise specified)

**Table 4. On/off-states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0 V, $I_D$ = 1 mA | 600 | | | V |
| $I_{DSS}$ | Zero-gate voltage drain current | $V_{GS}$ = 0 V, $V_{DS}$= 600 V | | | 1 | µA |
| | | $V_{GS}$ = 0 V, $V_{DS}$ = 600 V, $T_C$ = 125 °C(1) | | | 100 | |
| $I_{GSS}$ | Gate-body leakage current | $V_{DS}$ = 0 V, $V_{GS}$ = ±25 V | | | ±5 | µA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 3.25 | 4 | 4.75 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 36 A | | 32 | 36 | mΩ |

1. *Defined by design, not subject to production test.*

**Table 5. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 100 V, f = 1 MHz | - | 4850 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 380 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 3.5 | - | pF |
| $C_{oss\ eq.}$ (1) | Equivalent output capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 0 to 480 V | - | 851 | - | pF |
| $R_G$ | Intrinsic gate resistance | f = 1 MHz open drain | - | 1.5 | - | Ω |
| $Q_g$ | Total gate charge | $V_{DD}$ = 480 V, $I_D$ = 72 A, $V_{GS}$ = 0 to 10 V (see Figure 2) | - | 106 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 32 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 45 | - | nC |

1. *$C_{oss\ eq.}$ is defined as the constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$.*

**Table 6. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 300 V, $I_D$ = 36 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see Figure 1 and Figure 6) | - | TBD | - | ns |
| $t_r$ | Rise time | | - | TBD | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | TBD | - | ns |
| $t_f$ | Fall time | | - | TBD | - | ns |

**Table 7. Source-drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 72 | A |
| $I_{SDM}$ (1) | Source-drain current (pulsed) | | - | | 288 | A |
| $V_{SD}$ (2) | Forward on voltage | $V_{GS}$ = 0 V, $I_{SD}$ = 72 A | - | | 1.6 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 72 A, di/dt = 100 A/µs, $V_{DD}$ = 60 V (see Figure 3) | - | 367 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 6.4 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 35 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 72 A, di/dt = 100 A/µs, $V_{DD}$ = 60 V, $T_J$ = 150 °C (see Figure 3) | - | 552 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 13.7 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 49.6 | | A |

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

## 2.1 Electrical characteristics (curves)

**Figure 1. Safe operating area**

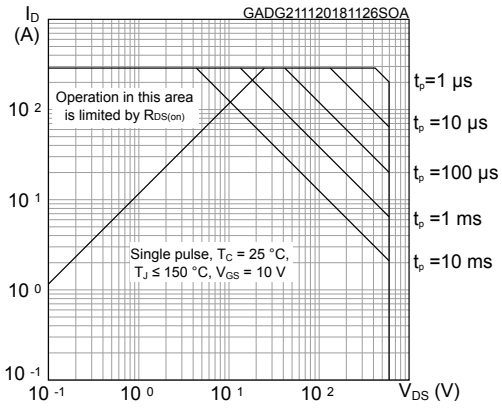



**Figure 2. Thermal impedance**

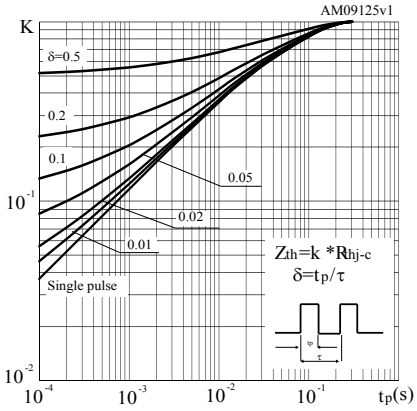



**Figure 3. Output characteristics**

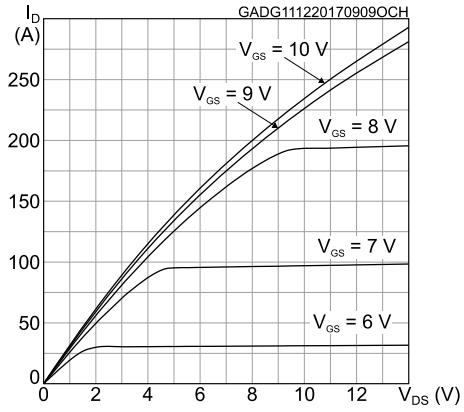



**Figure 4. Transfer characteristics**

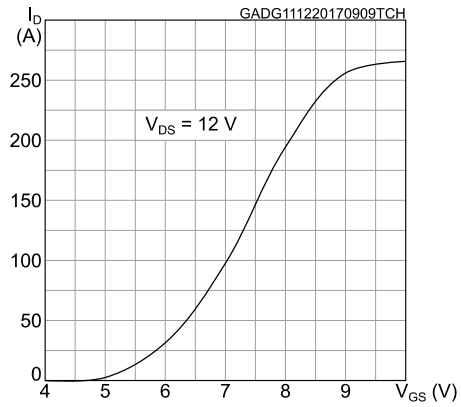



**Figure 5. Gate charge vs gate-source voltage**

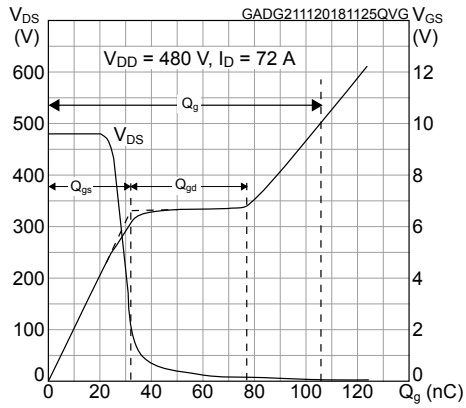



**Figure 6. Static drain-source on-resistance**

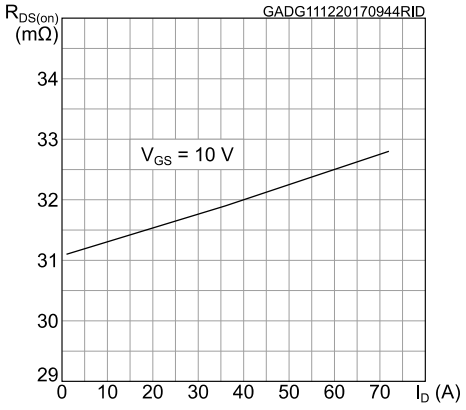


**Figure 7. Normalized on-resistance vs temperature**

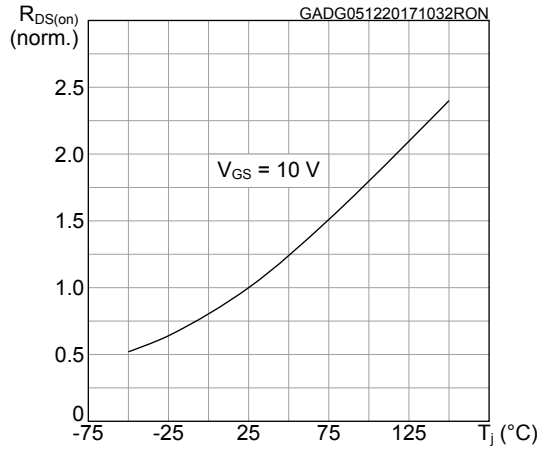



**Figure 8. Normalized $V_{(BR)DSS}$ vs temperature**

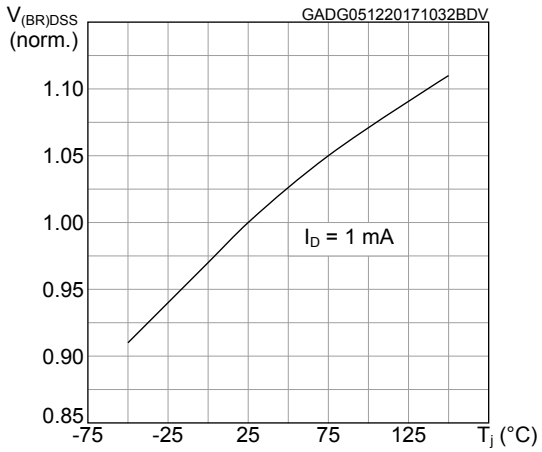



**Figure 9. Capacitance variations**

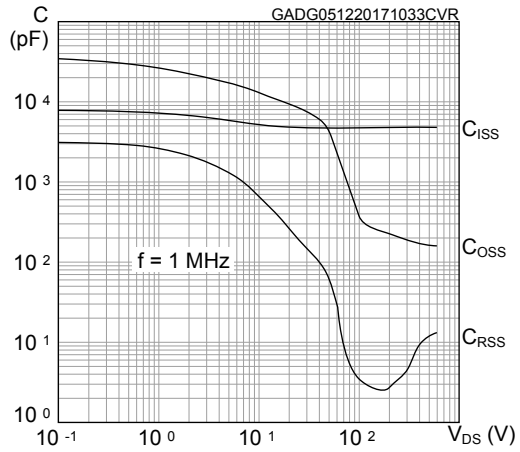



**Figure 10. Normalized gate threshold voltage vs temperature**

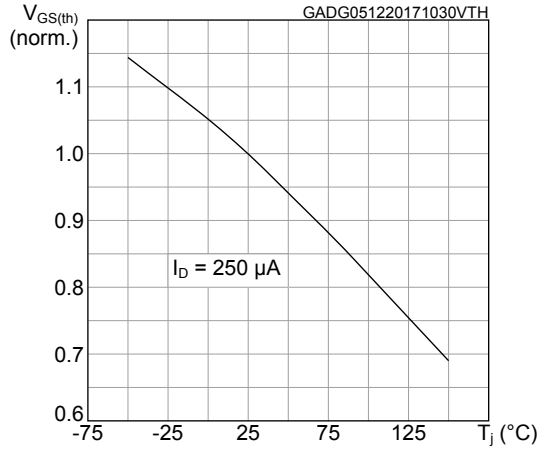



**Figure 11. Output capacitance stored energy**

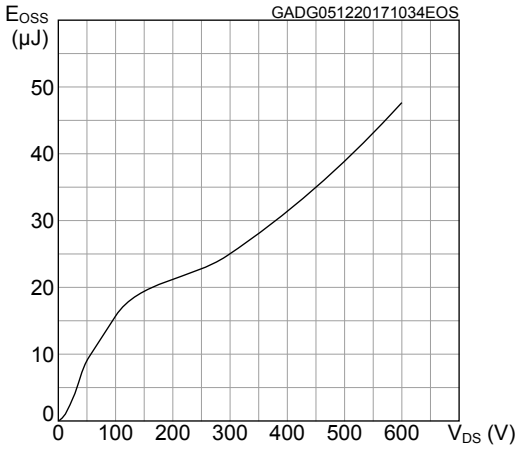
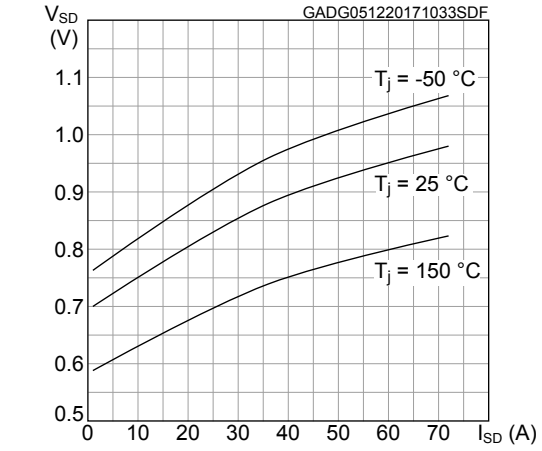



**Figure 12. Source-drain diode forward characteristics**



# 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**

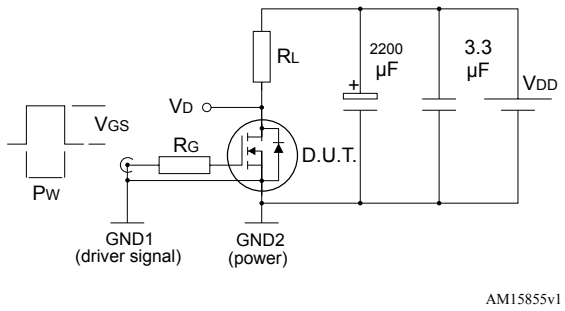



**Figure 14. Test circuit for gate charge behavior**

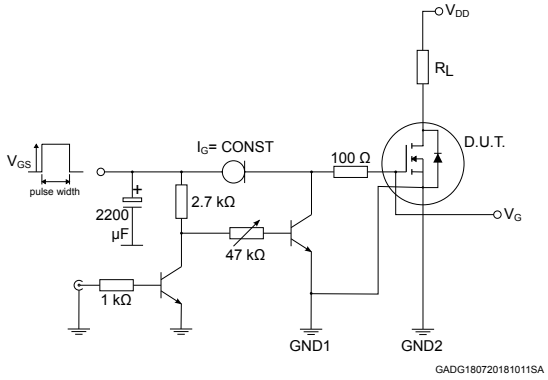



**Figure 15. Test circuit for inductive load switching and diode recovery times**

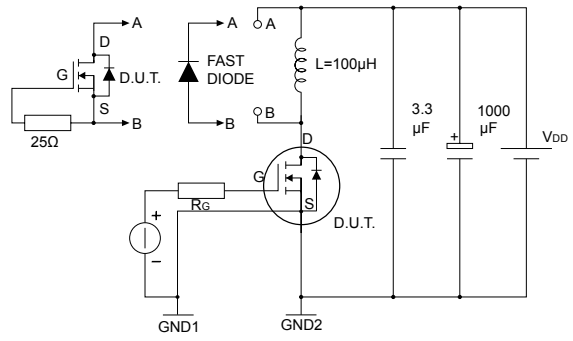



**Figure 16. Unclamped inductive load test circuit**

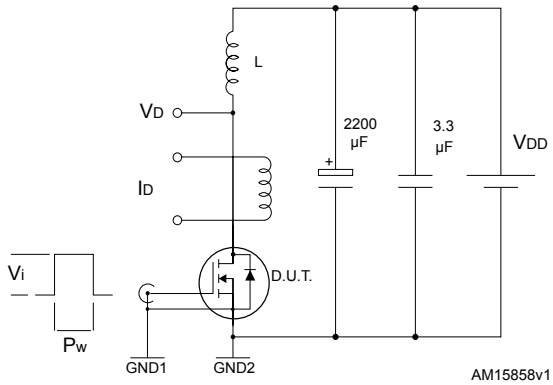



**Figure 17. Unclamped inductive waveform**

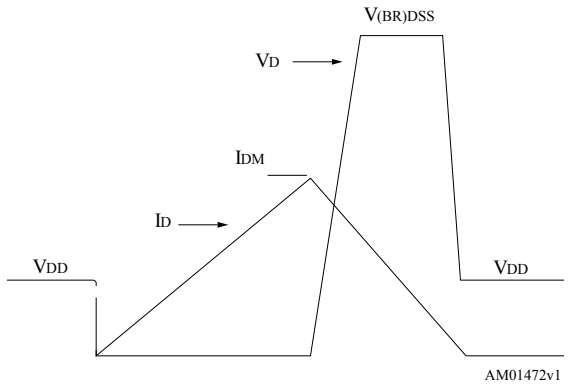
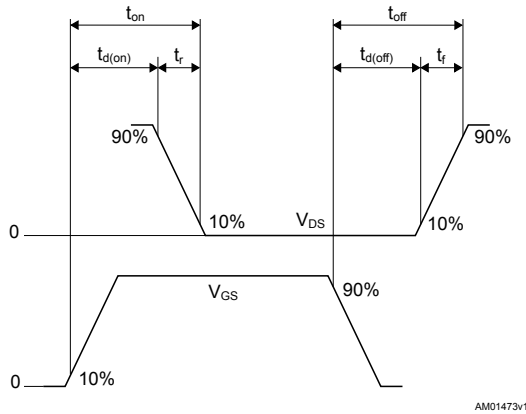



**Figure 18. Switching time waveform**



# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

## 4.1 TO247-4 package information

**Figure 19. TO247-4 package outline**

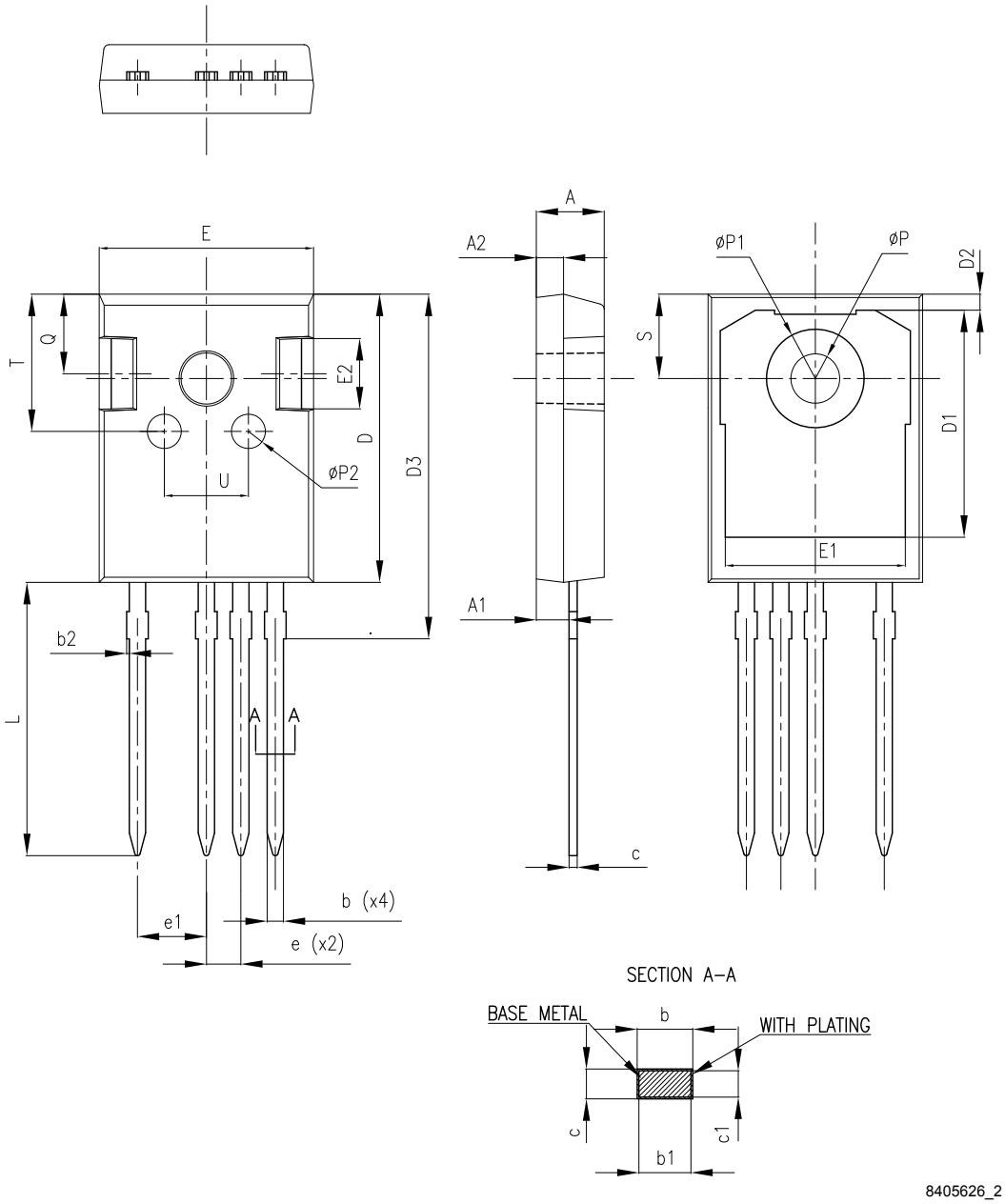


Table 8. **TO247-4 mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 4.90 | 5.00 | 5.10 |
| A1 | 2.31 | 2.41 | 2.51 |
| A2 | 1.90 | 2.00 | 2.10 |
| b | 1.16 | | 1.29 |
| b1 | 1.15 | 1.20 | 1.25 |
| b2 | 0 | | 0.20 |
| c | 0.59 | | 0.66 |
| c1 | 0.58 | 0.60 | 0.62 |
| D | 20.90 | 21.00 | 21.10 |
| D1 | 16.25 | 16.55 | 16.85 |
| D2 | 1.05 | 1.20 | 1.35 |
| D3 | 24.97 | 25.12 | 25.27 |
| E | 15.70 | 15.80 | 15.90 |
| E1 | 13.10 | 13.30 | 13.50 |
| E2 | 4.90 | 5.00 | 5.10 |
| E3 | 2.40 | 2.50 | 2.60 |
| e | 2.44 | 2.54 | 2.64 |
| e1 | 4.98 | 5.08 | 5.18 |
| L | 19.80 | 19.92 | 20.10 |
| P | 3.50 | 3.60 | 3.70 |
| P1 | | | 7.40 |
| P2 | 2.40 | 2.50 | 2.60 |
| Q | 5.60 | | 6.00 |
| S | | 6.15 | |
| T | 9.80 | | 10.20 |
| U | 6.00 | | 6.40 |

## Revision history

Table 9. **Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 11-Dec-2017 | 1 | Initial version |
| 07-Dec-2018 | 2 | Removed maturity status indication from cover page. The document status is production data.<br>Updated schematic diagram on cover page.<br>Updated Table 1. Absolute maximum ratings, Table 5. Dynamic and Table 7. Source-drain diode.<br>Updated Section 2.1 Electrical characteristics (curves).<br>Minor text changes |

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