



## Product Change Notification / SYST-29FUUCT634

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### Date:

02-Aug-2022

### Product Category:

Ethernet Switches

### PCN Type:

Document Change

### Notification Subject:

Data Sheet - KSZ9893R 3-Port Gigabit Ethernet Switch with RGMII/MII/RMII Interface - Data Sheet Revision

### Affected CPNs:

[SYST-29FUUCT634\\_Affected\\_CPN\\_08022022.pdf](#)  
[SYST-29FUUCT634\\_Affected\\_CPN\\_08022022.csv](#)

### Notification Text:

SYST-29FUUCT634

Microchip has released a new Datasheet for the KSZ9893R 3-Port Gigabit Ethernet Switch with RGMII/MII/RMII Interface - Data Sheet of devices. If you are using one of these devices please read the document located at [KSZ9893R 3-Port Gigabit Ethernet Switch with RGMII/MII/RMII Interface - Data Sheet](#).

**Notification Status:** Final

**Description of Change:** Revision includes:

Section 4.1.7, "Auto-Negotiation" Updated description from "mode" to "speed." Also added the following sentence: "With parallel detection, the duplex will always be half-duplex."

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Section 4.1.8, "LinkMD® Cable Diagnostics" Updated to add additional details and test script.

Section 4.10.1, "Media Independent Interface (MII)" Updated description to remove half duplex operation.

Section 5.1.2.2, "In-Band Management (IBA) Control Register" Added the following note to bit 31: "If using I2C, do not enable IBA."

Section 5.1.3.2, "LED Strap-In Register" Changed definition from: "Strap-in values of Select RXD and LED pins [RXD2\_1, RXD2\_0, LED1\_1, LED1\_0]" to "Strap-in values of Select RXD and LED pins [RXD1, RXD0, LED1\_1, LED1\_0]".

Section 5.1.4.69, "Global PM Available Register" New register added for Packet Memory Available Block Count.

Section 5.1.5.3, "VLAN Table Entry 2 Register" Updated description of bits 2-0 from "1 = Untag packets upon egress at this port; 0 = Do not untag upon egress at this port" to "1 = Forward to this port; 0 = Do not forward to this port".

Section 5.2.2.1, "PHY Basic Control Register" Updated bit 7 from "Collision Test" to "Reserved".

Section 5.2.2.1, "PHY Basic Control Register" Updated bit 10 default value from "0b" to "1b".

Section 5.2.2.2, "PHY Basic Status Register" Updated bit 0 default from "0" to "1".

Section 5.2.2.4, "PHY ID Low Register" Updated value from "0x1631" to "0x1637".

Section 5.2.2.20, "PHY Auto MDI / MDI-X Register" Updated Reserved bit (15:8) default value from "0x00" to "0x24".

Section 5.2.2.21, "Port Special Register" Added register.

Section 5.2.7.4, "Port Authentication Control Register" Updated bit 2 definition from "1 = Enable; 0 = Enable" to "1 = Enable; 0 = Disable".

Section 5.2.9.2, "Port Control 1 Register" Updated address range from "0xNA04 - 0xNA03" to "0xNA04 - 0xNA07". Updated type from "RO" to "RW". Updated default value of bits 2-0 from "0b" to "1b".

Section 5.2.9.3, "Port Transmit Queue Memory Register" Added register.

Section 5.4.1, "MMD LED Mode Register" Added the following text to bit 4: "For Single-LED mode, set this bit and also set bit 9 in register 0xN13C-0xN13D."

Table 5-7, "MMD Register Map" Updated example of MMD Register Read from: "Register 11h - 13h for the LED mode status" to "Register 00h for the MMD LED Mode Register."

Table 3-3, "Configuration Strap Descriptions" Added the following note to LED1\_1: "If using I2C, do not enable IBA."

Table 4.7.5, "Energy Efficient Ethernet (EEE)" Corrected "disabled by default" to "enabled by default". Additionally, added the following sentence: "EEE is enabled or disabled in the MMD EEE Advertisement register."

Table 4-5, "Tail Tag Frame Format" Updated byte number for Tail Tagging from "2" to "1".

Table 3-2, "Pin Descriptions" For Power Management Event PME\_N, updated buffer type from "IPU/O8" to "I/O8" and added the following note: "An external pull-up or pull-down resistor is required to set the desired strapping level."

Table 3-2, "Pin Descriptions" Updated pin RX\_ER so that RMII mode is with MII mode.

Table 3-3, "Configuration Strap Descriptions" Updated RX\_ER, PME\_N description to remove "Default" from bit 1 and added the following note: "Note that PME\_N does not have an internal pullup or pull-down, so an external pull-up or pull-down resistor is always required."

Table 6-11, "Power-up and Reset Timing Values" Updated Note 3 to indicate the following: "The power supplies may be powered down in any sequence."

**Impacts to Data Sheet:** See above details.  
**Reason for Change:** To Improve Productivity  
**Change Implementation Status:** Complete

**Date Document Changes Effective:** 02 August 2022

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

**Markings to Distinguish Revised from Unrevised Devices:** N/A

## Attachments:

[KSZ9893R 3-Port Gigabit Ethernet Switch with RGMII/MII/RMII Interface - Data Sheet](#)

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Affected Catalog Part Numbers (CPN)

KSZ9893RNXC

KSZ9893RNXI

KSZ9893RNXC-TR

KSZ9893RNXI-TR