WIDEBAND, LOW NOISE, LOW DISTORTION FULLY DIFFERENTIAL AMPLIFIER WITH RAIL-TO-RAIL OUTPUTS

FEATURES

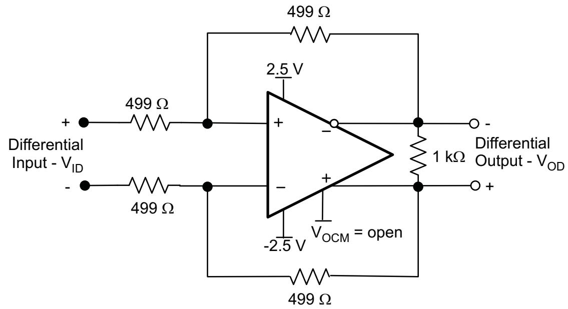
- **Fully Differential Architecture With Rail-to-Rail Outputs**
- **Centered Input Common-mode Range**
- **Minimum Gain of 1 V/V (0 dB)**
- **Bandwidth: 620 MHz**
- **Slew Rate: 570 V/µs**
- **0.1% Settling Time: 7 ns**
- **HD_2: –115 dBc at 100 kHz, V_{OD} = 8 V_{PP}**
- **HD_3: –123 dBc at 100 kHz, V_{OD} = 8 V_{PP}**
- **Input Voltage Noise: 2 nV/$\sqrt{Hz}$ (f >10 kHz)**
- **Output Common-Mode Control**
- **Power Supply:**
  - **Voltage: 3.3 V (±1.65 V) to 5 V (±2.5 V)**
  - **Current: 14.2 mA**
- **Power-Down Capability: 15 µA**

APPLICATIONS

- **5-V and 3.3-V Data Acquisition Systems**
- **High Linearity ADC Amplifier**
- **Wireless Communication**
- **Test and Measurement**
- **Voice Processing Systems**

RELATED PRODUCTS

Device	BW (MHZ)	Slew Rate (V/µsec)	THD (dBc)	V_N (nV/Hz)
THS4509	2000	6600	-102 at 10 MHz	1.9
THS4500	370	2800	-82 at 8 MHz	7
THS4130	150	52	-97 at 250 kHz	1.3



DESCRIPTION

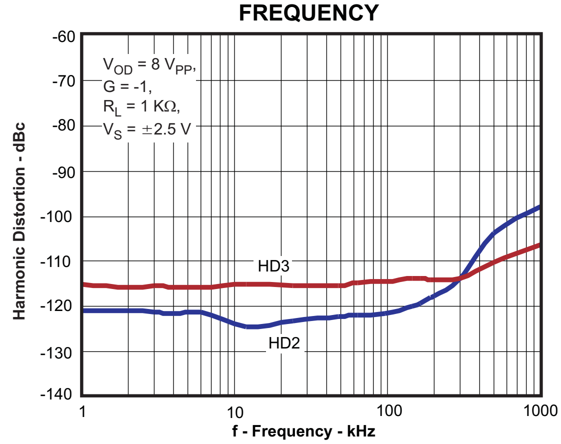
The THS4520 is a wideband, fully differential operational amplifier designed for 5-V data acquisition systems. It has very low noise at 2 nV/$\sqrt{Hz}$, and low harmonic distortion of –115 dBc HD_2 and –123 dBc HD_3 at 100 kHz with 8 V_{PP}, and 1-kΩ load. The slew rate is 570 V/µs, and with a settling time of 7 ns to 0.1% (2-V step), it is ideal for data acquisition applications. It is designed for unity gain stability.

To allow for dc coupling to ADCs, its unique output common-mode control circuit maintains the output common-mode voltage within 0.25 mV offset (typical) from the set voltage. The common-mode set point defaults to mid-supply by internal circuitry, which may be over-driven from an external source.

The input and output are optimized for best performance with their common-mode voltages set to mid-supply. Along with high performance at low power supply voltage, this makes for extremely high performance single supply 5-V and 3.3-V data acquisition systems.

The THS4520 is offered in a Quad 16-pin leadless QFN package (RGT), and is characterized for operation over the full industrial temperature range from –40°C to 85°C.

THS4520
HARMONIC DISTORTION
vs
FREQUENCY



Measured HD2/HD3 for G = -1, V_{OD} = 8 V_{PP}, R_L = 1 KΩ (circuit shown on the left)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

			UNIT
V_{S-} to V_{S+}	Supply voltage		6 V
V_I	Input voltage		$\pm V_S$
V_{ID}	Differential input voltage		4 V
I_O	Output current(1)		200 mA
	Continuous power dissipation		See Dissipation Rating Table
T_J	Maximum junction temperature		150°C
	Maximum junction temperature, continuous operation, long term reliability		125°C
T_A	Operating free-air temperature range		–40°C to 85°C
T_{stg}	Storage temperature range		–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300°C
	ESD ratings	HBM	2000
		CDM	1500
		MM	100

(1) The THS4520 incorporates a (QFN) exposed thermal pad on the underside of the chip. See TI technical brief SLMA002 and SLMA004 for more information about utilizing the QFN thermally enhanced package.

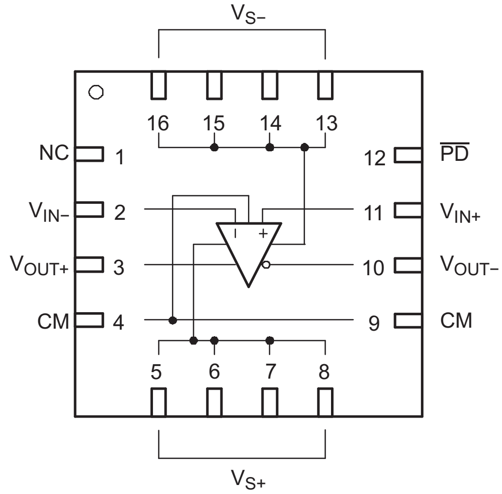
DISSIPATION RATINGS TABLE PER PACKAGE

PACKAGE(1)	θ_{JC}	θ_{JA}	POWER RATING	
			$T_A \leq 25°C$	$T_A = 85°C$
RGT (16)	2.4°C/W	39.5°C/W	2.3 W	225 mW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

DEVICE INFORMATION

RGT Package
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL (RGT PACKAGE)		DESCRIPTION
NO.	NAME	
1	NC	No internal connection
2	V_{IN-}	Inverting amplifier input
3	V_{OUT+}	Non-inverted amplifier output
4, 9	CM	Common-mode voltage input
5, 6, 7, 8	V_{S+}	Positive amplifier power supply input
10	V_{OUT-}	Inverted amplifier output
11	V_{IN+}	Non-inverting amplifier input
12	$\overline{PD}$	Powerdown, $\overline{PD}$ = logic low puts part into low power mode, $\overline{PD}$ = logic high or open for normal operation. If the PD pin is open (unterminated) the device will default to the enabled state.
13, 14, 15, 16	V_{S-}	Negative amplifier power supply input

SPECIFICATIONS; $V_{S+} – V_{S–}$ = 5 V:

Test conditions unless otherwise noted: V_{S+} = +2.5 V, $V_{S–}$ = –2.5 V, G = 0 dB, CM = open, V_O = 2 V_{PP}, R_F = 499 Ω, R_L = 200 Ω Differential, T_A = 25°C Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE								
Small-Signal Bandwidth	G = 0 dB, V_O = 100 mV_{PP}				620		MHz	C
	G = 6 dB, V_O = 100 mV_{PP}				450		MHz	
	G = 10 dB, V_O = 100 mV_{PP}				330		MHz	
	G = 20 dB, V_O = 100 mV_{PP}				120		MHz	
Gain-Bandwidth Product	G = 20 dB				1200		MHz	
Bandwidth for 0.1 dB flatness	G = 6 dB, V_O = 2 V_{PP}				30		MHz	
Large-Signal Bandwidth	G = 6 dB, V_O = 2 V_{PP}				132		MHz	
Slew Rate (Differential)	2-V Step				570		V/μs	C
Rise Time					4		ns	
Fall Time					4			
Settling Time to 1%					6.2			
Settling Time to 0.1%					7			
2nd Order Harmonic Distortion(2)	f = 100 kHz(3)	R_L = 1 kΩ	V_{OD} = 8 V_{PP}		–115		dBc	C
	f = 1 MHz(4)	R_L = 200 Ω	V_{OD} = 2 V_{PP}		–100			
			V_{OD} = 4 V_{PP}		–93			
		R_L = 1 kΩ	V_{OD} = 2 V_{PP}		–101			
			V_{OD} = 4 V_{PP}		–101			
	f = 8 MHz (4)	R_L = 200 Ω	V_{OD} = 2 V_{PP}		–103			
			V_{OD} = 4 V_{PP}		–97			
		R_L = 1 kΩ	V_{OD} = 2 V_{PP}		–100			
			V_{OD} = 4 V_{PP}		–95			
3rd Order Harmonic Distortion(2)	f = 100 kHz(3)	R_L = 1 kΩ	V_{OD} = 8 V_{PP}		–123		dBc	C
	f = 1 MHz (4)	R_L = 200 Ω	V_{OD} = 2 V_{PP}		–105			
			V_{OD} = 4 V_{PP}		–93			
		R_L = 1 kΩ	V_{OD} = 2 V_{PP}		–101			
			V_{OD} = 4 V_{PP}		–96			
	f = 8 MHz (4)	R_L = 200 Ω	V_{OD} = 2 V_{PP}		–92			
			V_{OD} = 4 V_{PP}		–88			
		R_L = 1 kΩ	V_{OD} = 2 V_{PP}		–102			
			V_{OD} = 4 V_{PP}		–91			
3rd Order Intermodulation Distortion	f_C = 100 kHz (3), 10-kHz Tone Spacing, R_L = 1k Ω, V_{OD} = 8 V_{PP} envelope, G = 0dB				–135		dBc	C
	f_C = 1 MHz (4), 100-kHz Tone Spacing, R_L = 200 Ω, V_{OD} = 4 V_{PP} envelope, G = 10dB				-82			
	f_C = 10 MHz (4), 100-kHz Tone Spacing, R_L = 200 Ω, V_{OD} = 4 V_{PP} envelope, G = 10dB				-82			
Input Voltage Noise	f > 10 kHz				2		nV/√Hz	
Input Current Noise	f > 10 kHz				2		pA/√Hz	

(1) Test levels: **(A)** 100% tested at 25°C. Overtemperature limits by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.
(2) For additional information, see the Typical Characteristics section and the Apllications section.
(3) Data collected with applied differential input signal and measured differential output signal.
(4) Data collected with applied single-ended input signal and measured differential output signal. See Figure 55 in the Applications/Test Circuits section for additional information.

SPECIFICATIONS; $V_{S+} - V_{S-}$ = 5 V: (continued)

Test conditions unless otherwise noted: V_{S+} = +2.5 V, V_{S-} = –2.5 V, G = 0 dB, CM = open, V_O = 2 V_{PP}, R_F = 499 Ω, R_L = 200 Ω Differential, T_A = 25°C Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL (1)
DC PERFORMANCE						
Open-Loop Voltage Gain (A_{OL})			112		dB	C
Input Offset Voltage	T_A = 25°C		±0.25	±2.5	mV	A
	T_A = –40°C to 85°C		±0.25	±3	mV	
Average Offset Voltage Drift	T_A = –40°C to 85°C		1		μV/°C	B
Input Bias Current	T_A = 25°C		6.5	10	μA	A
	T_A = –40°C to 85°C		6.4	11		
Average Bias Current Drift	T_A = –40°C to 85°C		1.9		nA/°C	B
Input Offset Current	T_A = 25°C		±0.2	±2.5	μA	A
	T_A = –40°C to 85°C		±0.2	±3		
Average Offset Current Drift	T_A = –40°C to 85°C		1.6		nA/°C	B
INPUT						
Common-Mode Input Range High			1.75		V	B
Common-Mode Input Range Low			–1.3			
Common-Mode Rejection Ratio			84		dB	
Differential Input Impedance			7.5‖0.31		kΩ‖pF	C
Common-Mode Input Impedance			2.67‖0.77		MΩ‖pF	C
OUTPUT						
Maximum Output Voltage High	Each output with 100 Ω to mid-supply, T_A = 25°C	1.95	2.16		V	A
	Each output with 100 Ω to mid-supply, T_A = –40C to 85°C	1.9	2.16			
Minimum Output Voltage Low	Each output with 100 Ω to mid-supply, T_A = 25°C		–2.16	–1.95	V	
	Each output with 100 Ω to mid-supply, T_A = –40C to 85°C		–2.16	–1.9		
Differential Output Voltage Swing	T_A = –40C to 85°C	7.8	8.64		V	
Differential Output Current Drive	R_L = 10 Ω		105		mA	C
Output Balance Error	V_O = 100 mV, f = 1 MHz		–80		dB	
OUTPUT COMMON-MODE VOLTAGE CONTROL						
Small-Signal Bandwidth			230		MHz	C
Gain			1		V/V	
Output Common-Mode Offset from CM input	1.25 V < CM < 3.5 V		±0.25		mV	
CM Input Bias Current	1.25 V < CM < 3.5 V		0.6		μA	
CM Input Voltage		–1.5		1.5	V	
CM Default Voltage	CM = 0.5 (V_{S+} + V_{S-})		0		V	
POWER SUPPLY						
Specified Operating Voltage		3	5	5.25	V	C
Maximum Quiescent Current	T_A = 25°C		14.2	15.3	mA	A
	T_A = –40C to 85°C		14.2	15.5		
Minimum Quiescent Current	T_A = 25°C	13.1	14.2		mA	
	T_A = –40C to 85°C	12.75	14.2			
Power Supply Rejection (±PSRR)			94		dB	
POWERDOWN	Referenced to V_{S-}					
Enable Voltage Threshold	For additional information, see the *Application Information* section of this data sheet.		>1.5		V	C
Disable Voltage Threshold			<–1.5		V	
Powerdown Quiescent Current	T_A = 25°C		15	70	μA	A
	T_A = –40C to 85°C		15	75		

SPECIFICATIONS; $V_{S+} - V_{S-}$ = 3.3 V:

Test conditions unless otherwise noted: V_{S+} = +1.65 V, V_{S-} = –1.65 V, G = 0 dB, CM = open, V_O = 1 V_{PP}, R_F = 499 Ω, R_L = 200 Ω Differential, T_A = 25°C Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE								
Small-Signal Bandwidth	G = 0 dB, V_O = 100 mV_{PP}				600		MHz	C
	G = 6 dB, V_O = 100 mV_{PP}				400		MHz	
	G = 10 dB, V_O = 100 mV_{PP}				310		MHz	
	G = 20 dB, V_O = 100 mV_{PP}				120		MHz	
Gain-Bandwidth Product	G = 20 dB				1200		MHz	
Bandwidth for 0.1 dB flatness	G = 6 dB, V_O = 1 V_{PP}				30		MHz	
Large-Signal Bandwidth	G = 0 dB, V_O = 1 V_{PP}				210		MHz	
Slew Rate (Differential)	2-V Step				320		V/µs	C
Rise Time					4		ns	
Fall Time					4			
Settling Time to 1%					6.6			
Settling Time to 0.1%					7.1			
2nd Order Harmonic Distortion(2)	f = 100 kHz(3)	R_L = 1 kΩ	V_{OD} = 4 V_{PP}		–135		dBc	C
	f = 1 MHz(4)	R_L = 200 Ω	V_{OD} = 1 V_{PP}		–107			
			V_{OD} = 2 V_{PP}		–101			
		R_L = 1 kΩ	V_{OD} = 1 V_{PP}		–97			
			V_{OD} = 2 V_{PP}		–103			
	f = 8 MHz(4)	R_L = 200 Ω	V_{OD} = 1 V_{PP}		–108			
			V_{OD} = 2 V_{PP}		–106			
		R_L = 1 kΩ	V_{OD} = 1 V_{PP}		–98			
			V_{OD} = 2 V_{PP}		–99			
3rd Order Harmonic Distortion(2)	f = 100 kHz(3)	R_L = 1 kΩ	V_{OD} = 4 V_{PP}		–146		dBc	C
	f = 1 MHz(4)	R_L = 200 Ω	V_{OD} = 1 V_{PP}		–112			
			V_{OD} = 2 V_{PP}		–105			
		R_L = 1 kΩ	V_{OD} = 1 V_{PP}		–94			
			V_{OD} = 2 V_{PP}		–103			
	f = 8 MHz(4)	R_L = 200 Ω	V_{OD} = 1 V_{PP}		–95			
			V_{OD} = 2 V_{PP}		–90			
		R_L = 1 kΩ	V_{OD} = 1 V_{PP}		–95			
			V_{OD} = 2 V_{PP}		–102			
3rd Order Intermodulation Distortion	f_C = 1 MHz(4), 100-kHz Tone Spacing, R_L = 200 Ω, V_{OD} = 4 V_{PP} envelope, G = 10dB				-80		dBc	C
	f_C = 10 MHz(4), 100-kHz Tone Spacing, R_L = 200 Ω, V_{OD} = 4 V_{PP} envelope, G = 10dB				-80			
Input Voltage Noise	f > 10 kHz				2		nV/√Hz	
Input Current Noise	f > 10 kHz				2		pA/√Hz	

(1) Test levels: **(A)** 100% tested at 25°C. Overtemperature limits by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.
(2) For additional information, see the Typical Characteristics section and the Apllications section.
(3) Data collected with applied differential input signal and measured differential output signal.
(4) Data collected with applied single-ended input signal and measured differential output signal. See Figure 55 in the Applications/Test Circuits section for additional information.

SPECIFICATIONS; $V_{S+} – V_{S–}$ = 3.3 V: (continued)

Test conditions unless otherwise noted: V_{S+} = +1.65 V, $V_{S–}$ = –1.65 V, G = 0 dB, CM = open, V_O = 1 V_{PP}, R_F = 499 Ω, R_L = 200 Ω Differential, T_A = 25°C Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL[1]
DC PERFORMANCE						
Open-Loop Voltage Gain (A_{OL})			104		dB	C
Input Offset Voltage	T_A = 25°C		±0.25		mV	
	T_A = –40°C to 85°C		±0.25		mV	
Average Offset Voltage Drift	T_A = –40°C to 85°C		1		μV/°C	
Input Bias Current	T_A = 25°C		6.5		μA	C
	T_A = –40°C to 85°C		6.4			
Average Bias Current Drift	T_A = –40°C to 85°C		1.9		nA/°C	
Input Offset Current	T_A = 25°C		±0.2		μA	C
	T_A = –40°C to 85°C		±0.2			
Average Offset Current Drift	T_A = –40°C to 85°C		1.6		nA/°C	
INPUT						
Common-Mode Input Range High			1.4		V	C
Common-Mode Input Range Low			–0.45			
Common-Mode Rejection Ratio			84		dB	
OUTPUT						
Maximum Output Voltage High	Each output with 100 Ω to mid-supply; T_A = 25°C		1.4		V	C
Minimum Output Voltage Low	T_A = 25°C		–1.4			
Differential Output Voltage Swing			5.6		V	
Differential Output Current Drive	R_L = 10 Ω		78		mA	C
Output Balance Error	V_O = 100 mV, f = 1 MHz		–80		dB	
OUTPUT COMMON-MODE VOLTAGE CONTROL						
Small-Signal Bandwidth			224		MHz	C
Gain			1		V/V	
Output Common-Mode Offset from CM input	1.25 V < CM < 3.5 V		±0.25		mV	
CM Input Bias Current	1.25 V < CM < 3.5 V		0.6		μA	
CM Default Voltage	CM = 0.5 (V_{S+} + V_{S-})		0		V	
POWER SUPPLY						
Specified Operating Voltage			3.3		V	C
Quiescent Current	T_A = 25°C		13		mA	
Power Supply Rejection (±PSRR)			94		dB	
POWERDOWN	Referenced to $V_{s–}$					
Enable Voltage Threshold	For additional information, see the *Application Information* section of this data sheet.		>1		V	C
Disable Voltage Threshold			<-1		V	
Powerdown Quiescent Current			10		μA	C

TYPICAL CHARACTERISTICS

TYPICAL AC PERFORMANCE: $V_{S+} – V_{S–} = 5$ V

Test conditions unless otherwise noted: V_{S+} = +2.5 V, $V_{S–}$ = –2.5 V, CM = open, V_O = 2 V_{PP}, R_F = 499 Ω, R_L = 200 Ω Differential, G = 0 dB, Single-Ended Input, Input and Output Referenced to Midrail

Small-Signal Frequency Response			Figure 1
Large Signal Frequency Response			Figure 2
Harmonic Distortion(1)	HD2	vs Frequency, V_O = 2 V_{PP}	Figure 3
	HD3	vs Frequency, V_O = 2 V_{PP}	Figure 4
	HD2	vs Frequency, V_O = 4 V_{PP}	Figure 5
	HD3	vs Frequency, V_O = 4 V_{PP}	Figure 6
	HD2	vs Output Voltage Swing, f = 1 MHz	Figure 7
	HD3	vs Output Voltage Swing, f = 1 MHz	Figure 8
	HD2	vs Output Voltage Swing, f = 8 MHz	Figure 9
	HD3	vs Output Voltage Swing, f = 8 MHz	Figure 10
	HD2	vs Load Resistance, f = 1 MHz	Figure 11
	HD3	vs Load Resistance, f = 1 MHz	Figure 12
	HD2	vs Load Resistance, f = 8 MHz	Figure 13
	HD3	vs Load Resistance, f = 8 MHz	Figure 14
	HD2	vs Output common-mode voltage	Figure 15
	HD3	vs Output common-mode voltage	Figure 16
0.1 dB Flatness			Figure 17
S-Parameters		vs Frequency	Figure 18
Slew Rate		vs Output Voltage	Figure 19
Transient Response		Gain = 6 dB, V_O = 4 V_{PP}	Figure 20
		Gain = 6 dB, V_O = 2 V_{PP}	Figure 21
Output Voltage Swing		vs Load Resistance	Figure 22
Input Offset Voltage		vs Input Common-Mode Voltage	Figure 23
Input Bias Current		vs Supply Voltage	Figure 24
Open Loop Gain and Phase		vs Frequency	Figure 25
Input Referred Noise		vs Frequency	Figure 26
Quiescent Current		vs Supply Voltage	Figure 27
Power Supply Current		vs Supply Voltage in Powerdown Mode	Figure 28
Output Balance Error		vs Frequency	Figure 29
CM Small-Signal Frequency Response			Figure 30
CM Input Bias Current		vs CM Input Voltage	Figure 31
Differential Output Offset Voltage		vs CM Input Voltage	Figure 32
Output Common-Mode Offset		vs CM Input Voltage	Figure 33

(1) For additional plots, see the Applications section.

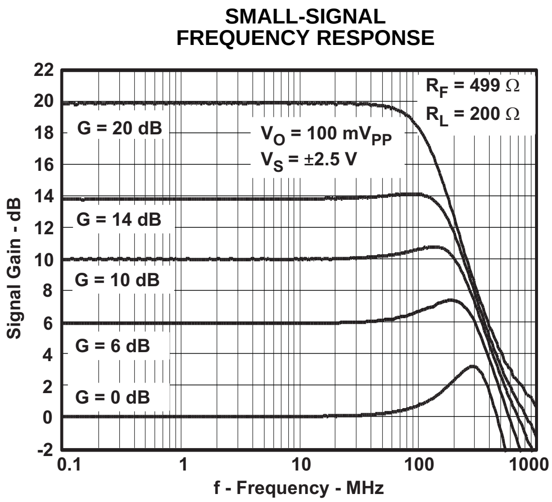


Figure 1.

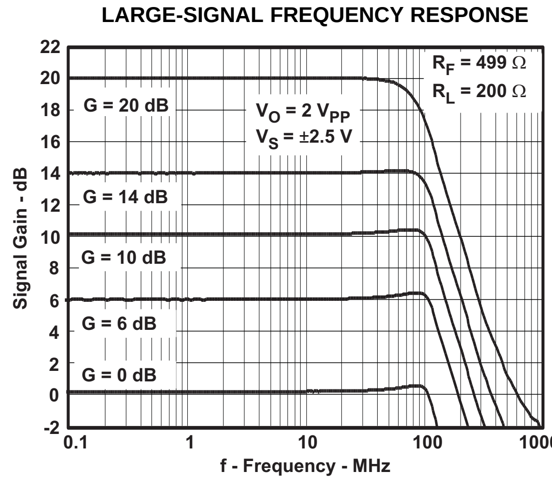


Figure 2.

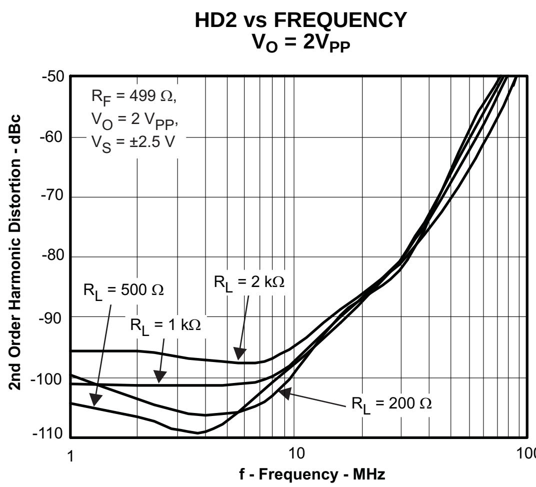


Figure 3.

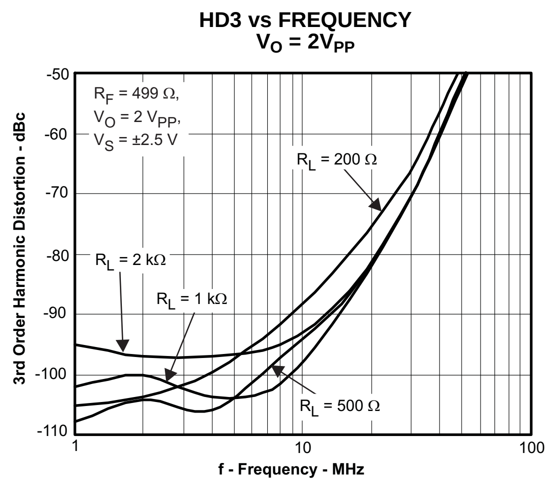


Figure 4.

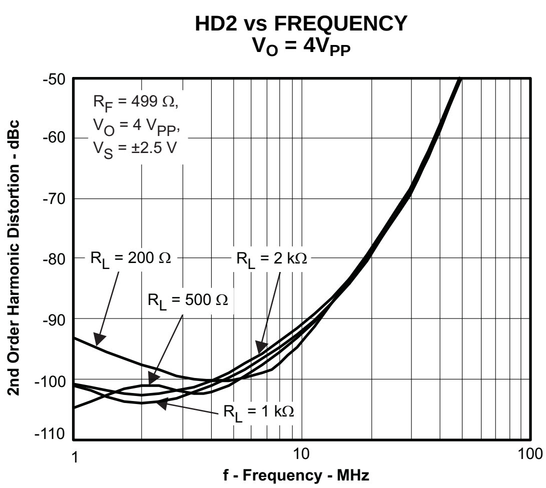


Figure 5.

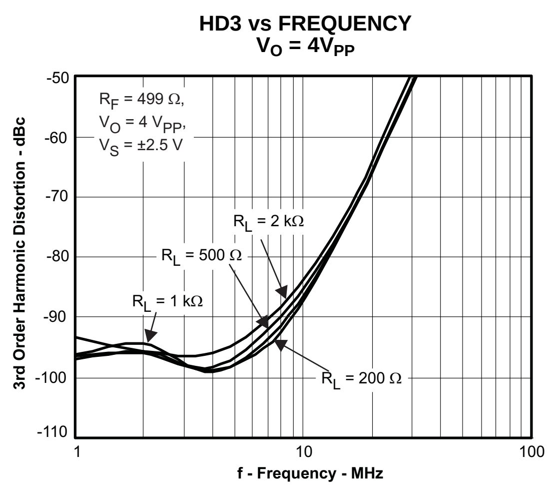


Figure 6.

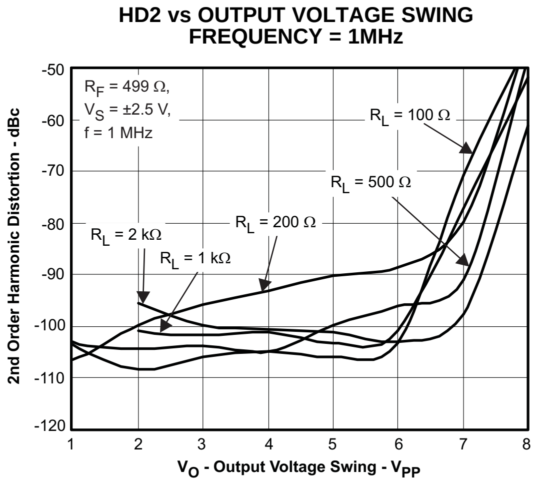


Figure 7.

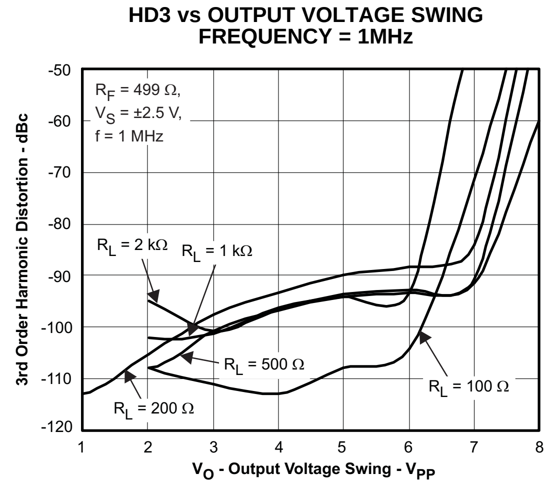


Figure 8.

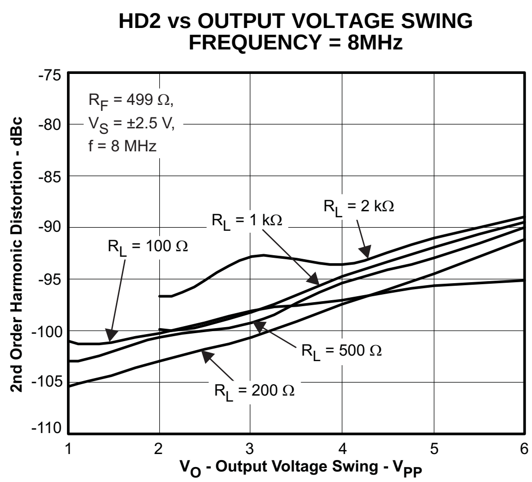


Figure 9.

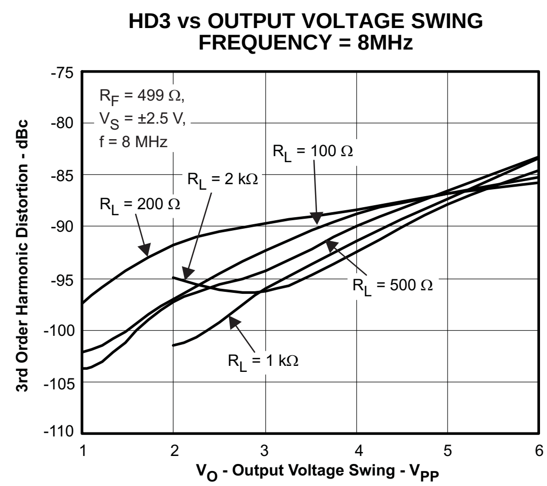


Figure 10.

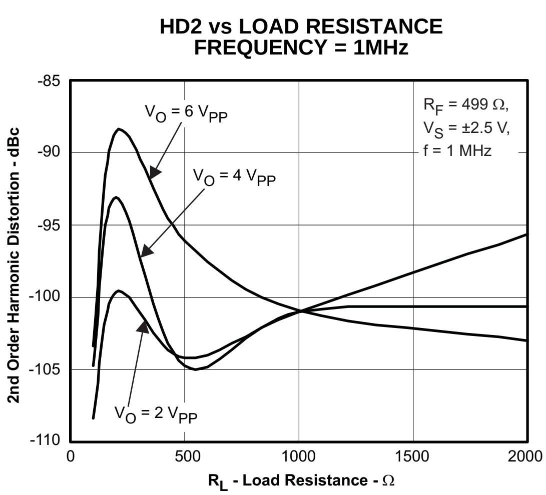


Figure 11.

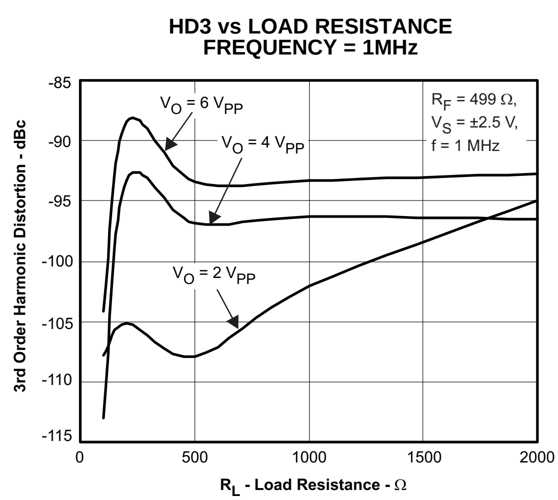


Figure 12.

HD2 vs LOAD RESISTANCE FREQUENCY = 8MHz

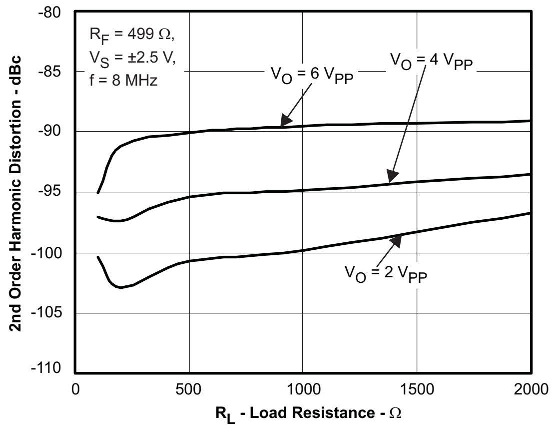


Figure 13.

HD3 vs LOAD RESISTANCE FREQUENCY = 8MHz

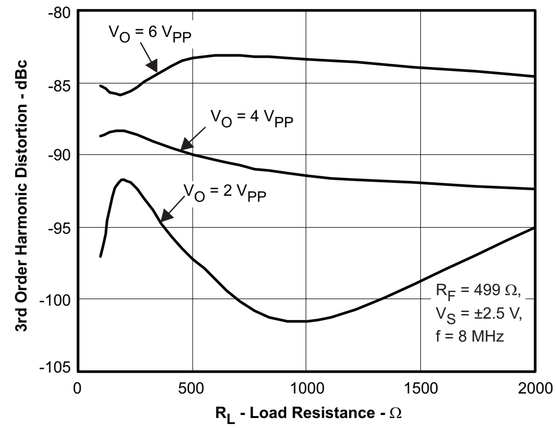


Figure 14.

HD2 vs OUTPUT COMMON-MODE VOLTAGE

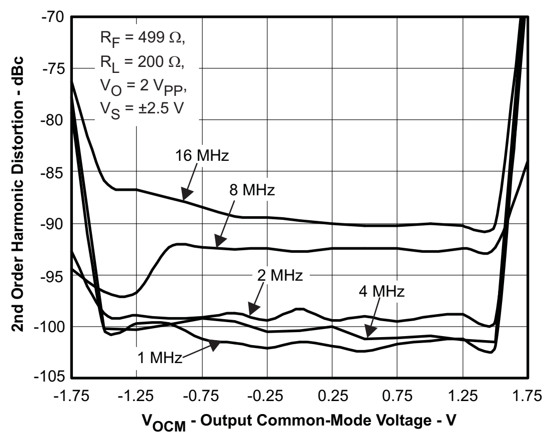


Figure 15.

HD3 vs OUTPUT COMMON-MODE VOLTAGE

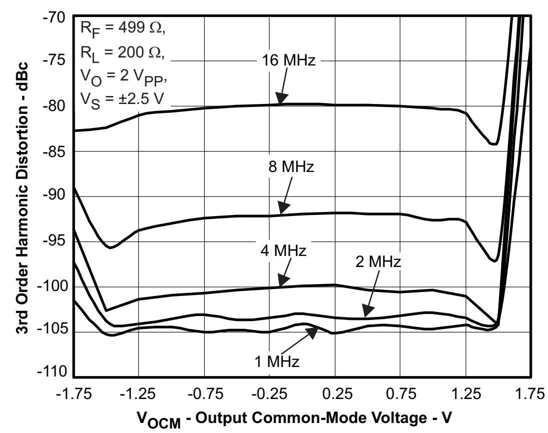


Figure 16.

0.1-dB FLATNESS

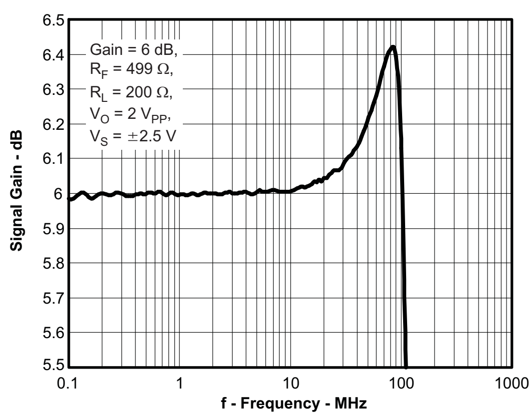
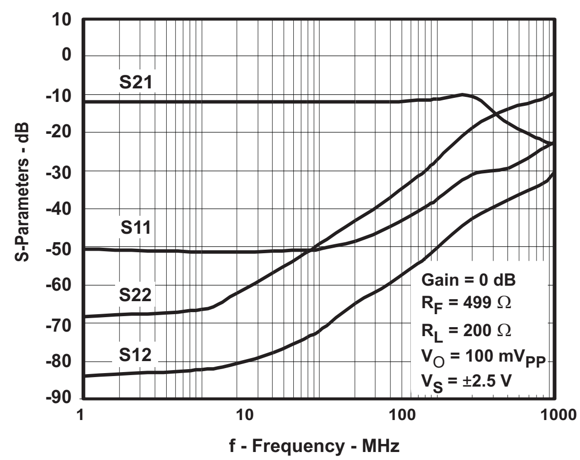


Figure 17.

S-PARAMETERS vs FREQUENCY



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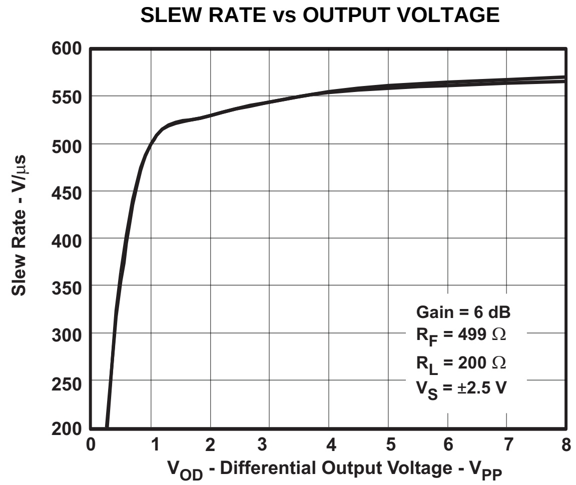

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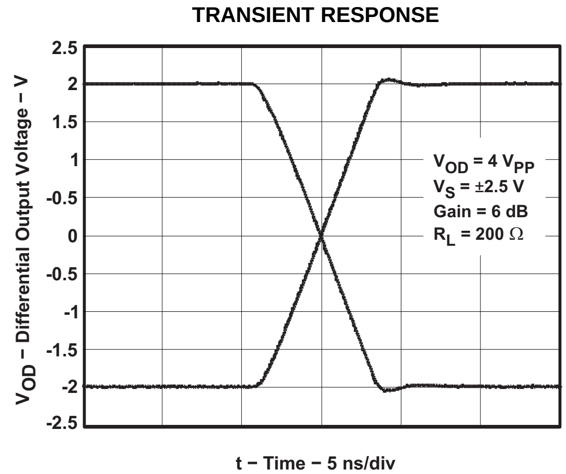

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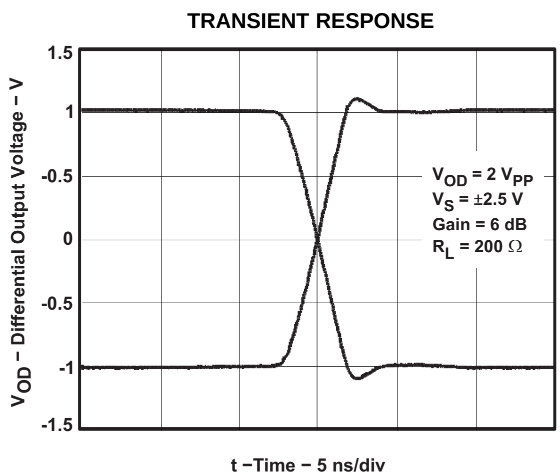


Figure 21.

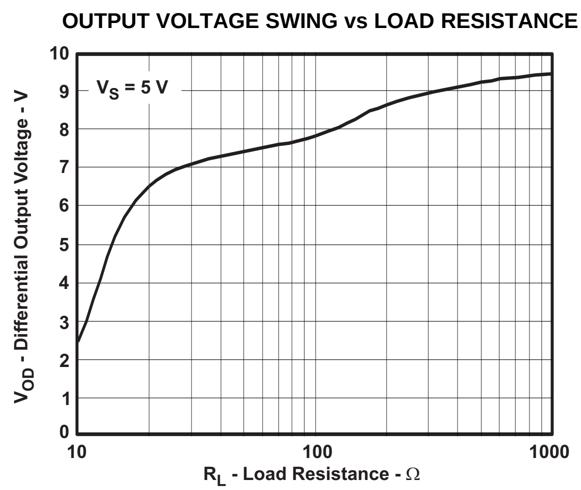


Figure 22.

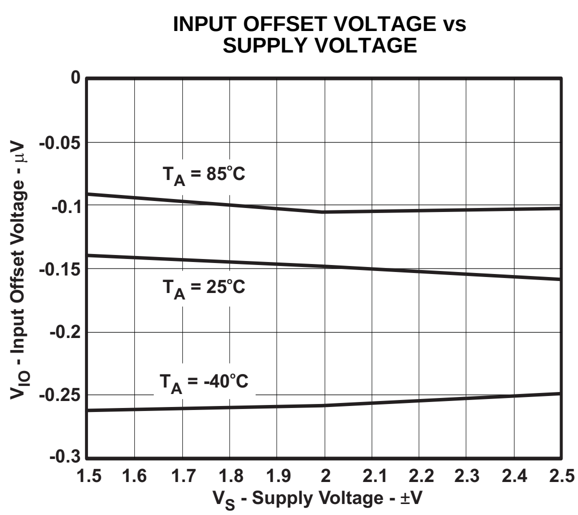


Figure 23.

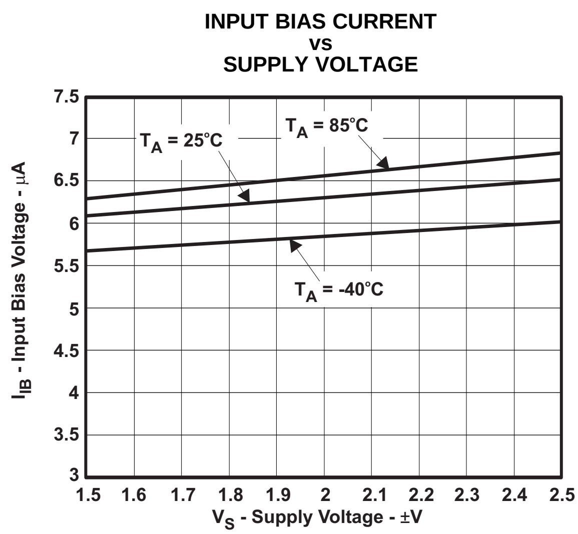


Figure 24.

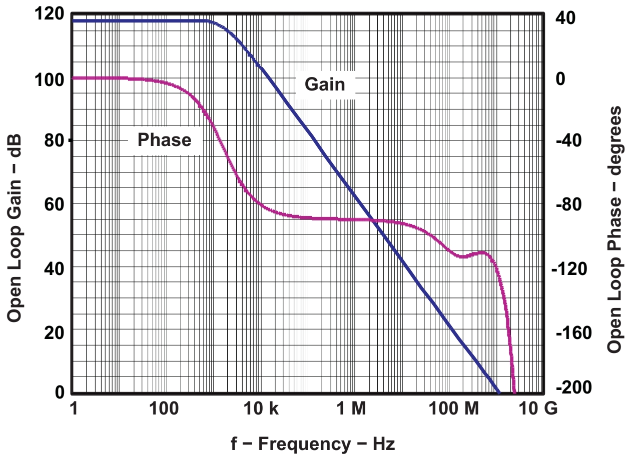
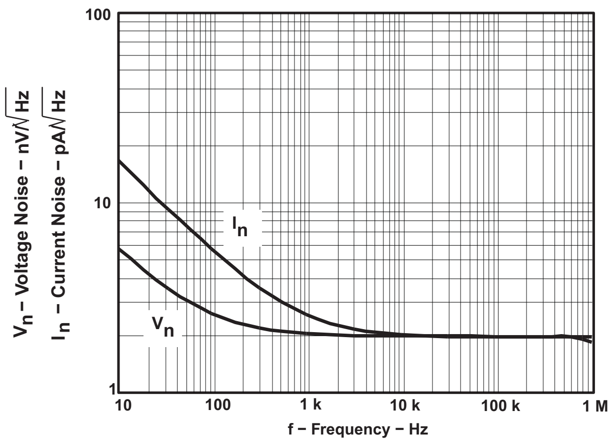


Figure 25.



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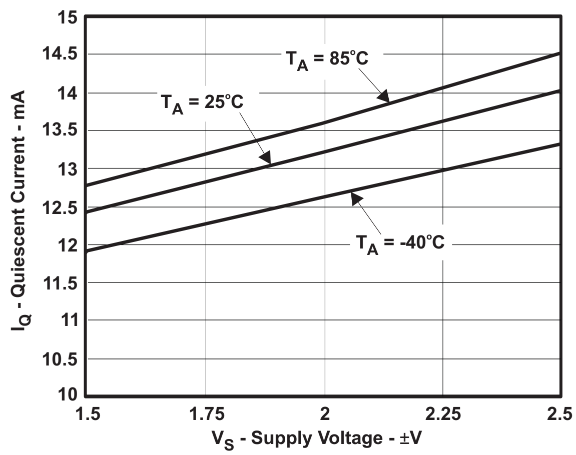


Figure 27.

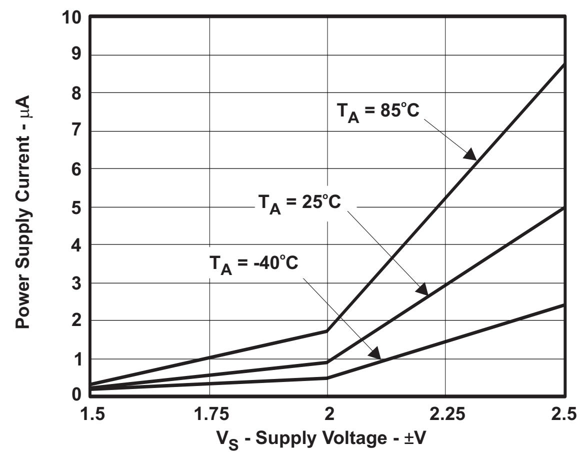


Figure 28.

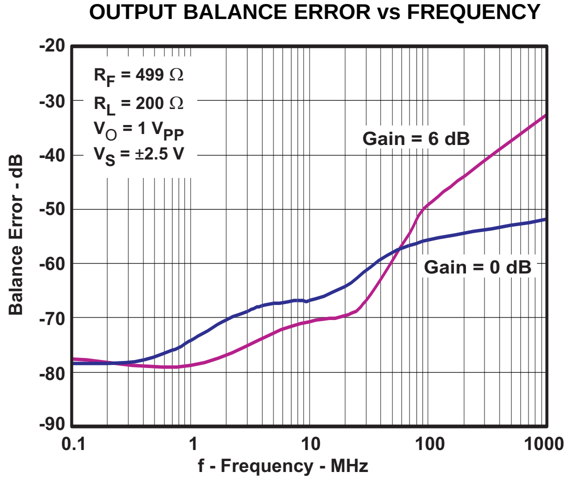


Figure 29.

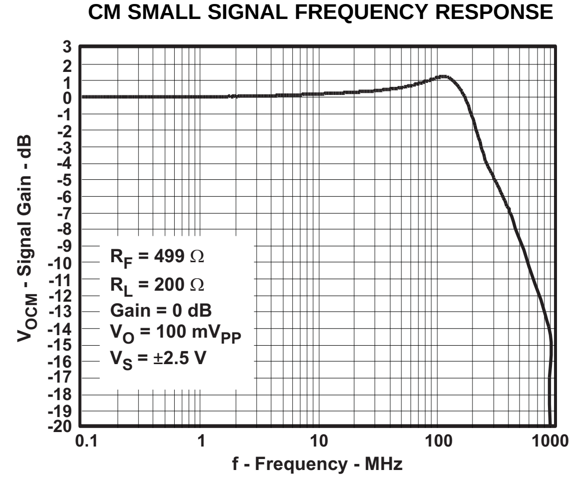


Figure 30.

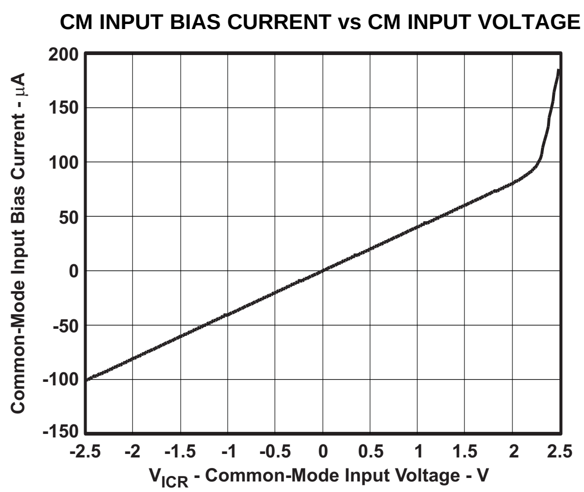


Figure 31.

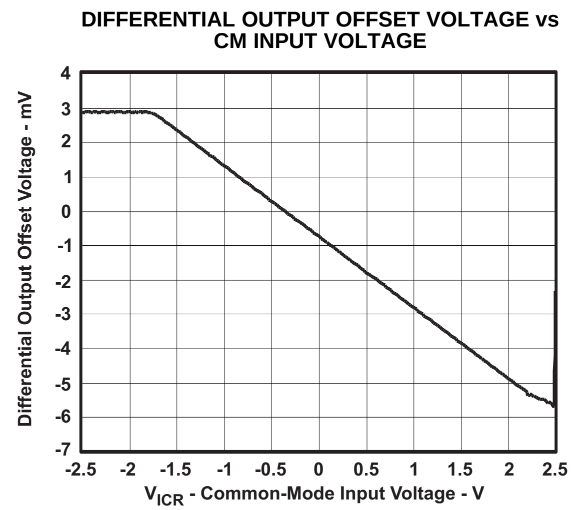


Figure 32.

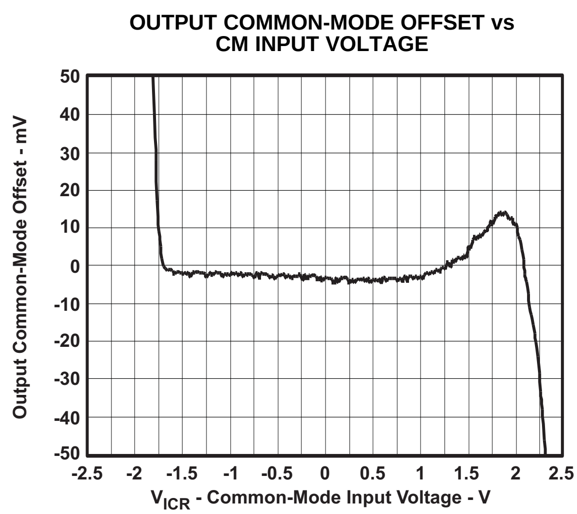


Figure 33.

TYPICAL AC PERFORMANCE: $V_{S+} - V_{S-}$ = 3.3 V

Test conditions unless otherwise noted: V_{S+} = 1.65 V, V_{S-} = –1.65 V, CM = open, V_{OD} = 1 V_{PP}, R_F = 499 Ω, R_L = 200 Ω Differential, G = 0 dB, Single-Ended Input, Input and Output Referenced to Midrail

Small-Signal Frequency Response			Figure 34
Large Signal Frequency Response			Figure 35
Harmonic Distortion (1)	HD2	vs Frequency	Figure 36
	HD3	vs Frequency	Figure 37
	HD2	vs Output Voltage Swing, f = 1 MHz	Figure 38
	HD3	vs Output Voltage Swing, f = 1 MHz	Figure 39
	HD2	vs Output Voltage Swing, f = 8 MHz	Figure 40
	HD3	vs Output Voltage Swing, f = 8 MHz	Figure 41
	HD2	vs Load Resistance, f = 1 MHz	Figure 42
	HD3	vs Load Resistance, f = 1 MHz	Figure 43
	HD2	vs Load Resistance, f = 8 MHz	Figure 44
	HD3	vs Load Resistance, f = 8 MHz	Figure 45
	HD2	vs Output common-mode voltage, V_O = 2 V_{pp}	Figure 46
	HD3	vs Output common-mode voltage, V_O = 2 V_{pp}	Figure 47
0.1 dB Flatness			Figure 48
S-Parameters		vs Frequency	Figure 49
Slew Rate		vs Output Voltage	Figure 50
Transient Response		Gain = 6 dB, V_O = 4 V_{pp}	Figure 51
		Gain = 6 dB, V_O = 2 V_{pp}	Figure 52
Output Balance Error		vs Frequency	Figure 53
CM Input Impedance		vs Frequency	Figure 54

(1) For additional plots, see the Applications section.

SMALL-SIGNAL FREQUENCY RESPONSE

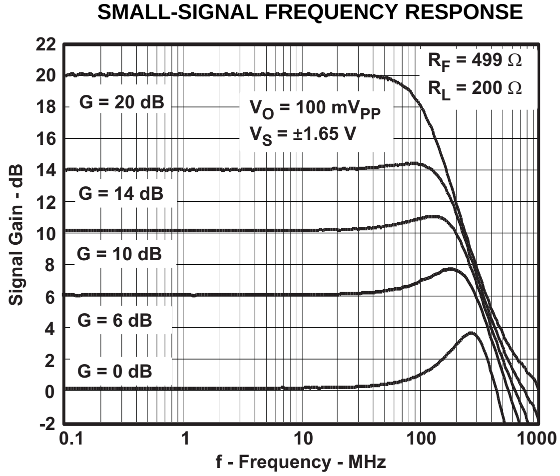


Figure 34.

LARGE-SIGNAL FREQUENCY RESPONSE

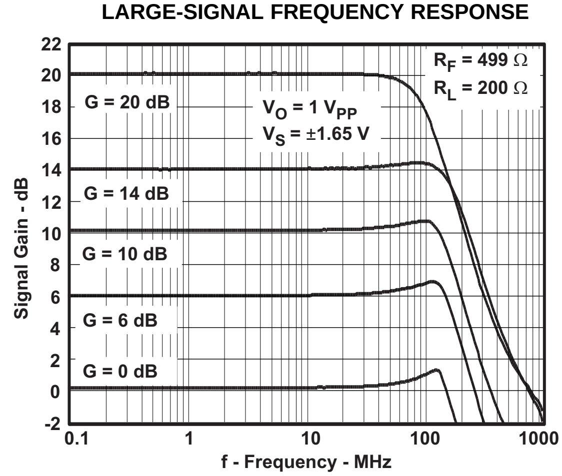


Figure 35.

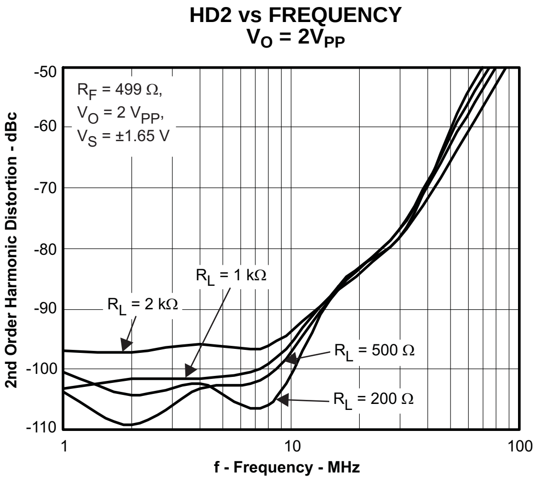


Figure 36.

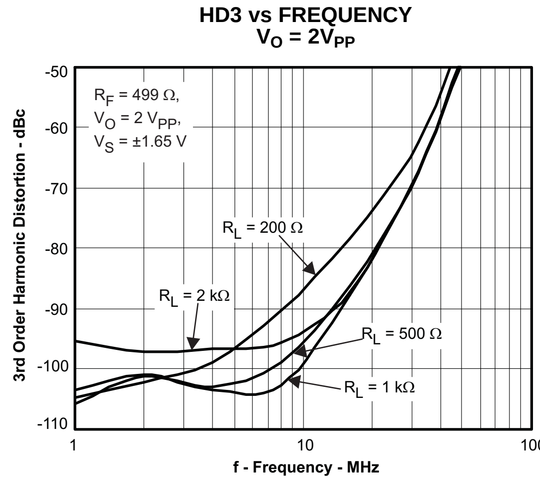


Figure 37.

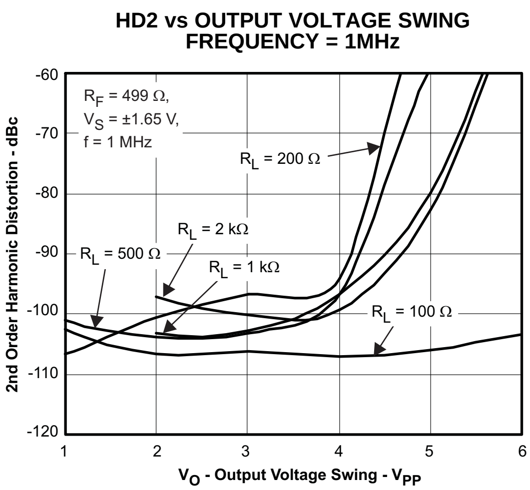


Figure 38.

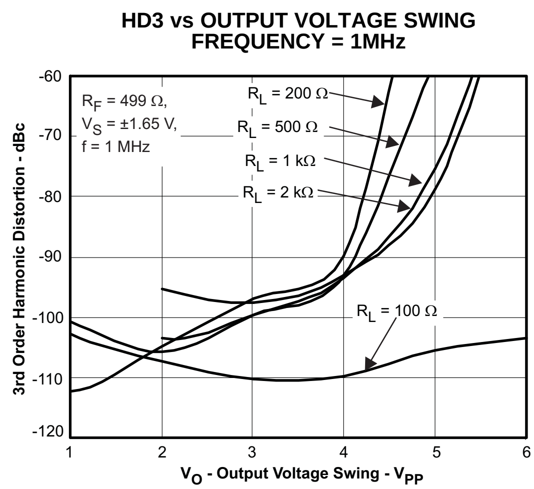


Figure 39.

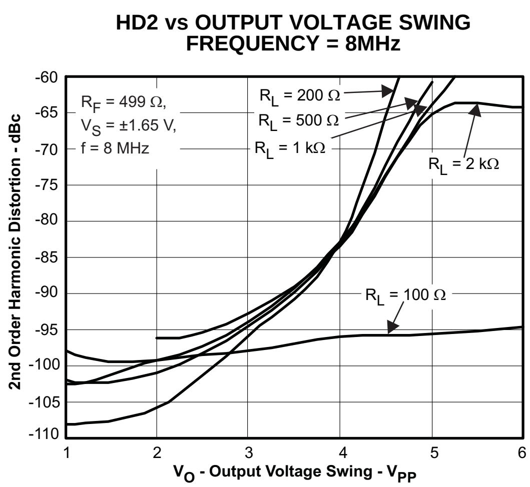


Figure 40.

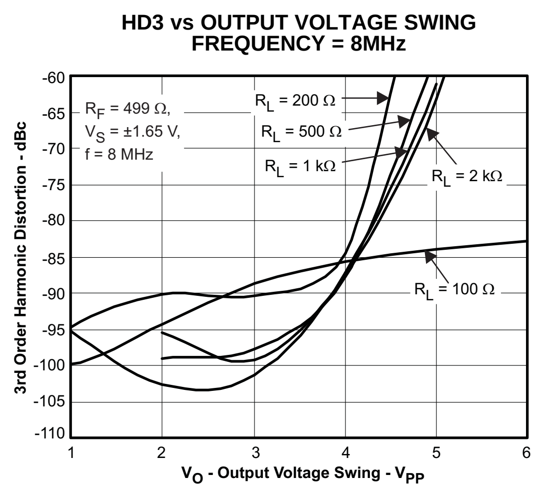


Figure 41.

HD2 vs LOAD RESISTANCE
FREQUENCY = 1MHZ

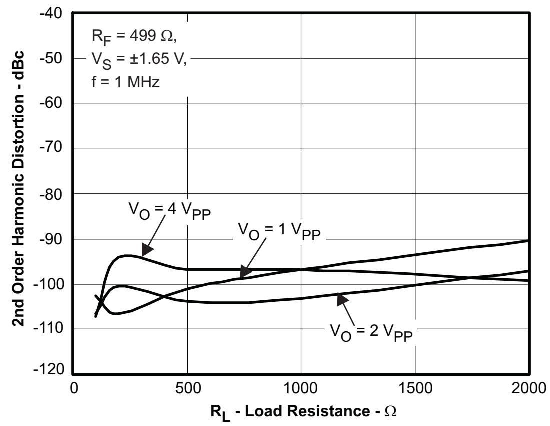


Figure 42.

HD3 vs LOAD RESISTANCE
FREQUENCY = 1MHZ

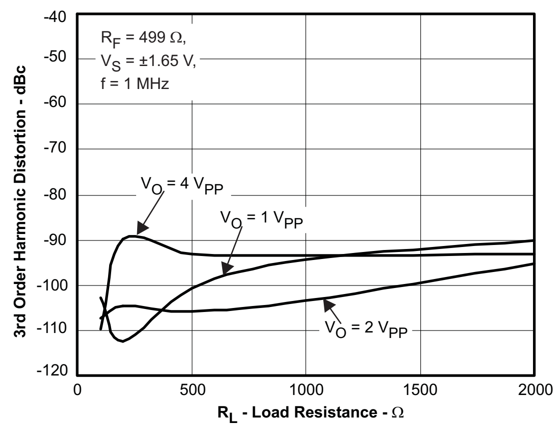


Figure 43.

HD2 vs LOAD RESISTANCE
FREQUENCY = 8MHZ

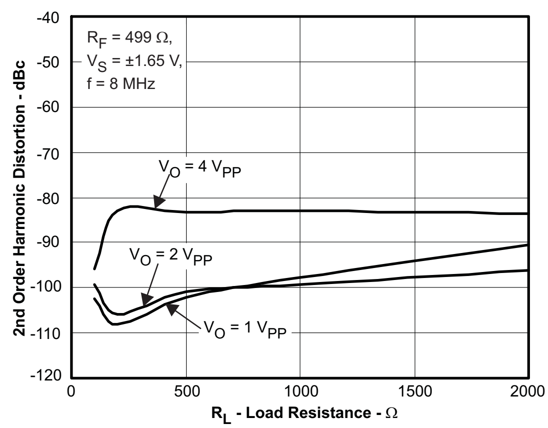


Figure 44.

HD3 vs LOAD RESISTANCE
FREQUENCY = 8MHZ

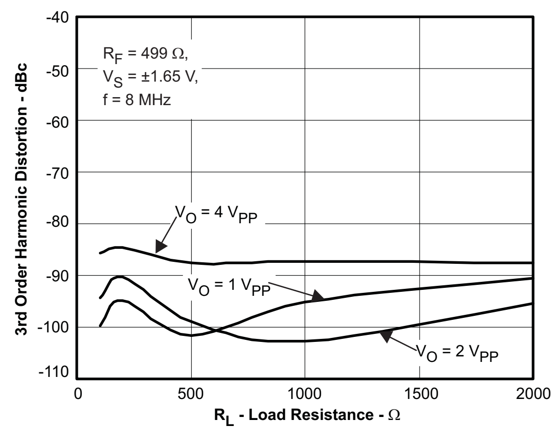


Figure 45.

HD2 vs
OUTPUT COMMON-MODE VOLTAGE

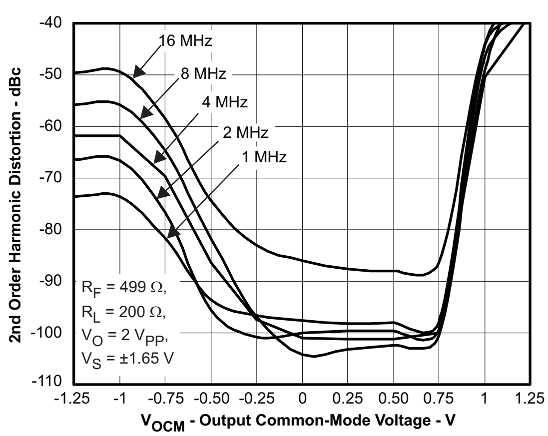


Figure 46.

HD3 vs
OUTPUT COMMON-MODE VOLTAGE

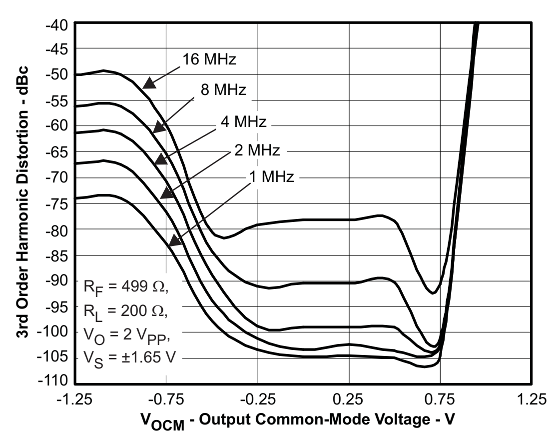


Figure 47.

0.1 dB FLATNESS

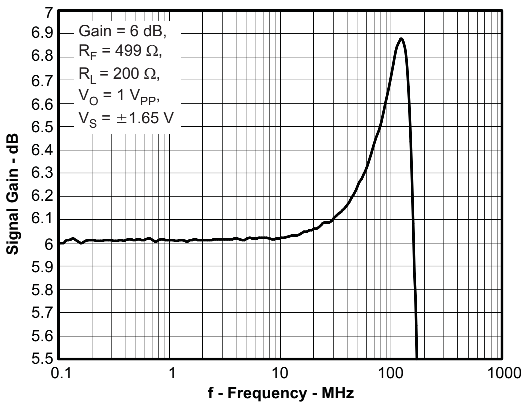


Figure 48.

S-PARAMETERS vs FREQUENCY

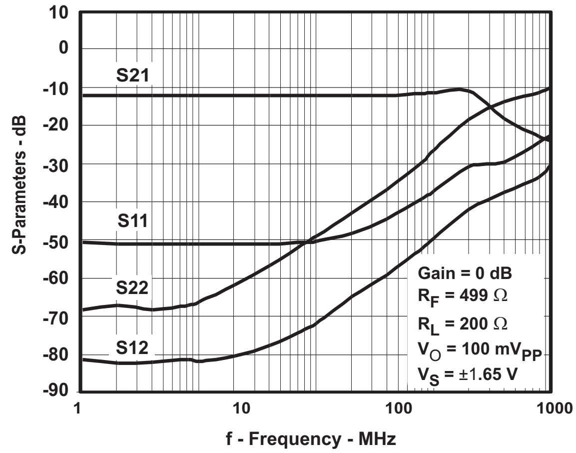


Figure 49.

TRANSITION RATE vs OUTPUT VOLTAGE

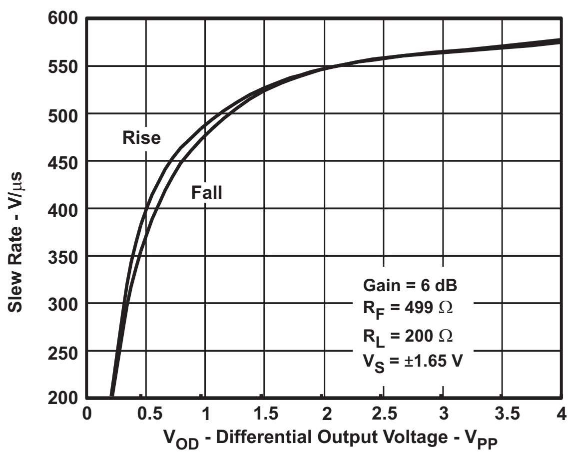


Figure 50.

TRANSIENT RESPONSE

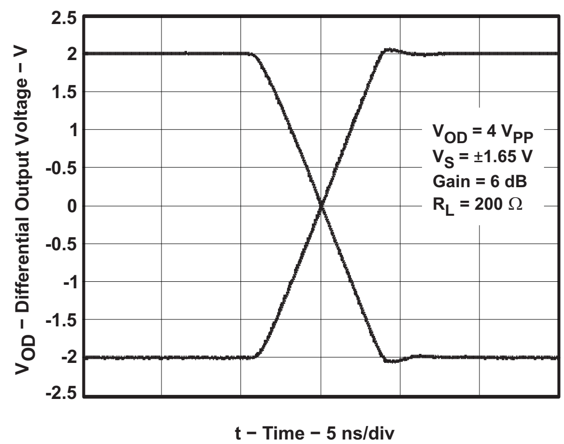


Figure 51.

TRANSIENT RESPONSE

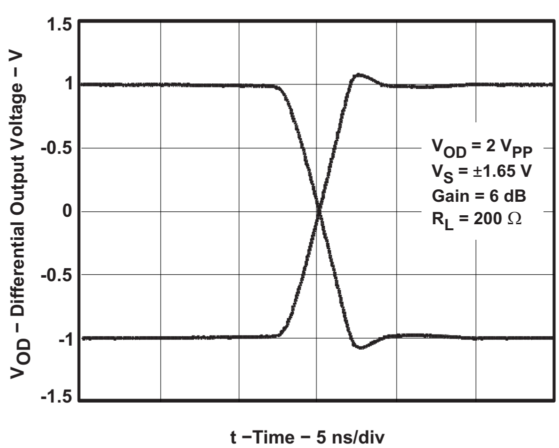


Figure 52.

OUTPUT BALANCE ERROR vs FREQUENCY

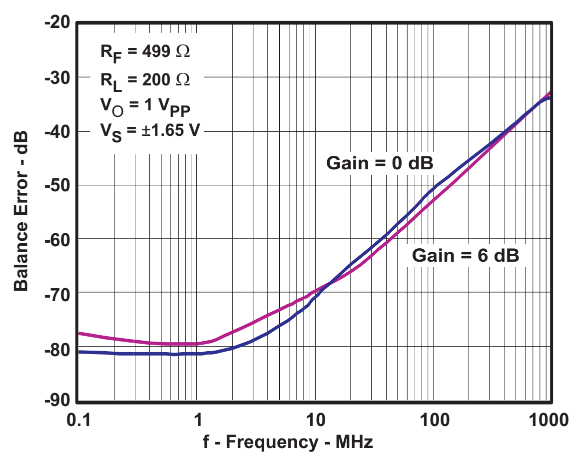


Figure 53.

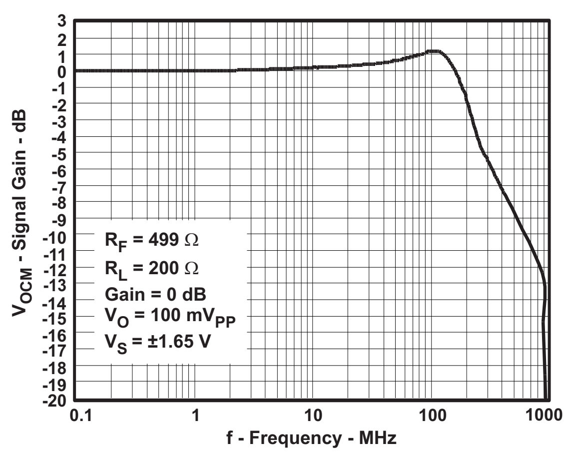


Figure 54.

TEST CIRCUITS

The THS4520 is tested with the following test circuits built on the EVM. For simplicity, power supply decoupling is not shown – see layout in the applications section for recommendations.

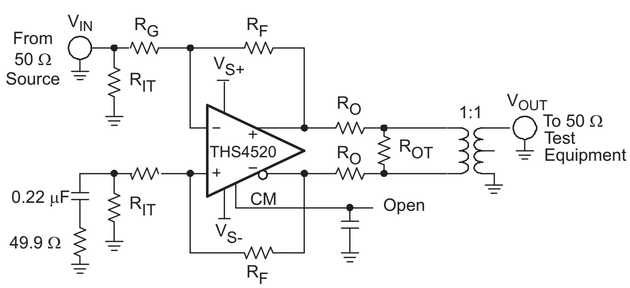


Figure 55. General Test Circuit for Device Testing and Characterization

Depending on the test conditions, component values are changed per the following tables, or as otherwise noted. The signal generators used are ac coupled 50-Ω sources and a 0.22-μF capacitor and a 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input to balance the circuit. A split power supply is used to ease the interface to common test equipment, but the amplifier can be operated single-supply as described in the applications section with no impact on performance.

Table 1. Gain Component Values

GAIN	R_F	R_G	R_{IT}
0 dB	499 Ω	487 Ω	53.6 Ω
6 dB	499 Ω	243 Ω	57.6 Ω
10 dB	499 Ω	147 Ω	63.4 Ω
14 dB	499 Ω	88.7 Ω	71.5 Ω
20 dB	499 Ω	34.8 Ω	115 Ω

Note: The gain setting includes 50-Ω source impedance. Components are chosen to achieve gain and 50-Ω input termination.

Table 2. Load Component Values

R_L	R_O	R_{OT}	Atten.
100 Ω	25 Ω	open	6 dB
200 Ω	86.6 Ω	69.8 Ω	16.8 dB
499 Ω	237 Ω	56.2 Ω	25.5 dB
1 kΩ	487 Ω	52.3 Ω	31.8 dB
2 k	976	51.1	–37.86

Note: The total load includes 50-Ω termination by the test equipment. Components are chosen to achieve load and 50-Ω line termination through a 1:1 transformer.

Due to the voltage divider on the output formed by the load component values, the amplifier's output is attenuated in test. The column *Atten* in Table 2 shows the attenuation expected from the resistor divider. When using a transformer at the output the signal will have slightly more loss, and the numbers will be approximate.

Frequency Response

The general circit shown in Figure 55 is modified as shown in Figure 56, and is used to measure the frequency response of the device.

A network analyzer is used as the signal source and as the measurement device. The output impedance of the network analyzer is 50 Ω. R_{IT} and R_G are chosen to impedance match to 50 Ω, and to maintain the proper gain. To balance the amplifier, a 0.22-μF capacitor and 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input.

The output is probed using a high-impedance differential probe across the 100-Ω resistor. The gain is referred to the amplifier output by adding back the 6-dB loss due to the voltage divider on the output.

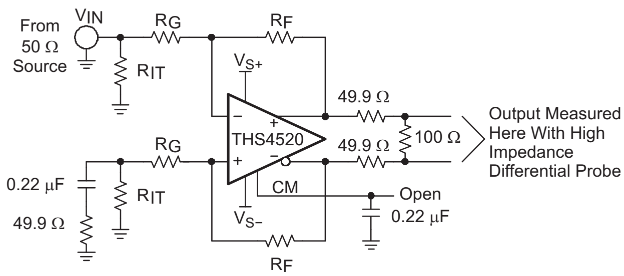


Figure 56. Frequency Response Test Circuit

S-Parameter, Slew Rate, Transient Response, Settling Time, Output Voltage

The circuit shown in Figure 57 is used to measure s-parameters, slew rate, transient response, settling time, and output voltage swing.

Because S21 is measured single-ended at the load with 50-Ω double termination, add 12 dB to see the amplifier's output as a differential signal.

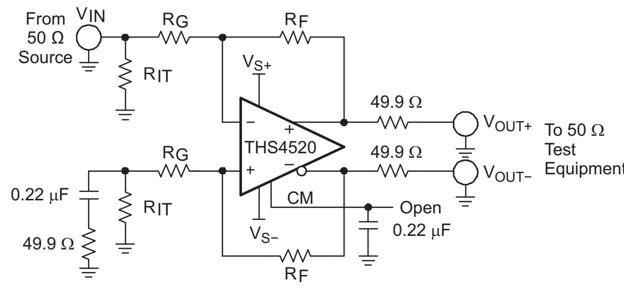


Figure 57. S-Parameter, SR, Transient Response, Settling Time, V_{OUT} Swing

CM Input

The circuit shown in Figure 58 is used to measure the frequency response of the CM input. Frequency response is measured single-ended at V_{OUT+} or V_{OUT-} with the input injected at V_{IN}, R_{CM} = 0 Ω and R_{CMT} = 49.9 Ω.

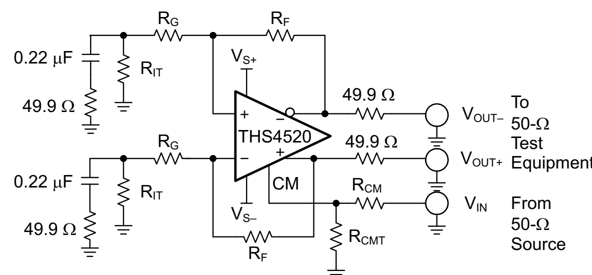


Figure 58. CM Input Test Circuit

APPLICATION INFORMATION

APPLICATIONS

The following circuits show application information for the THS4520. For simplicity, power supply decoupling capacitors are not shown in these diagrams. For more detail on the use and operation of fully differential op amps see application report *Fully-Differential Amplifiers* (SLOA054) .

Differential Input to Differential Output Amplifier

The THS4520 is a fully differential op amp, and can be used to amplify differential input signals to differential output signals. A basic block diagram of the circuit is shown in Figure 59 (CM input not shown). The gain of the circuit is set by R_F divided by R_G.

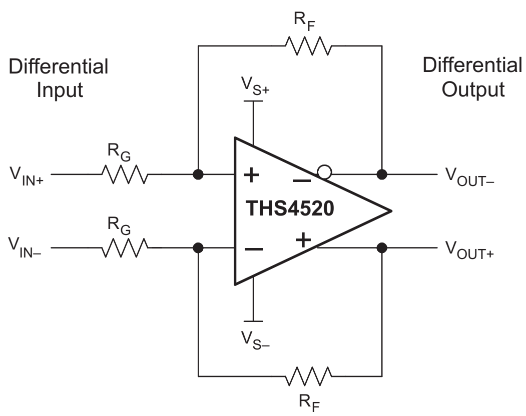


Figure 59. Differential Input to Differential Output Amplifier

Depending on the source and load, input and output termination can be accomplished by adding R_{IT} and R_O.

Single-Ended Input to Differential Output Amplifier

The THS4520 can be used to amplify and convert single-ended input signals to differential output signals. A basic block diagram of the circuit is shown in Figure 60 (CM input not shown). The gain of the circuit is again set by R_F divided by R_G.

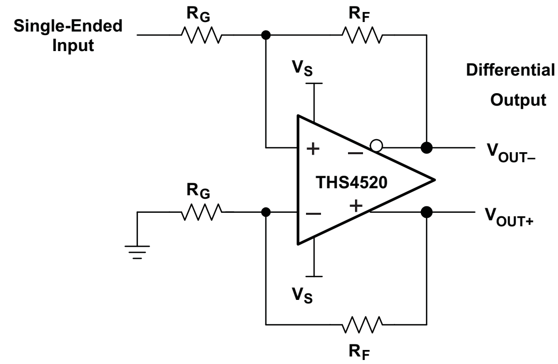


Figure 60. Single-Ended Input to Differential Output Amplifier

Input Common-Mode Voltage Range

The input common-model voltage of a fully differential op amp is the voltage at the '+' and '–' input pins of the op amp.

It is important to not violate the input common-mode voltage range (V_{ICR}) of the op amp. Assuming the op amp is in linear operation, the differential voltage across the input pins is only a few millivolts at most. So finding the voltage at one input pin determines the input common-mode voltage of the op amp.

Treating the negative input as a summing node, the voltage is given by Equation 1:

$$V_{IC} = \left(V_{OUT+} \times \frac{R_G}{R_G + R_F} \right) + \left(V_{IN-} \times \frac{R_F}{R_G + R_F} \right) \quad (1)$$

To determine the V_{ICR} of the op amp, the voltage at the negative input is evaluated at the extremes of V_{OUT+}.

As the gain of the op amp increases, the input common-mode voltage becomes closer and closer to the input common-mode voltage of the source.

Setting the Output Common-Mode Voltage

The output common-mode voltage is set by the voltage at the CM pin. The internal common-mode control circuit maintains the output common-mode voltage within 0.25-mV offset (typical) from the set voltage, when set within ±0.5 V of mid-supply. If left unconnected, the common-mode set point is set to mid-supply by internal circuitry, which may be over-driven from an external source. Figure 61 is representative of the CM input. The internal CM circuit has about 230 MHz of bandwidth, which is required for best performance, but it is intended to be a DC bias input pin. Bypass capacitors are recommended on this pin to reduce noise at the output. The external current required to overdrive the internal resistor divider is given by Equation 2:

$$I_{EXT} = \frac{2V_{CM} - (V_{S+} - V_{S-})}{50\ k\Omega} \qquad (2)$$

where V_{CM} is the voltage applied to the CM pin.

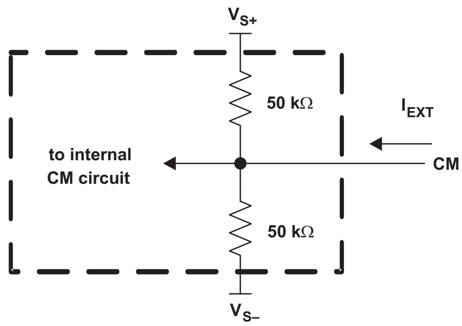


Figure 61. CM Input Circuit

Powerdown Operation: Device Enable/Disable Thresholds

The enable/disable thresholds of the THS4520 are dependent upon the power supplies, and the thresholds are always referenced to the lower power supply rail. The device is enabled or disabled for the following conditions:

- Device enabled: $V_{PD} > V_{S-} + 0.8 \times (V_{S+} - V_{S-})$
- Device disabled: $V_{PD} < V_{S-} + 0.2 \times (V_{S+} - V_{S-})$

If the $\overline{PD}$ pin is left open, the device will default to the enabled state.

Table 3 shows the thresholds for some common power supply configurations:

Table 3. Power Supply Configurations

Power Supply (V_{S+}, V_{S-})	Enable Threshold (V)	Disable Threshold (V)	Comment
±2.5 V	1.5	-1.5	Shown in data table
±1.65 V	1	-1	Shown in data table
(4 V , -1 V)	3	0	Split, unbalanced supplies
(5 V, gnd)	4	1	Single-sided supply
(3.3 V, gnd)	2.64	0.66	Single-sided supply
(3 V, gnd)	2.4	0.6	Single-sided supply

Single-Supply Operation (3 V to 5 V)

To facilitate testing with common lab equipment, the THS4520 EVM allows split-supply operation, and the characterization data presented in this data sheet was taken with split-supply power inputs. The device can easily be used with a single-supply power input without degrading the performance. Figure 62, Figure 63, and Figure 64 show DC and AC-coupled single-supply circuits with single-ended inputs. These configurations all allow the input and output common-mode voltage to be set to mid-supply allowing for optimum performance. The information presented here can also be applied to differential input sources.

In Figure 62, the source is referenced to the same voltage as the CM pin (V_{CM}). V_{CM} is set by the internal circuit to mid-supply. R_T along with the input impedance of the amplifier circuit provides input termination, which is also referenced to V_{CM}.

Note R_S and R_T are added to the alternate input from the signal input to balance the amplifier. Alternately, one resistor can be used equal to the combined value $R_G + R_S||R_T$ on this input. This is also true of the circuits shown in Figure 63 and Figure 64.

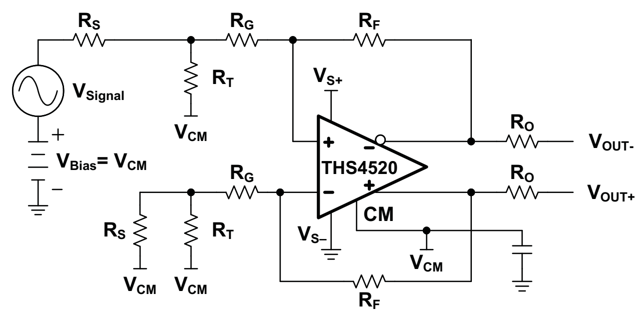


Figure 62. THS4520 DC Coupled Single-Supply with Input Biased to V_{CM}

In Figure 63 the source is referenced to ground and so is the input termination resistor. R_{PU} is added to the circuit to avoid violating the V_{ICR} of the op amp. The proper value of resistor to add can be calculated from Equation 3:

$$R_{PU} = \frac{(V_{IC} - V_{S+})}{V_{CM}\left(\frac{1}{R_F}\right) - V_{IC}\left(\frac{1}{R_{IN}} + \frac{1}{R_F}\right)} \qquad (3)$$

V_{IC} is the desired input common-mode voltage, V_{CM} = CM, and $R_{IN} = R_G + R_S||R_T$. To set to mid-supply, make the value of $R_{PU} = R_G + R_S||R_T$.

Table 4 is a modification of Table 1 to add the proper values with R_{PU} assuming a 50-Ω source impedance and setting the input and output common-mode voltage to mid-supply.

There are two drawbacks to this configuration. One is it requires additional current from the power supply. Using the values shown for a gain of 0 dB requires 10 mA more current with 5-V supply, and 6.5 mA more current with 3.3-V supply.

The other drawback is this configuration also increases the noise gain of the circuit. In the 10-dB gain case, noise gain increases by a factor of 1.7.

Table 4. RPU Values for Various Gains

Gain	R_F	R_G	R_{IT}	R_{PU}
0 dB	499 Ω	487 Ω	54.9 Ω	511 Ω
6 dB	499 Ω	243 Ω	59 Ω	270 Ω
10 dB	499 Ω	150 Ω	68.1 Ω	178 Ω
14 dB	499 Ω	93.1 Ω	82.5 Ω	124 Ω
20 dB	499 Ω	40.2 Ω	221 Ω	80.6 Ω

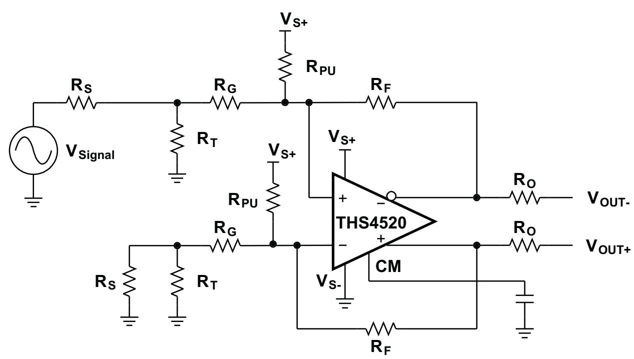


Figure 63. THS4520 DC Coupled Single-Supply with R_{PU} Used to Set V_{IC}

Figure 64 shows AC coupling to the source. Using capacitors in series with the termination resistors allows the amplifier to self-bias both input and output to mid-supply.

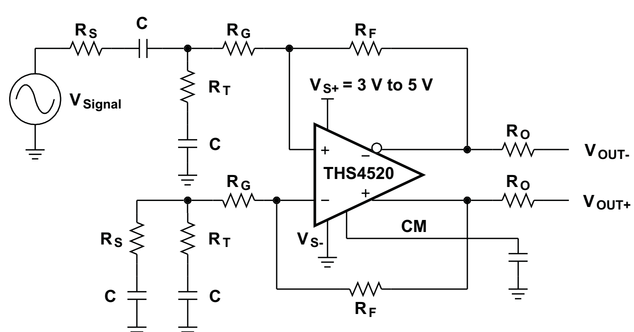


Figure 64. THS4520 AC Coupled Single-Supply

FULLY DIFFERENTIAL AMPLIFIER WITH REDUCED PEAKING

Figure 65 shows a fully differential amplifier that reduces peaking at low gains. The resistor R_C compensates the THS4520 to have higher noise gain (NG), which reduces the AC response peaking (typically 3.8dB at G = +1 without R_C) without changing the DC forward gain. The input signal, V_{IN}, is assumed to be from a low impedance source, such as an op amp.

When the two feedback paths are symmetrical, the noise gain is given by the expression:

$$NG = 1 + \frac{R_F}{R_G} + \frac{2R_F}{R_C} \tag{4}$$

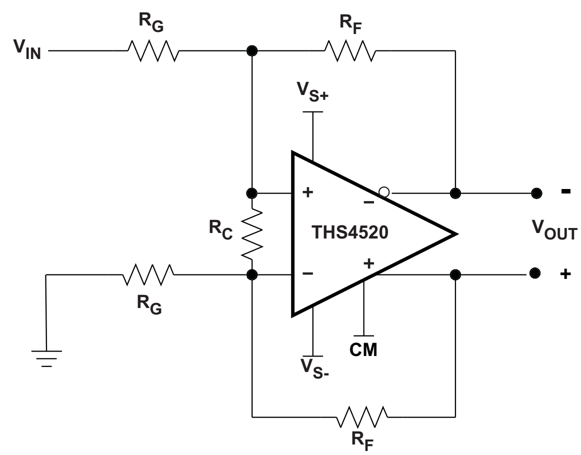


Figure 65. THS4520 with Noise Gain Compensation

A unity-gain buffer can be designed by selecting R_F = 499 Ω, R_G = 499 Ω and R_C = open. The resulting forward gain response is similar to the characteristics plots with G = 0dB (see Figure 1), and the noise gain equal to 2. If R_C is then made equal to 200 Ω the noise gain increases to 7, which typically gives a frequency response with less peaking and with less bandwidth, and the forward gain remains equal to unity.

The plot in Figure 66 shows the measured small-signal AC response of a THS4520 EVM in the default unity-gain configuration (see Figure 72). When the termination resistors present on the EVM (R1, R2, and R12 in Figure 72) and the source resistance of the signal generator (R_S = 50 Ω) are taken into account, the calculated noise gain of the default EVM is NG = 1.97. Also included in the plot are two curves which represent the measured response of the same board with two values of R_C, one with R_C = 200 Ω (NG = 6.96) and one with R_C =487 Ω (NG = 4.02). The low-frequency roll-off of the AC response is due to the transformer (T1 in Figure 72). The curves illustrate the reduced peaking and the reduced bandwidth due to increased noise gain when the circuit is configured for low forward gain. Note that using noise gain compensation increases the circuit output noise and decreases the circuit bandwidth. Compared to the default configuration (no R_C) using R_C = 200 Ω and R_C = 487 Ω increases the circuit output noise by approximately 10.9dB and 6dB respectively.

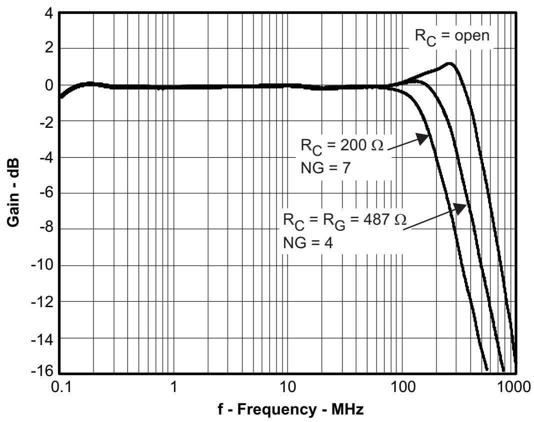


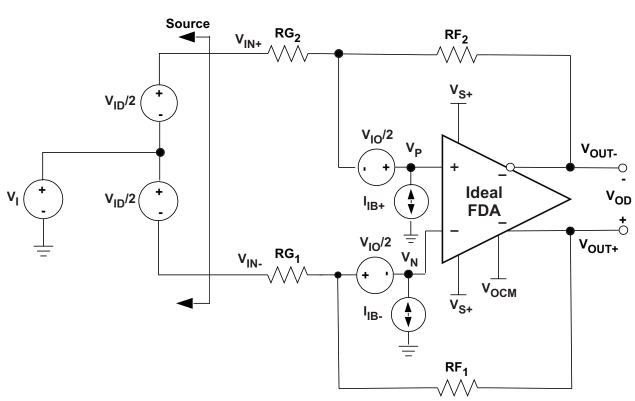
Figure 66. THS4520 EVM Small Signal Response With and Without Noise Gain Compensation

DC ERRORS IN A FULLY DIFFERENTIAL AMPLIFIER

Summary

A DC error model of a fully differential voltage feedback amplifier shown in the following circuit diagram. The output error has four contributing factors in this model:

1. Input offset voltage (V_{IO}).
2. Input offset current (I_{IO}).
3. Input bias currents (I_{IB+}, I_{IB-}) interacting with mismatched feedback networks.
4. Mismatch between input and output common-mode voltages interacting with the mismatched feedback networks.



When there is no mismatch between the feedback networks (RF_1 = RF_2 and RG_1 = RG_2) the output error due to the input offset voltage is given by:

$$\Delta V_{OD}\left(V_{IO}\right) = V_{IO}\frac{RG + RF}{RG} = V_{IO}/\beta \qquad (5)$$

where β is often called the *feedback factor*.

$$\beta = \frac{RG}{RG + RF} \qquad (6)$$

For additional information, see the applications note *Fully Differential Amplifiers* (SLOA054).

The output error due to the input offset current is given by:

$$\Delta V_{OD}\left(I_{IO}\right) = I_{IO}RF \qquad (7)$$

If there is mismatch ($RF_1 \neq RF_2$ or $RG_1 \neq RG_2$), then the output error due to the input bias currents is:

$$\Delta V_{OD}\left(I_{IB}, I_{IO}\right) = 2\frac{I_{IB}\left(R_{EQ1} - R_{EQ2}\right) + I_{IO}\left(R_{EQ1} + R_{EQ2}\right)}{\left(\beta_1 + \beta_2\right)} \qquad (8)$$

Where $I_{IB} = (I_{IB+} + I_{IB-})/2$, $R_{EQ1,2} = RF_{1,2} \parallel RG_{1,2}$ and $\beta_{1,2} = RG_{1,2}/(RG_{1,2} + RF_{1,2})$.

There is an additional contribution to the output error if the input and output common-mode voltages are mismatched:

$$\Delta V_{OD}\left(V_{OCM}, V_{ICM}\right) = 2 \times \left(V_{OCM} - V_{ICM}\right)\frac{\left(\beta_1 - \beta_2\right)}{\left(\beta_1 + \beta_2\right)} \qquad (9)$$

Note that this source of output error will be negligible if the two feedback paths are well matched. The analysis that leads to the results shown above is beyond the scope of this section. An applications note that shows the detailed analysis will be available in the near future.

DEPENDENCE OF HARMONIC DISTORTION ON DEVICE OUTPUT SWING AND SIGNAL FREQUENCY

Typical plots of HD2 or HD3 usually show the dependence of these parameters upon a single variable, like frequency, output swing, load, or circuit gain. Operating conditions of interest are usually dependent on several variables that are often spread across several different plots. This forces the designer to interpolate across several plots in an attempt to capture the parameters and operating conditions for his/her application.

Unlike typical plots where HD2 or HD3 is plotted against a single variable, the plots below show constant contours of THS4520 HD2 and HD3 plotted against the joint parameters of device output swing and signal frequency. These two parameters are of particular interest because their joint interaction reflects the usable slewing and bandwidth limits of a device. Output swing and frequency limits are often prime consideration when picking a device and quantifying their joint impact on HD allows a more precise judgment on the ability of a device to meet the *need for speed*. The curves that separate each colored region represent the value of HD2,3 indicated on the plot. Following a curve over the ranges of output swing and frequency show the conditions over which that value of HD2,3 occurs.

Note that the horizontal axis represents the base-10 logarithm of frequency in units of MHz. So on the horizontal axis the value of ‘2’ represents 100 MHz, ‘1’ represents 10 MHz and ‘0’ represents 1 MHz, respectively. This strategy was chosen to provide spacing between curves that allowed the viewer to easily resolve the individual curves. Plotting frequency on a linear scale caused the curves to be crowded and difficult to distinguish. Unfortunately a semilog axis format was not possible because of the plotting function. The measured data in the plots represent measurements of a THS4520 evaluation board in the default unity-gain configuration with R_L = 200Ω. For more information on the circuit configuration, see the information on the THS4520 evaluation board later in this section.

The first two plots (Figure 67 andFigure 68) are for HD2 and HD3 respectively, with a power supply of ±2.5 V. The line labeled *Large Signal BW* in each of the two plots represents the measured large signal bandwidth over the range of output signal swing in the plot (V_{out} = 1 V_{pp} to 8 V_{pp}). The BW lines fall in the shaded region that represents very poor distortion performance: HD2 > –45dBc or HD3 > –40dBc. The intent in plotting the bandwidth was to provide a realistic comparison between the reported large signal bandwidth and useful distortion performance. The areas between the plots are shaded to help illustrate the 10dB changes in HD2 or HD3 between the adjacent curves. The third and fourth plots (Figure 69andFigure 70) are the constant contours of HD2 and HD3 respectively for a power supply of ±1.65 V.

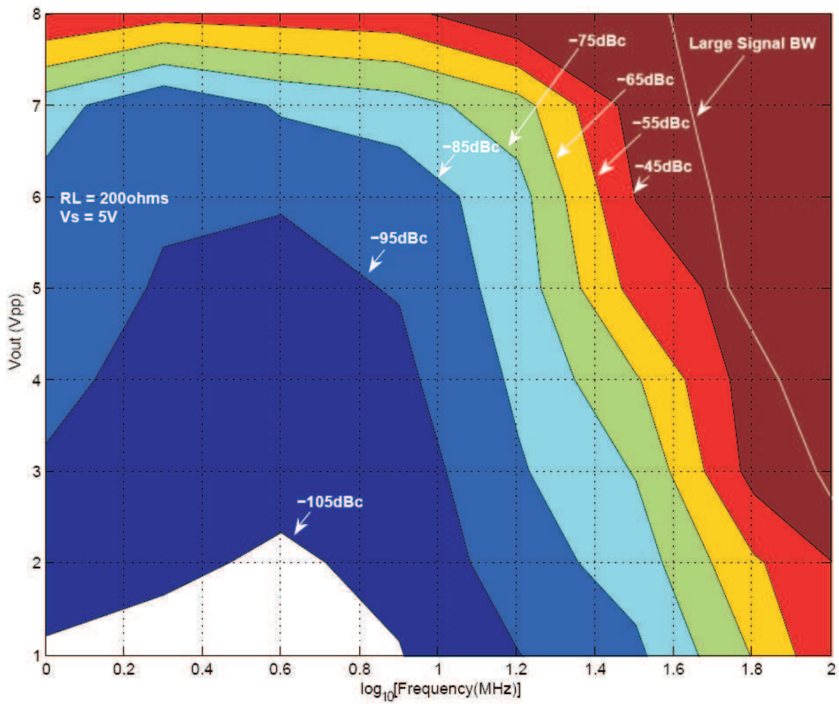


Figure 67. Constant HD2 Contours vs Output Swing and $\log_{10}$ (Frequency - MHz)
V_S = 2.5 V, Gain = 1, R_L = 200 Ω

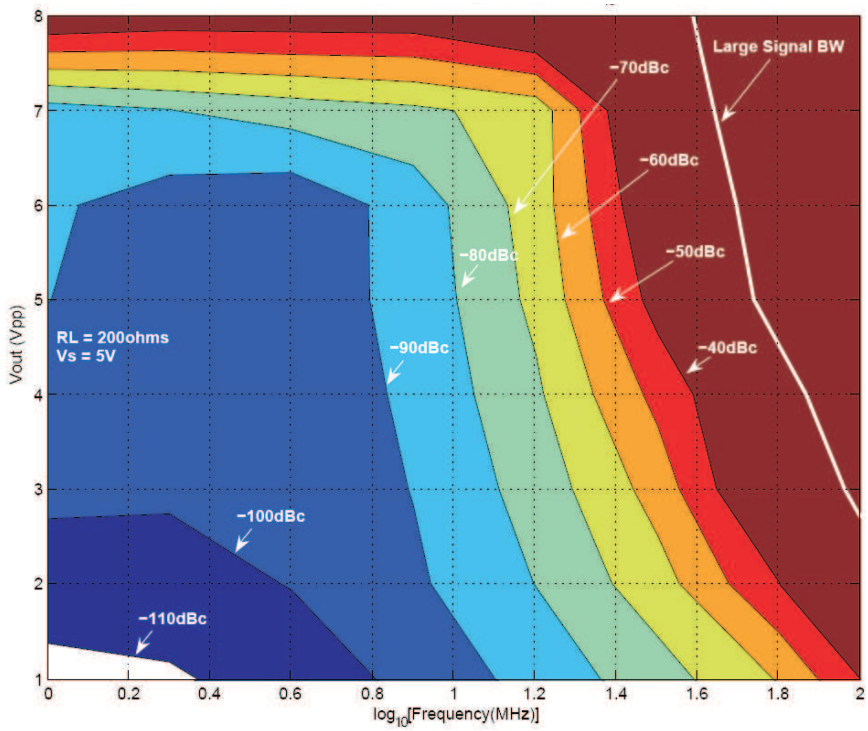


Figure 68. Constant HD3 Contours vs Output Swing and $\log_{10}$ (Frequency - MHz) V_S = 2.5 V, Gain = 1, R_L = 200 Ω

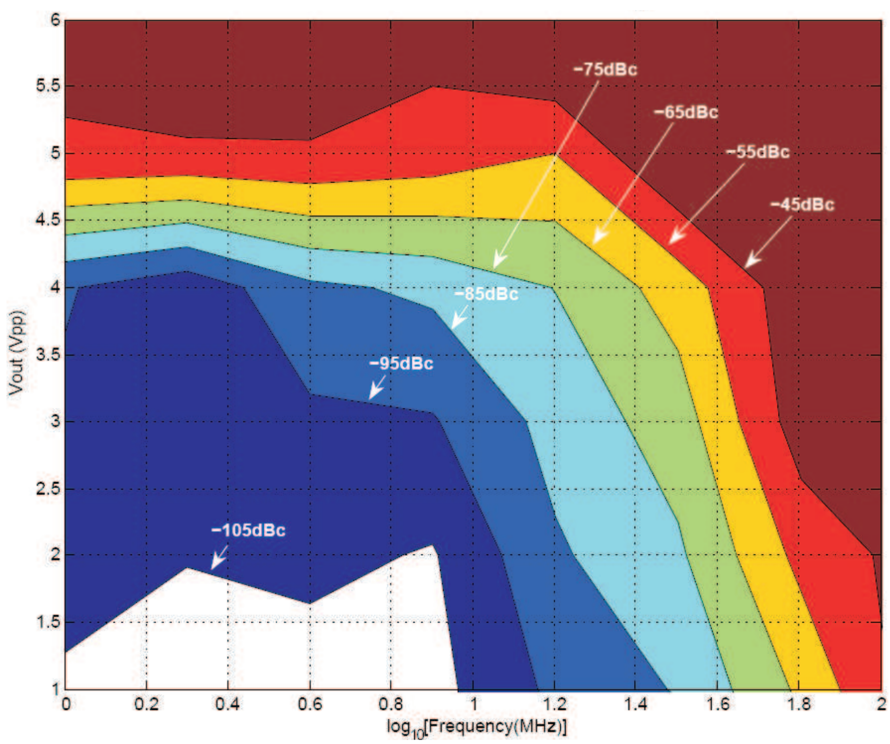


Figure 69. Constant HD2 Contours vs Output Swing and $\log_{10}$ (Frequency - MHz) V_S = 1.65 V, Gain = 1, R_L = 200 Ω

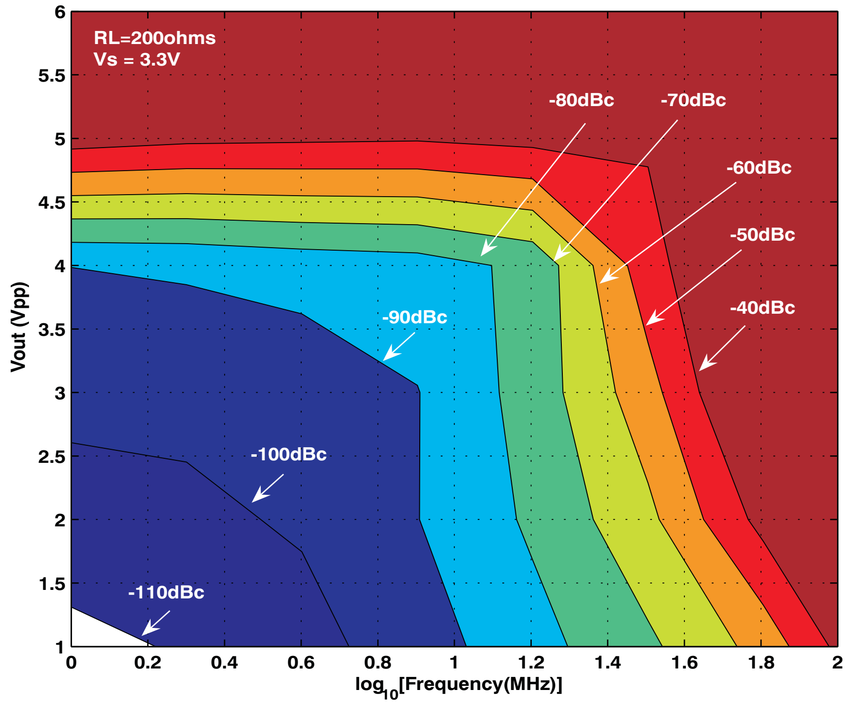


Figure 70. Constant HD2 Contours vs Output Swing and $\log_{10}$ (Frequency - MHz)
V_S = 1.65 V, Gain = 1, R_L = 200 Ω

Layout Recommendations

It is recommended to follow the layout of the external components near the amplifier, ground plane construction, and power routing of the EVM as closely as possible. General guidelines are:

1. Signal routing should be direct and as short as possible into and out of the op amp circuit.
2. The feedback path should be short and direct avoiding vias.
3. Ground or power planes should be removed from directly under the amplifier's input and output pins.
4. An output resistor is recommended on each output, as near to the output pin as possible.
5. Two 10-µF and two 0.1-µF power-supply decoupling capacitors should be placed as near to the power-supply pins as possible.
6. Two 0.1-µF capacitors should be placed between the CM input pins and ground. This limits noise coupled into the pins. One each should be placed to ground near pin 4 and pin 9.
7. It is recommended to split the ground pane on layer 2 (L2) as shown below and to use a solid ground on layer 3 (L3). A single-point connection should be used between each split section on L2 and L3.
8. A single-point connection to ground on L2 is recommended for the input termination resistors R1 and R2. This should be applied to the input gain resistors if termination is not used.
9. The THS4520 recommended PCB footprint is shown in Figure 71.

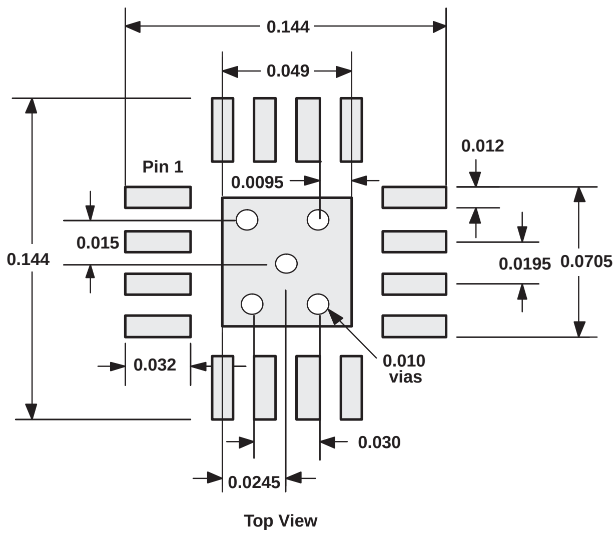


Figure 71. QFN Etch and Via Pattern

THS4520 EVM

Figure 72 is the THS4520 EVAL1 EVM schematic, layers 1 through 4 of the PCB are shown Figure 73, and Table 5 is the bill of material for the EVM as supplied from TI.

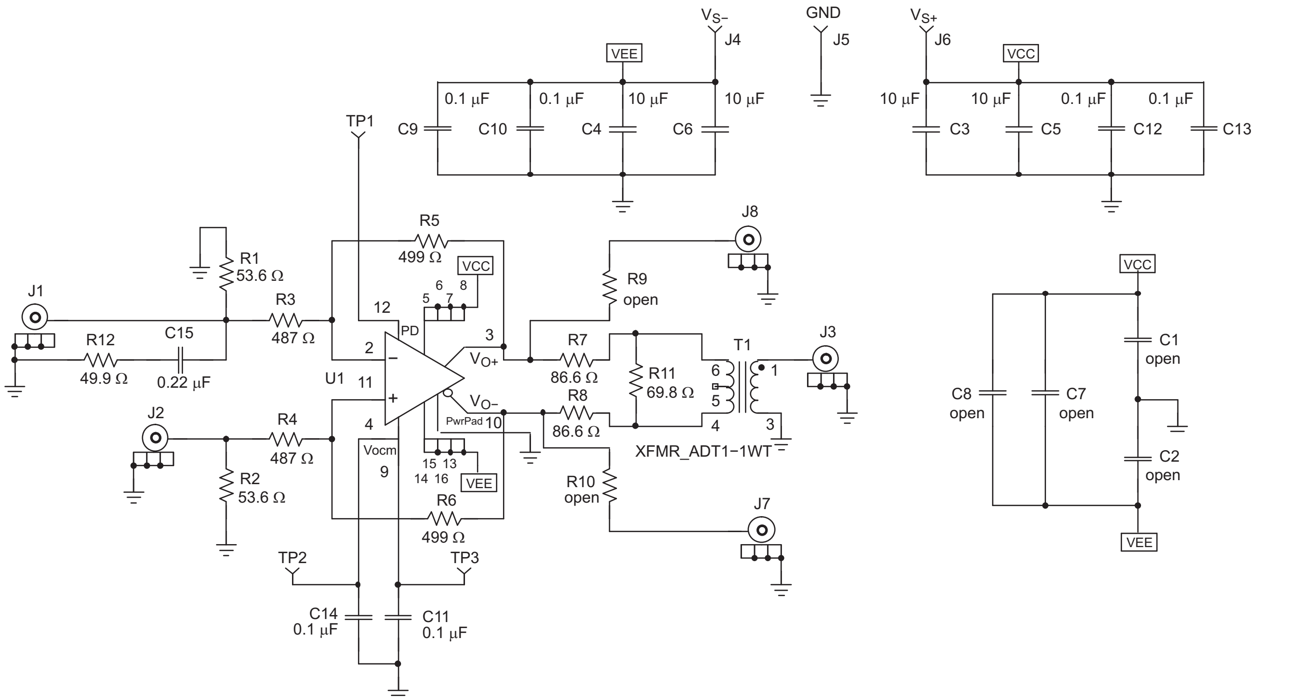


Figure 72. THS4520 EVAL1 EVM Schematic

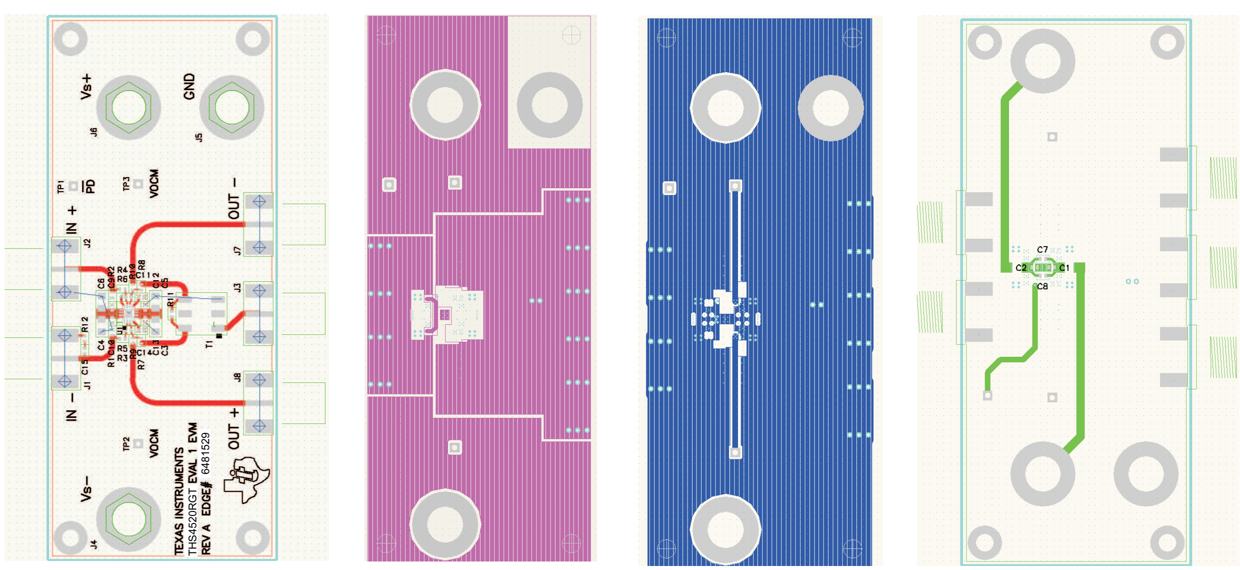


Figure 73. THS4520 EVAL1 EVM Layer 1 through 4

Table 5. THS4520 EVAL1 EVM Bill of Materials

ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	PCB QTY	MANUFACTURER'S PART NUMBER
1	CAP, 10.0 µF, Ceramic, X5R, 6.3V	0805	C3, C4, C5, C6	4	(AVX) 08056D106KAT2A
2	CAP, 0.1 µF, Ceramic, X5R, 10V	0402	C9, C10, C11, C12, C13, C14	6	(AVX) 0402ZD104KAT2A
3	CAP, 0.22 ΩF, Ceramic, X5R, 6.3V	0402	C15	1	(AVX) 04026D224KAT2A
4	OPEN	0402	C1, C2, C7, C8	4	
5	OPEN	0402	R9, R10	2	
6	Resistor, 49.9 Ω, 1/16W, 1%	0402	R12	1	(KOA) RK73H1ETTP49R9F
7	Resistor, 53.6 Ω, 1/16W, 1%	0402	R1, R2	2	(KOA) RK73H1ETTP53R6F
8	Resistor, 69.8 Ω, 1/16W, 1%	0402	R11	1	(KOA) RK73H1ETTP69R8F
9	Resistor, 86.6 Ω, 1/16W, 1%	0402	R7, R8	2	(KOA) RK73H1ETTP86R6F
10	Resistor, 487 Ω, 1/16W, 1%	0402	R3, R4	2	(KOA) RK73H1ETTP4870F
11	Resistor, 499 Ω, 1/16W, 1%	0402	R5, R6	2	(KOA) RK73H1ETTP4990F
12	Transformer, RF		T1	1	(MINI-CIRCUITS) ADT1-1WT
13	Jack, banana receptance, 0.25" diameter hole		J4, J5, J6	3	(HH SMITH) 101
14	OPEN		J1, J7, J8	3	
15	Connector, edge, SMA PCB Jack		J2, J3	2	(JOHNSON) 142-0701-801
16	Test point, Red		TP1, TP2, TP3	3	(KEYSTONE) 5000
17	IC, THS4520		U1	1	(TI) THS4520RGT
18	Standoff, 4-40 HEX, 0.625" length			4	(KEYSTONE) 1808
19	SCREW, PHILLIPS, 4-40, 0.250"			4	SHR-0440-016-SN
20	Printed circuit board			1	(TI) EDGE# 6481529

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 3 V to 5 V and the output voltage range of 3 V to 5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85 = C. The EVM is designed to operate properly with certain components above 85 = C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4520RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4520	Samples
THS4520RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4520	Samples
THS4520RGTTG4	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4520	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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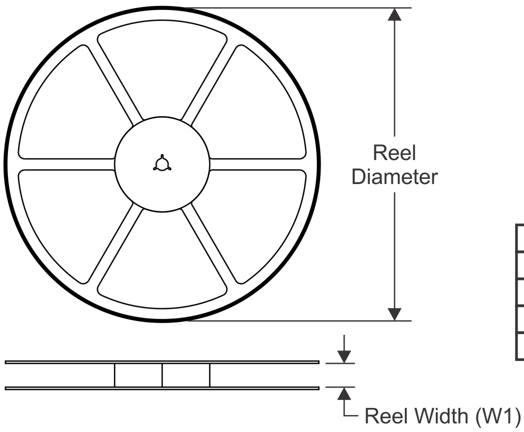
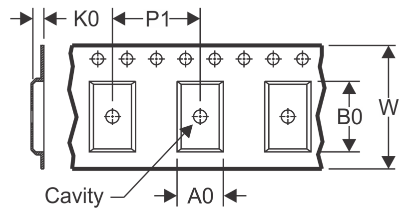
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

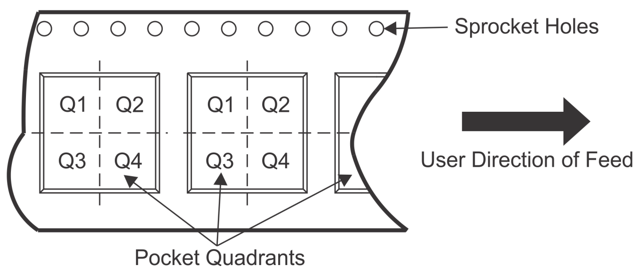


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

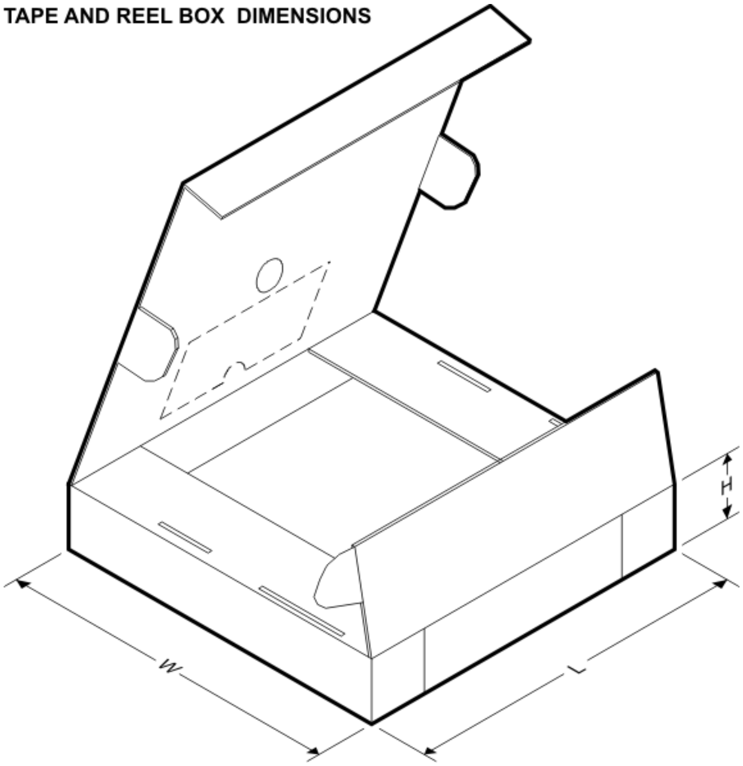
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4520RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THS4520RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

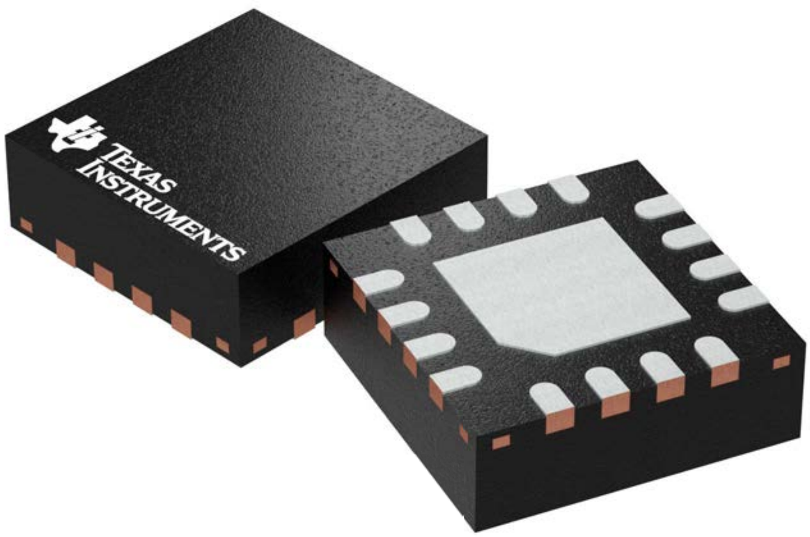


*All dimensions are nominal

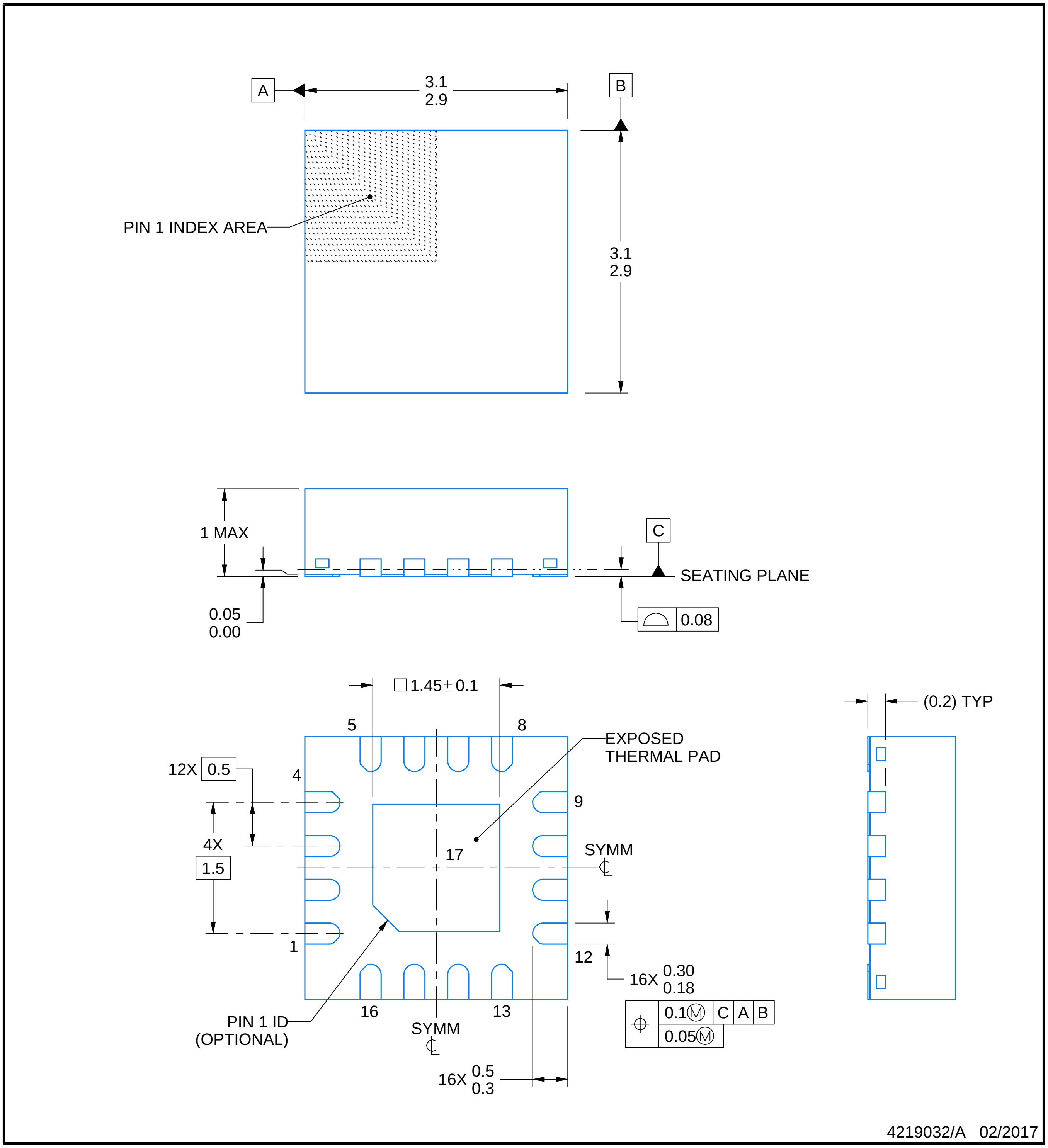
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4520RGTR	VQFN	RGT	16	3000	853.0	449.0	35.0
THS4520RGTT	VQFN	RGT	16	250	210.0	185.0	35.0

RGT 16 — VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

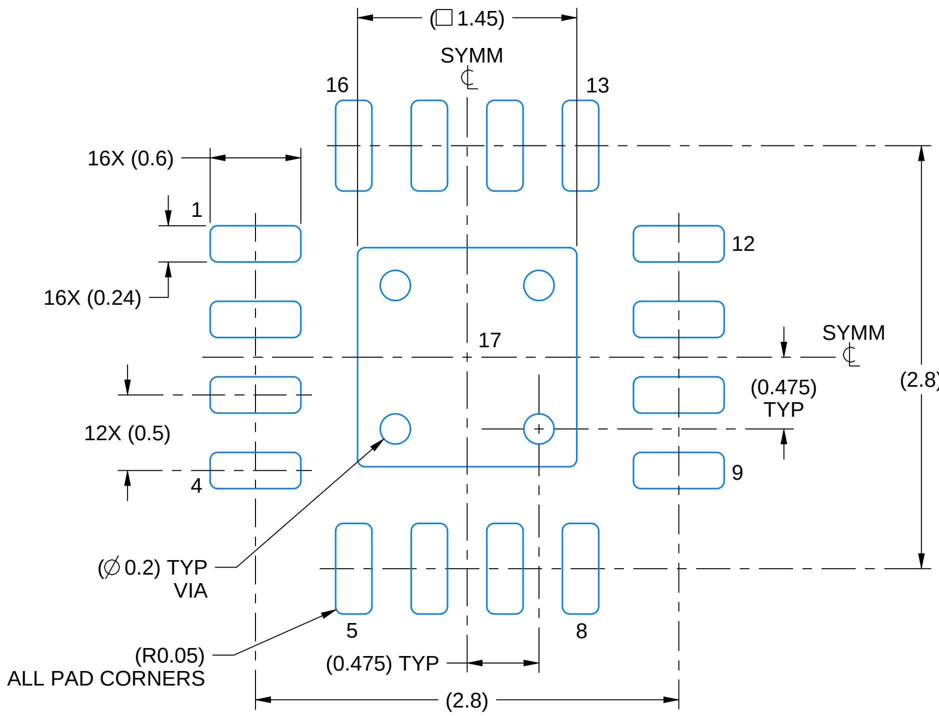


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

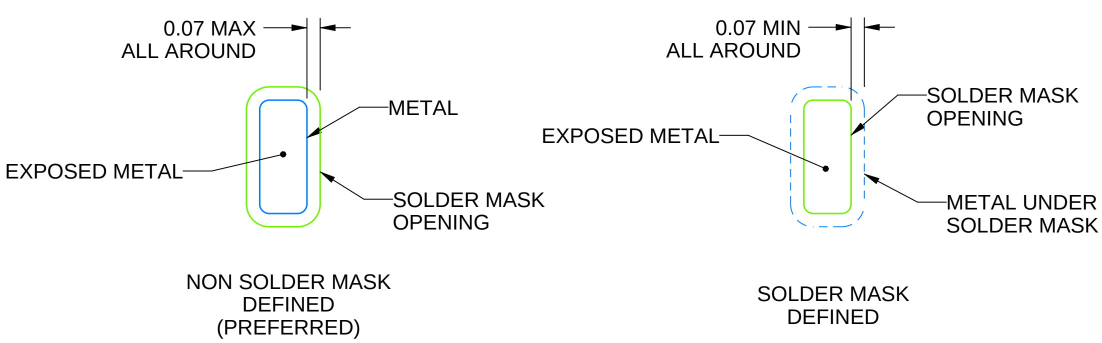


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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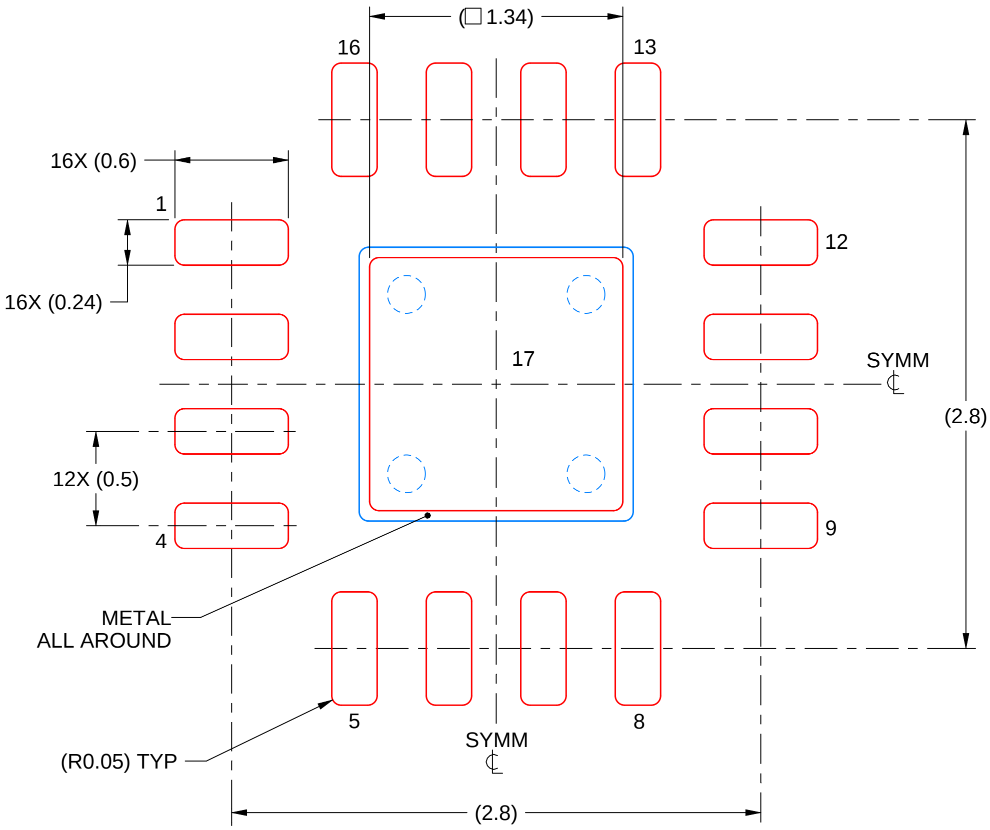
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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