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FAIRCHILD SEMICONDUCTOR®

October 2013

FDPF3N50NZ

N-Channel UniFET^{TM} II MOSFET

500 V, 3 A, 2.5 Ω

Features

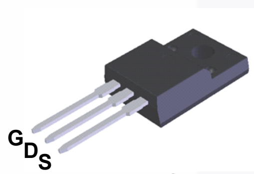
- $R_{DS(on)}$ = 2.1 Ω (Typ.) @ V_{GS} = 10 V, I_D = 1.5 A
- Low Gate Charge (Typ. 6.2 nC)
- Low C_{rss} (Typ. 2.5 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Improved Capability
- RoHS Compliant

Applications

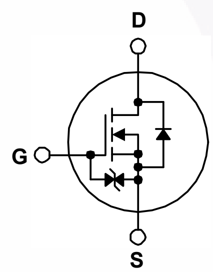
- LCD/LED TV
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

Description

UniFET^{TM} II MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET II MOSFET to withstand over 2kV HBM surge stress. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



TO-220F



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter			FDPF3N50NZ	Unit
V_{DSS}	Drain to Source Voltage			500	V
V_{GSS}	Gate to Source Voltage			±25	V
I_D	Drain Current	- Continuous (T_C = 25°C)		3*	A
		- Continuous (T_C = 100°C)		1.8*	
I_{DM}	Drain Current	- Pulsed	(Note 1)	12*	A
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	113	mJ
I_{AR}	Avalanche Current		(Note 1)	3	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	5.4	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	10	V/ns
P_D	Power Dissipation	(T_C = 25°C)		27	W
		- Derate above 25°C		0.21	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds			300	°C

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FDPF3N50NZ	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	4.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDPF3N50NZ	FDPF3N50NZ	TO-220F	Tube	N/A	50 units

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V, T_C = 25°C	500	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25°C	-	0.5	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 400V, V_{GS} = 0V,T_C = 125°C	-	-	10	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±25V, V_{DS} = 0V	-	-	±10	μA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 1.5A	-	2.1	2.5	Ω
g_{FS}	Forward Transconductance	V_{DS} = 20V, I_D = 1.5A	-	1.9	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V f = 1MHz	-	210	280	pF
C_{oss}	Output Capacitance		-	30	45	pF
C_{rss}	Reverse Transfer Capacitance		-	2.5	5	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 400V I_D = 3A V_{GS} = 10V (Note 4)	-	6.2	9	nC
Q_{gs}	Gate to Source Gate Charge		-	1.4	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	3.1	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250V, I_D = 3A V_{GS} = 10V, R_{GEN} = 25Ω (Note 4)	-	10	30	ns
t_r	Turn-On Rise Time		-	15	40	ns
$t_{d(off)}$	Turn-Off Delay Time		-	26	60	ns
t_f	Turn-Off Fall Time		-	17	45	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	3	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	12	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_{SD} = 3A	-	-	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_{SD} = 3A dI_F/dt = 100A/μs	-	190	-	ns
Q_{rr}	Reverse Recovery Charge		-	0.52	-	μC

Notes:
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 25mH, I_{AS} = 3A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3. I_{SD} ≤ 3A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Characteristics

Figure 1. On-Region Characteristics

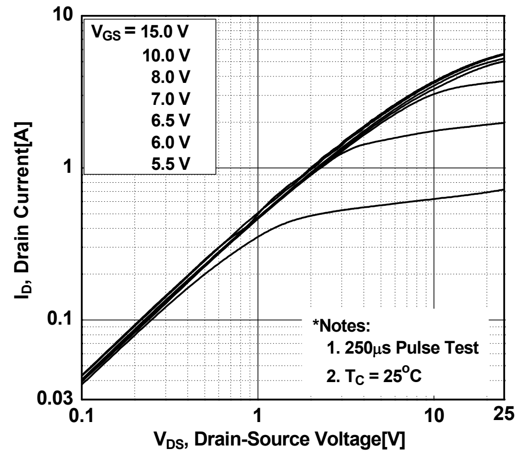


Figure 2. Transfer Characteristics

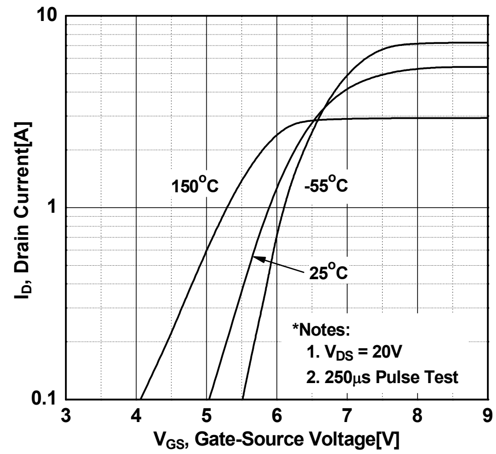


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

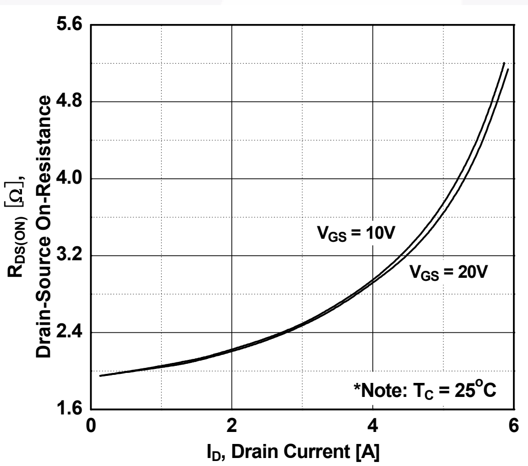


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

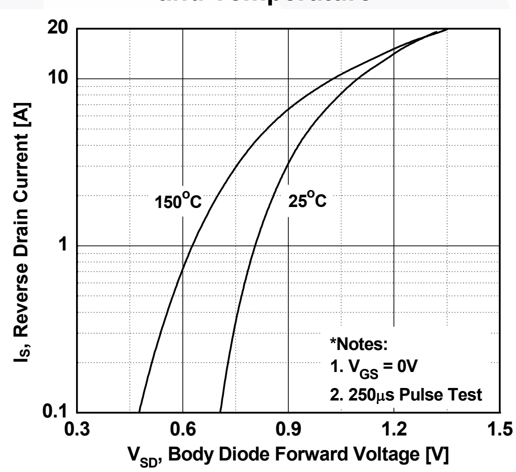


Figure 5. Capacitance Characteristics

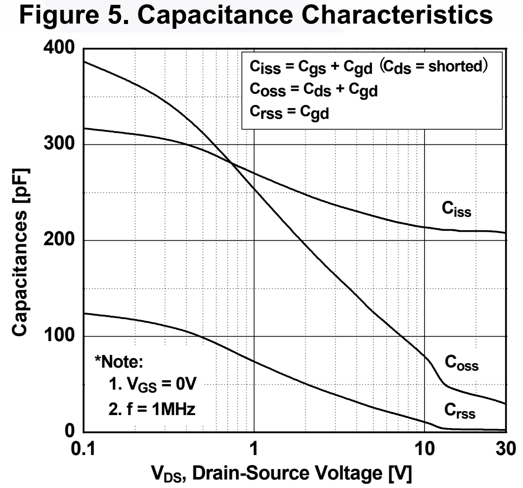
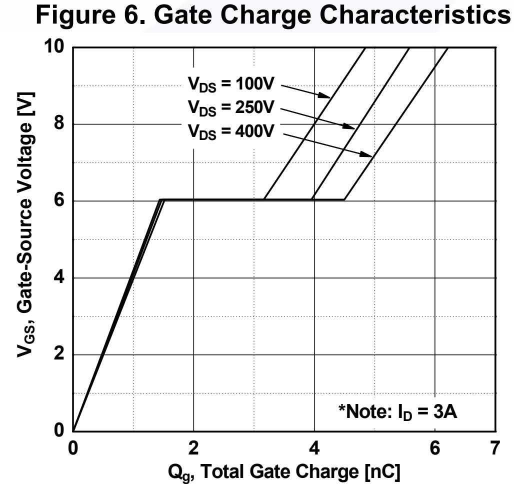


Figure 6. Gate Charge Characteristics



Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

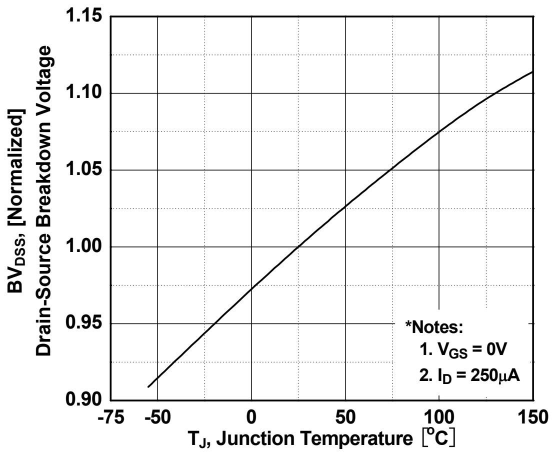


Figure 8. On-Resistance Variation vs. Temperature

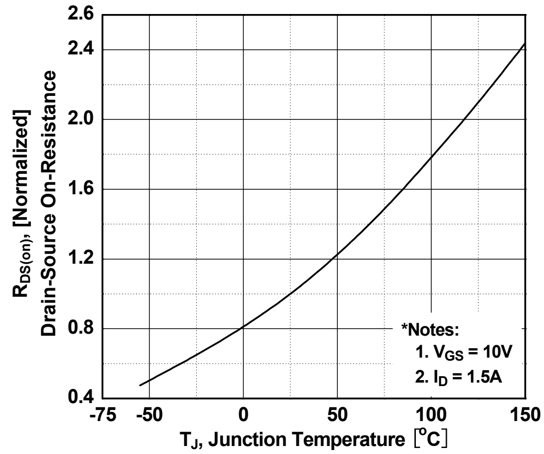


Figure 9. Maximum Safe Operating Area vs. Case Temperature-FDPF3N50NZ

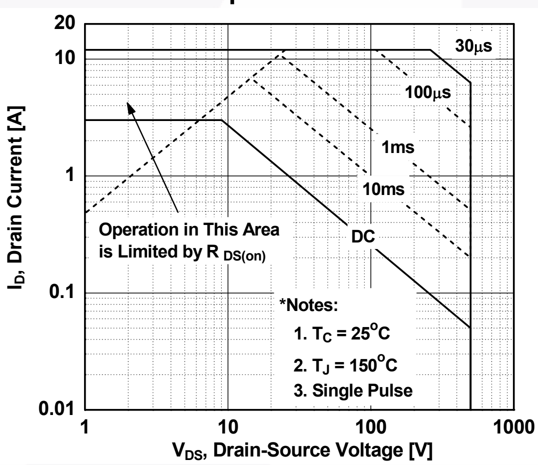


Figure 10. Maximum Drain Current

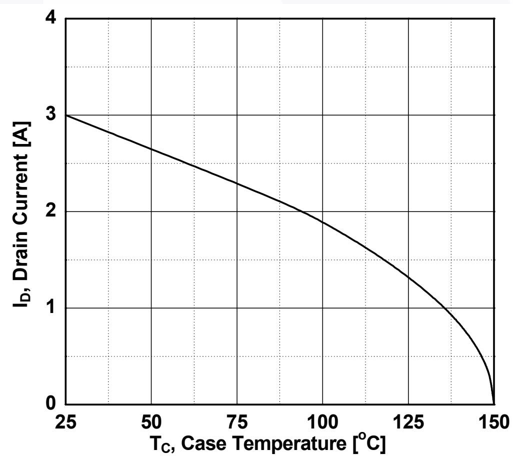
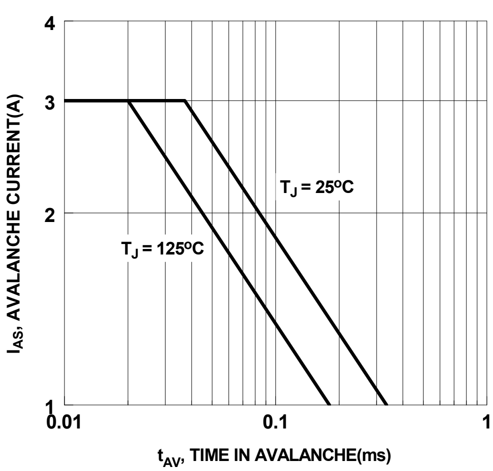


Figure 11. Unclamped Inductive Switching Capability



Typical Characteristics (Continued)

Figure 12. Transient Thermal Response Curve- FDPF3N50NZ

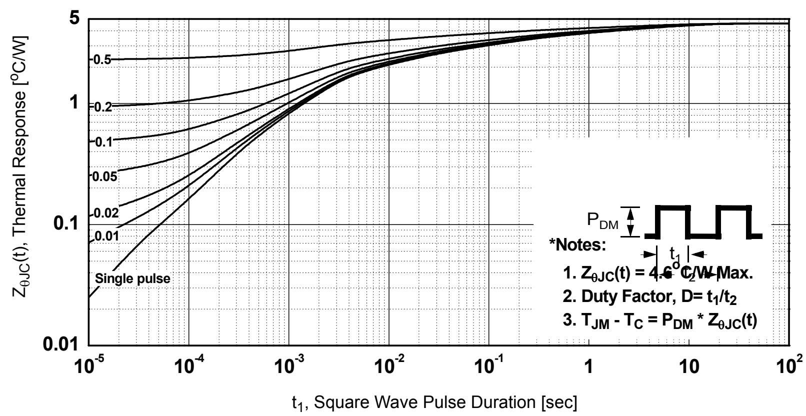


Figure 13. Gate Charge Test Circuit & Waveform

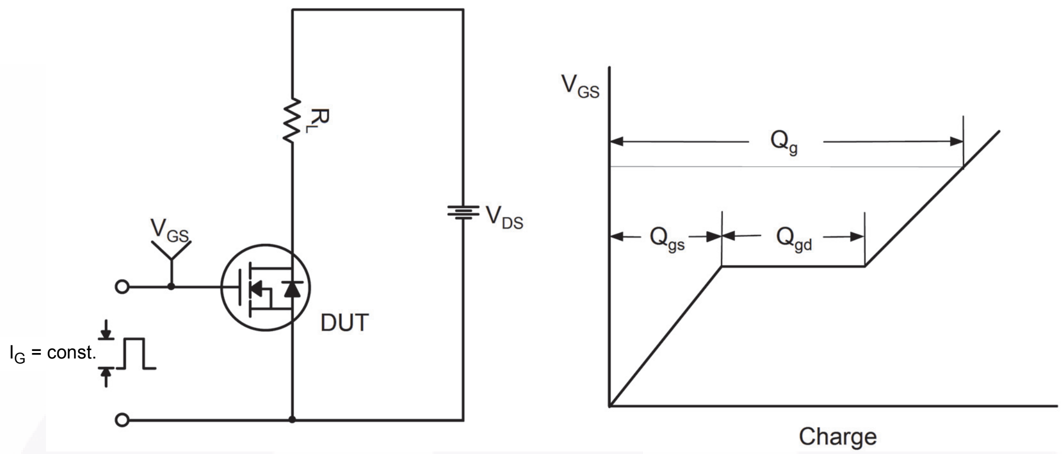


Figure 14. Resistive Switching Test Circuit & Waveforms

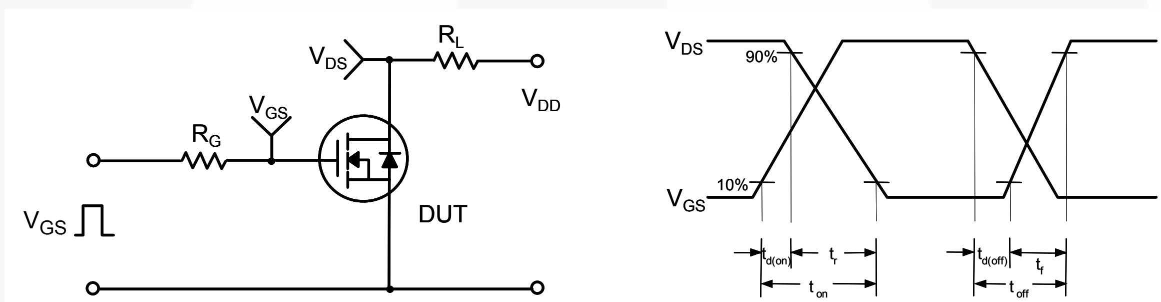


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

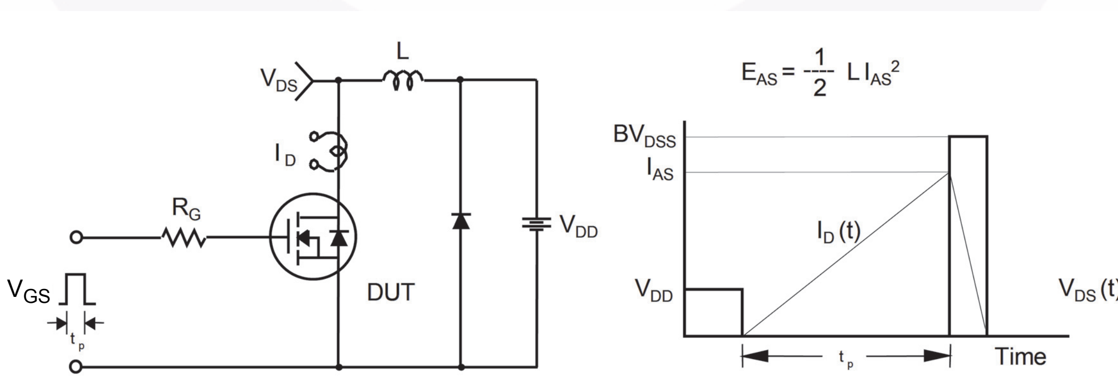
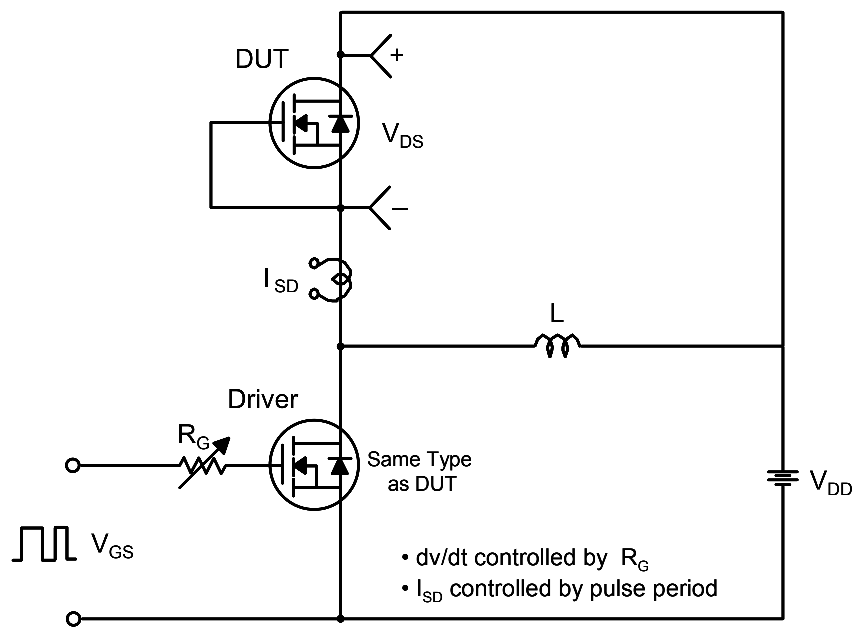
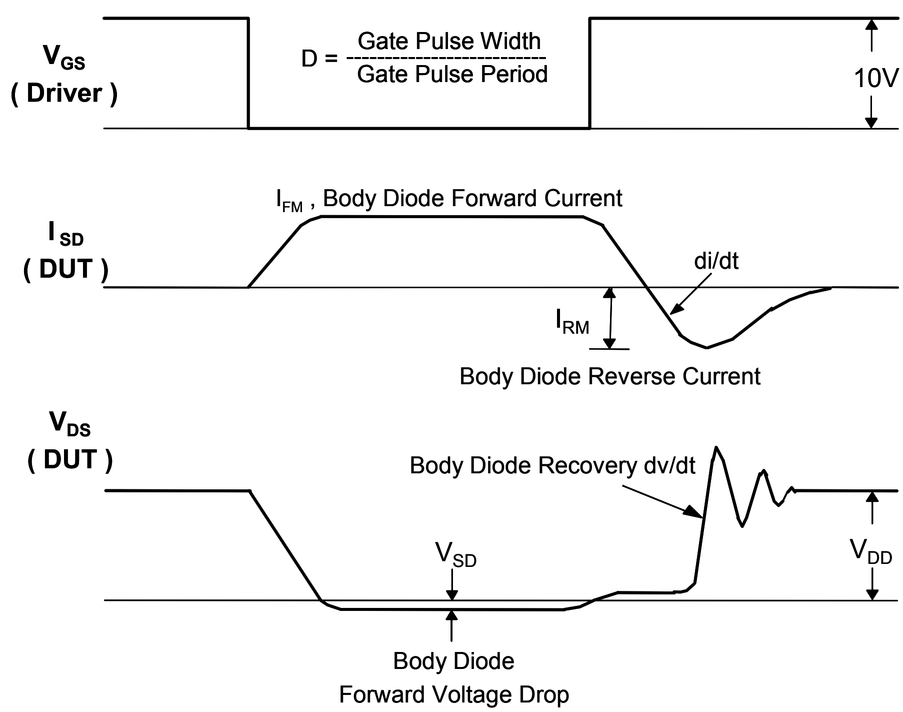


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms





Mechanical Dimensions

TO-220F 3L

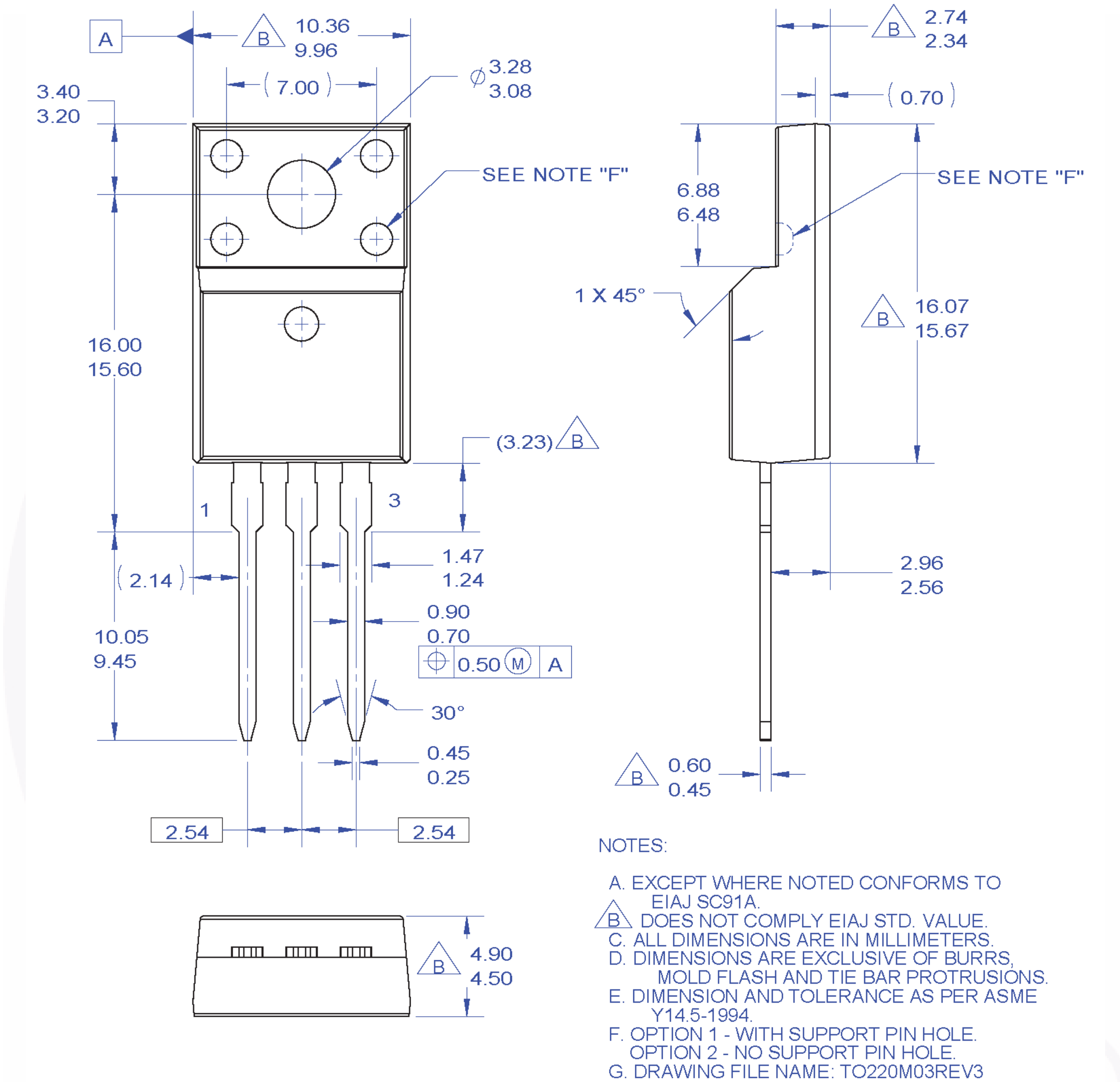


Figure 17. TO220, Molded, 3LD, Full Pack, EIAJ SC91, Straight Lead

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Dimension in Millimeters

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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Rev. I66

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