SAM L21 Family

SAM L21 Family Silicon Errata and Data Sheet Clarification

SAM L21 Family

The SAM L21 family of devices that you have received conform functionally to the current Device Data Sheet DS60001477A, except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1.

The errata described in this document will be addressed in future revisions of the SAM L21 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in 2. Data Sheet Clarifications, following the discussion of silicon issues.

Table 1. SAM L21 Silicon Device Identification

Part Number	Device Identification (DID[31:0])	Revision ID (DID.REVISION[3:0])	
		B	C
ATSAML21J18B	0x10810x0F	0x1	0x2
ATSAML21J17B	0x10810x10		
ATSAML21J16B	0x10810x11		
ATSAML21G18B	0x10810x14		
ATSAML21G17B	0x10810x15		
ATSAML21G16B	0x10810x16		
ATSAML21E18B	0x10810x19		
ATSAML21E17B	0x10810x1A		
ATSAML21E16B	0x10810x1B		
ATSAML21E15B	0x10810x1C		

Note: Refer to the “Device Services Unit” chapter in the current device data sheet (DS60001477A) for detailed information on device identification and revision IDs for your specific device.

Silicon Errata Summary

Table 2. Silicon Errata Issue Summary

Module	Feature	Errata Number	Issue Summary	Affected Revisions	
				B	C
DSU	Wake-up From Standby Retention Mode	1.1.1	When device is waking from Standby Retention mode, selected alternate function on PA30 (for example, SERCOM) will be lost and it functions as the SWCLK pin and can switch device to Debug mode.	X	X
PM	Low-Power Configuration	1.2.1	If the PM.STDBYCFG.VREGSMOD field is set to 2 (low-power configuration), the oscillator source driving the GCLK_MAIN clock will still be running in Standby mode causing extra consumption.	X	
DFLL48M	Write Access to DFLL Register	1.3.1	The DFLL clock must be requested before being configured, otherwise a write access to a DFLL register can freeze the device.	X	X
DFLL48M	Out of Bounds Interrupt	1.3.2	If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated.	X	X
DFLL48M	DFLL Status Bit in USB Clock Recovery Mode	1.3.3	The DFLL status bits in the STATUS register, during the USB clock recovery mode, can be wrong after a USB suspend state.	X	X
DMAC	Disable a Trigger from the Module	1.4.1	A write from DMAC to a register in a module to disable a trigger from the module to DMAC, does not work in Standby mode.	X	
DMAC	Linked Descriptor	1.4.2	When using many DMA channel, if one of these DMA channels has a linked descriptor, a fetch error can appear on this channel.	X	X
DMAC	Linked Descriptors	1.4.3	When at least one channel using linked descriptors is already active, enabling another DMA channel (with or without linked descriptors) can result in a channel Fetch Error (FERR) or an incorrect descriptor fetch.	X	X
FDPLL96M	FDPLL Jitter	1.5.1	Maximum FDPLL input reference clock frequency (fGCLK_DPLL) does not meet the published specification.	X	
FDPLL96M	DPLLRATIO Register	1.5.2	When FDPLL ratio value in the DPLLRATIO register is changed on the fly, the STATUS.DPLLLDRTO will not be set even though the ratio is updated.	X	X
PORT	PORT Read/Write on Non-Implemented Register	1.6.1	PORT read/write attempts on non-implemented registers, including addresses beyond the last implemented register group (PA, PB), do not generate a PAC protection error.	X	X
PORT	Pull-up and Pull-down Configurations on PA24 and PA25 Pins	1.6.2	On PA24 and PA25 pins, the pull-up and pull-down configuration is not disabled automatically when alternative pin function is enabled.	X	X
SUPC	Buck Converter Mode	1.7.1	Digital Phase-Locked Loop (FDPLL96M) and Digital Frequency-Locked Loop (DFLL48M) PLL's cannot be used with main voltage regulator in Buck converter mode.	X	X
SUPC	Buck Converter as a Main Voltage Regulator	1.7.2	When Buck converter is set as main voltage regulator (SUPC.VREG.SEL=1), the microcontroller can freeze when leaving Standby mode.	X	X
ADC	ADC Result in Unipolar Mode	1.8.1	The LSB of ADC result is stuck at zero in Unipolar mode for 8-bit and 10-bit resolution.	X	X
ADC	Window Monitor	1.8.2	When window monitor is enabled and its output is 0, the ADC GCLK is kept running.	X	

.....continued

Module	Feature	Errata Number	Issue Summary	Affected Revisions	
				B	C
ADC	Free-Running Mode	1.8.3	In Standby Sleep mode when the ADC is in free-running mode (CTRLC.FREERUN=1) and the RUNSTDBY bit is set to 0 (CTRLA.RUNSTDBY=0), the ADC keeps requesting its generic clock.	X	X
ADC	SYNCBUSY.SWTRIG Bit	1.8.4	ADC SYNCBUSY.SWTRIG get stuck to one after wake-up from Standby Sleep mode.	X	X
TC	SYNCBUSY Flag	1.9.1	When clearing the STATUS.PERBUFV/STATUS.CCBUFVx flags, the SYNCBUSY.PER/SYNCBUSY.CCx flags are released before the PERBUF/CCBUFx registers are restored to their expected value.	X	X
TCC	Advance Capture Mode	1.10.1	Advance Capture mode (CAPTMIN CAPTMAX LOCMIN LOCMAX DERIV0) doesn't work if an upper channel is not in one of these modes.	X	X
TCC	SYNCBUSY Flag	1.10.2	When clearing the STATUS.xxBUFV flag, SYNCBUSY is released before the register is restored to its appropriate value.	X	X
TCC	MAX Capture Mode	1.10.3	In Capture mode while using max Capture mode, with the timer set in Up-Counting mode, if an input event occurred within two cycles before TOP, the value captured is zero instead of TOP.	X	X
TCC	Dithering Mode	1.10.4	Using TCC in Dithering mode with external retrigger events can lead to unexpected stretch of right aligned pulses, or shrink of left aligned pulses.	X	X
SERCOM	USART in Auto-Baud Mode	1.11.1	In USART Auto-Baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.	X	X
SERCOM	SDA and SCL Fall Time	1.11.2	When configured in HS or FastMode+, SDA and SCL fall times are shorter than I^2C specification requirement and can lead to reflection.	X	X
DAC	STATUS.READY Bit	1.12.1	If CLK_APB_DAC is slower than GCLK_DAC, the STATUS.READY bit may never be set.	X	
DAC	STATUS.READY is Not Cleared	1.12.2	If the DAC is enabled, STATUS.READY is not cleared during standby and will remain one after waking up, even though the DAC needs to reinitialize.	X	
DAC	SYNCBUSY.ENABLE Bit	1.12.3	The SYNCBUSY.ENABLE bit is stuck at 1 after disabling and enabling the DAC when refresh is used.	X	X
DAC	SYNCBUSY.DATA1 and SYNCBUSY.DATABUF1	1.12.4	For specific DAC configurations, the SYNCBUSY.DATA1 and SYNCBUSY.DATABUF1 may be stuck at 1.	X	X
DAC	VOUT Value	1.12.5	The desired VOUT value may not be reached at the first DAC conversion after the device power-up or after wake-up from standby.	X	X
DAC	DMA as Input to the DAC	1.12.6	When using the DMA as an input to the DAC, the previous target DAC VOUT value may not be reached when the DMA trigger DAC Empty triggers a new DMA write to the DAC to start a new DAC conversion.	X	X
ADC	Effective Number of Bits	1.13.1	The ADC Effective number of Bits (ENOB) is 9.2 in this revision.	X	
ADC	Power Consumption	1.13.2	Over consumption for up to 1.6 seconds on VDDANA when the ADC is disabled either manually or automatically.	X	
EIC	EIC_ASYNCH Register	1.14.1	Access to the EIC_ASYNCH register in 8-bit or 16-bit mode is not functional.	X	X

.....continued

Module	Feature	Errata Number	Issue Summary	Affected Revisions	
				B	C
EIC	Low Level or Rising Edge or Both Edges	1.14.2	When the EIC is configured to generate an interrupt on a low level or rising edge or both edges (CONFIGn.SENSEx) with the filter enabled (CONFIGn.FILTENx), a spurious flag might appear.	X	X
EIC	NMI Configuration	1.14.3	Changing the NMI configuration (CONFIGn.SENSEx) on the fly may lead to a false NMI interrupt.	X	X
EIC	Asynchronous Edge Detection	1.14.4	When the asynchronous edge detection is enabled, and the system is in Standby mode, only the first edge will generate an event.	X	X
TRNG	Power Consumption in Standby Mode	1.15.1	When TRNG is disabled, some internal logic could continue to operate causing an over consumption.	X	X
EVSYS	Synchronous Path	1.16.1	Using synchronous, spurious overrun can appear with generic clock for the channel always on.	X	X
EVSYS	Overrun Flag	1.16.2	The acknowledge between an event user and the EVSYS clears the CHSTATUS.CHBUSYn bit before this information is fully propagated in the EVSYS one GCLK_EVSYS_CHANNEL_n clock cycle later which triggers and overrun flag.	X	X

Table of Contents

1. Silicon Errata Issues

The following issues apply to the SAM L21 family of devices.

Note: The silicon errata listed in this document supersedes the Errata Chapter 51 in SAM L21 product data sheet (DS60001477A).

1.1 Device Service Unit (DSU)

1.1.1 Wake-up From Standby Retention Mode Reference:16144

When device is waking from Standby Retention mode, selected alternate function on PA30 (for example, SERCOM) will be lost and it functions as the SWCLK pin and can switch device to Debug mode.

Workaround

Disable the debugger hot plug-in detection by setting the security bit. Security is set by issuing the NVMCTRL SSB command.

Affected Silicon Revisions

B	C					
X	X					

1.2 Power Manager (PM)

1.2.1 Low-Power Configuration Reference:14539

If the PM.STDBYCFG.VREGSMOD field is set to 2 (low-power configuration), the oscillator source driving the GCLK_MAIN clock will still be running in Standby mode causing extra consumption.

Workaround

Before entering Standby mode, switch the GCLK_MAIN to the OSCULP32K clock. After wake-up, switch back to the GCLK_MAIN clock.

Affected Silicon Revisions

B	C					
X						

1.3 48 MHz Digital Frequency-Locked Loop (DFLL48M)

1.3.1 Write Access to DFLL Register Reference:9905

The DFLL clock must be requested before being configured, otherwise a write access to a DFLL register can freeze the device.

Workaround

Write a zero to the DFLL ONDEMAND bit in the DFLLCTRL register before configuring the DFLL module.

Affected Silicon Revisions

B	C					
X	X					

1.3.2 Out of Bounds Interrupt Reference:16192

If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated. These interrupts will be generated even if the final calibration values at DFLL48M lock are not at maximum or minimum, and might therefore be false out of bounds interrupts.

Workaround

Check the lock bits, DFLLLCKC and DFLLLCKF, in the OSCCTRL Interrupt Flag Status and Clear register (INTFLAG) are both set before enabling the DFLLOOB interrupt.

Affected Silicon Revisions

B	C					
X	X					

1.3.3 DFLL Status Bit in USB Clock Recovery Mode Reference:16193

The DFLL status bits in the STATUS register, during the USB clock recovery mode, can be wrong after a USB suspend state.

Workaround

Do not monitor the DFLL status bits in the STATUS register during the USB clock recovery mode.

Affected Silicon Revisions

B	C					
X	X					

1.4 Direct Memory Access Controller (DMAC)

1.4.1 Disable a Trigger from the Module Reference:14648

A write from DMAC to a register in a module to disable a trigger from the module to DMAC, does not work in Standby mode. (that is, DAC and SERCOM in Transmission mode).

Workaround

If the module generating the trigger also generates the event, use event interface instead of triggers with DMAC.

Affected Silicon Revisions

B	C					
X						

1.4.2 Linked Descriptor Reference:15670

When using many DMA channel, if one of these DMA channels has a linked descriptor, a fetch error can appear on this channel.

Workaround

Do not use linked descriptors, instead make a software link.

1. Replace the channel which used the linked descriptor by a two-channel DMA (with linked descriptor disabled) handled by a two-channel event system:
   – DMA channel 0 transfer completion can send a conditional event for DMA channel 1 (through event system with configuration of BTCTRL.EVOSEL=BLOCK for channel 0 and configuration CHCTRLB.EVACT=CBLOCK for channel 1)
   – On the transfer complete reception of the DMA channel 0, immediately re-enable the channel 0
   – Then DMA channel 1 transfer completion can send a conditional event for DMA channel 0 (through event system with configuration of BTCTRL.EVOSEL=BLOCK for channel 1 and configuration CHCTRLB.EVACT=CBLOCK for channel 0)
   – On the transfer complete reception of the DMA channel 1, immediately re-enable the channel 1
   – The mechanism can be launched by sending a software event on the DMA channel 0

Affected Silicon Revisions

B	C						
X	X						

1.4.3 Linked Descriptors Reference:15683

When at least one channel using linked descriptors is already active, enabling another DMA channel (with or without linked descriptors) can result in a channel Fetch Error (FERR) or an incorrect descriptor fetch.

This happens if the channel number of the channel being enabled is lower than the channel already active.

Workaround

When enabling a DMA channel while other channels using linked descriptors are already active, the channel number of the new channel enabled must be greater than the other channel numbers.

Affected Silicon Revisions

B	C					
X	X					

1.5 96 MHz Fractional Digital Phase Locked Loop (FDPLL96M)

1.5.1 FDPLL Jitter Reference:14784

Maximum FDPLL input reference clock frequency (fGCLK_DPLL) does not meet the published specification. The maximum supported input reference clock is 1MHz.

Workaround
None.

Affected Silicon Revisions

B	C					
X						

1.5.2 DPLLRATIO Register Reference:15753

When FDPLL ratio value in the DPLLRATIO register is changed on the fly, the STATUS.DPLLLDRTO will not be set even though the ratio is updated.

Workaround
Monitor the INTFLAG.DPLLLDRTO instead of STATUS.DPLLLDRTO to get the status for DPLLRATIO update.

Affected Silicon Revisions

B	C					
X	X					

1.6 PORT - I/O Pin Controller

1.6.1 PORT Read/Write on Non-Implemented Register Reference:15611

PORT read/write attempts on non-implemented registers, including addresses beyond the last implemented register group (PA, PB), do not generate a PAC protection error.

Workaround
None.

Affected Silicon Revisions

B	C						
X	X						

1.6.2 Pull-up and Pull-down Configurations on PA24 and PA25 Pins Reference:15581

On PA24 and PA25 pins, the pull-up and pull-down configuration is not disabled automatically when alternative pin function is enabled.

Workaround
For PA24 and PA25 pins, the GPIO pull-up and pull-down must be disabled before enabling alternative functions on them.

Affected Silicon Revisions

B	C					

X	X					

1.7 Supply Controller (SUPC)

1.7.1 Buck Converter Mode Reference: CHIP003-311 & CHIP003-314

Buck Converter mode is not supported when using Digital Phase-Locked Loop (FDPLL96M) and Digital Frequency-Locked Loop (DFLL48M). As a result, Table 46-7 and Table 47-2 “Active Current Consumption - Active Mode” data for Buck Converter mode with DFLL48M configuration is not valid and must be disregarded.

Workaround
Use the LDO Regulator mode when using FDPLL and DFLL.

Affected Silicon Revisions

B	C					
X	X					

1.7.2 Buck Converter as a Main Voltage Regulator Reference:15264

When Buck converter is set as main voltage regulator (SUPC.VREG.SEL=1), the microcontroller can freeze when leaving Standby mode.

Workaround
Enable the main voltage regulator in Standby mode (SUPC.VREG.RUNSTDBY=1) and set the standby in PL0 bit to one (SUPC.VREG.STDBYPL0=1).

Note: When SUPC.VREG.STDBYPL0=1, in Standby Sleep mode, the voltage regulator is used in PL0.

Affected Silicon Revisions

B	C					
X	X					

1.8 Analog-to-Digital Controller (ADC)

1.8.1 ADC Result in Unipolar Mode Reference:14431

The LSB of ADC result is stuck at zero in Unipolar mode for 8-bit and 10-bit resolution.

Workaround
Use 12-bit resolution and take only least 8 bits or 10 bits, if necessary.

Affected Silicon Revisions

B	C					
X	X					

1.8.2 Window Monitor Reference:14449

When window monitor is enabled and its output is 0, the ADC GCLK is kept running. Power consumption will be higher than expected in sleep modes.

Workaround

None.

Affected Silicon Revisions

B	C					
X						

1.8.3 Free-Running Mode Reference:15463

In Standby Sleep mode when the ADC is in free-running mode (CTRLC.FREERUN=1) and the RUNSTDBY bit is set to 0 (CTRLA.RUNSTDBY=0), the ADC keeps requesting its generic clock.

Workaround

Stop the free-running mode (CTRLC.FREERUN=0) before entering Standby Sleep mode.

Affected Silicon Revisions

B	C					
X	X					

1.8.4 SYNCBUSY.SWTRIG Bit Reference:16027

ADC SYNCBUSY.SWTRIG get stuck to one after wake-up from Standby Sleep mode.

Workaround

Ignore ADC SYNCBUSY.SWTRIG status when waking up from Standby Sleep mode. ADC result can be read after INTFLAG.RESRDY is set. To start the next conversion, write a ‘1’ to SWTRIG.START.

Affected Silicon Revisions

B	C					
X	X					

1.9 Timer/Counter (TC)

1.9.1 SYNCBUSY Flag Reference:15056, TMR100-12

When clearing the STATUS.PERBUFV/STATUS.CCBUFVx flags, the SYNCBUSY.PER/SYNCBUSY.CCx flags are released before the PERBUF/CCBUFx registers are restored to their expected value.

Workaround

Successively clear the STATUS.PERBUFV/STATUS.CCBUFVx flags twice to ensure that the PERBUF/CCBUFx registers value is properly restored before updating it.

.

Affected Silicon Revisions

B	C					
X	X					

1.10 Timer/Counter for Control Applications (TCC)

1.10.1 Advance Capture Mode Reference:14817

Advance Capture mode (CAPTMIN CAPTMAX LOCMIN LOCMAX DERIV0) doesn't work if an upper channel is not in one of these modes, for example, when CC[0]=CAPTMIN, CC[1]=CAPTMAX, CC[2]=CAPTEN, and CC[3]=CAPTEN, CAPTMIN and CAPTMAX won't work.

Workaround

Basic Capture mode must be set in lower channel and advance Capture mode in upper channel.

Example: CC[0]=CAPTEN , CC[1]=CAPTEN , CC[2]=CAPTMIN, CC[3]=CAPTMAX

All capture will be done as expected.

Affected Silicon Revisions

B	C					
X	X					

1.10.2 SYNCBUSY Flag Reference:15057, TMR101-50

When clearing the STATUS.xxBUFV flag, SYNCBUSY is released before the register is restored to its appropriate value.

Workaround

To ensure that the register value is properly restored before updating this same register through xx or xxBUF with a new value, the STATUS.xxBUFV flag must be cleared twice.

Affected Silicon Revisions

B	C					
X	X					

1.10.3 MAX Capture Mode Reference:15059

In Capture mode while using max Capture mode, with the timer set in Up-Counting mode, if an input event occurred within two cycles before TOP, the value captured is zero instead of TOP.

Workaround

Two possible options are as follows:

1. If event is controllable, the capture event should not occur when counter is within 2 cycles before TOP value.
2. Use timer in down Counter mode and capture MIN value instead of MAX.

Affected Silicon Revisions

B	C					
X	X					

1.10.4 Dithering Mode Reference:15625

Using TCC in Dithering mode with external retrigger events can lead to unexpected stretch of right aligned pulses, or shrink of left aligned pulses.

Workaround

Do not use retrigger events or actions when TCC is configured in Dithering mode.

Affected Silicon Revisions

B	C					
X	X					

1.11 Serial Communication Interface (SERCOM)

1.11.1 USART in Auto-Baud Mode Reference:13852

In USART Auto-Baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.

Workaround

None

Affected Silicon Revisions

B	C					
X	X					

1.11.2 SDA and SCL Fall Time Reference:16225

When configured in HS or FastMode+, SDA and SCL fall times are shorter than I^2C specification requirement and can lead to reflection.

Workaround

When reflection is observed a 100 ohms serial resistor can be added on the impacted line.

Affected Silicon Revisions

B	C					
X	X					

1.12 Digital-to-Analog Converter (DAC)

1.12.1 STATUS.READY Bit Reference:14664

If CLK_APB_DAC is slower than GCLK_DAC, the STATUS.READY bit may never be set.

Workaround

Wait for INTFLAG.EMPTY to be one after enabling the DAC instead of waiting for STATUS.READY.

Affected Silicon Revisions

B	C					
X						

1.12.2 STATUS.READY is Not Cleared Reference:14678

If the DAC is enabled, STATUS.READY is not cleared during standby and will remain one after waking up, even though the DAC needs to reinitialize.

Workaround

Wait for INTFLAG.EMPTY to be one after enabling the DAC instead of waiting for STATUS.READY.

Affected Silicon Revisions

B	C					
X						

1.12.3 SYNCBUSY.ENABLE Bit Reference:14885

The SYNCBUSY.ENABLE bit is stuck at 1 after disabling and enabling the DAC when refresh is used.

Workaround

After the DAC is disabled in Refresh mode, wait for at least 30 us before re-enabling the DAC.

Affected Silicon Revisions

B	C						
X	X						

1.12.4 SYNCBUSY.DATA1 and SYNCBUSY.DATABUF1 Reference:14910

For specific DAC configurations, the SYNCBUSY.DATA1 and SYNCBUSY.DATABUF1 may be stuck at 1.

Workaround

Do not use the Refresh mode and Events simultaneously for DAC1. If event is used, write data to DATABUF1 with no refresh. DAC0 is not limited by this restriction.

Affected Silicon Revisions

B	C					

X	X					

1.12.5 VOUT Value Reference: 14917

The desired VOUT value may not be reached at the first DAC conversion after the device power-up or after wake-up from standby.

Workaround
Perform a second DAC conversion after power-up or wake-up from standby.

Table 1-1. Affected Silicon Revisions

B	C					
X	X					

1.12.6 DMA as Input to the DAC Reference:15210

When using the DMA as an input to the DAC, the previous target DAC VOUT value may not be reached when the DMA trigger 'DAC Empty' triggers a new DMA write to the DAC to start a new DAC conversion.

Workaround
Do not use the 'DAC Empty' DMA triggers to initiate a new DAC conversion from the DMA.

Affected Silicon Revisions

B	C					
X	X					

1.13 ADC

1.13.1 Effective Number of Bits Reference:13850

The ADC Effective number of Bits (ENOB) is 9.2 in this revision.

Workaround
None.

Affected Silicon Revisions

B	C					
X						

1.13.2 Power Consumption Reference:14349

Over consumption for up to 1.6 seconds on VDDANA when the ADC is disabled either manually or automatically.

Workaround
None.

Affected Silicon Revisions

B	C					
X						

1.14 External Interrupt Controller (EIC)

1.14.1 EIC_ASYNCH Register Reference:14417

Access to the EIC_ASYNCH register in 8-bit or 16-bit mode is not functional.

Workaround

- Writing in 8-bit mode will also write this byte in all bytes of the 32-bit word
- Writing higher 16-bits will also write the lower 16-bits
- Writing lower 16-bits will also write the higher 16-bits

The following two workarounds are available:

- Use 32-bit Write mode
- Write only lower 16-bits (This will write upper 16-bits also, but does not impact the application).

Table 1-2. Affected Silicon Revisions

B	C					
X	X					

1.14.2 Low Level or Rising Edge or Both Edges Reference:15278

When the EIC is configured to generate an interrupt on a low level or rising edge or both edges (CONFIGn.SENSEx) with the filter enabled (CONFIGn.FILTENx), a spurious flag might appear for the dedicated pin on the INTFLAG.EXTINT[x] register immediately the EIC is enabled using the CTRLA ENABLE bit.

Workaround

Clear the INTFLAG bit once the EIC is enabled and before enabling the interrupts.

Affected Silicon Revisions

B	C					
X	X					

1.14.3 NMI Configuration Reference:15279

Changing the NMI configuration (CONFIGn.SENSEx) on the fly may lead to a false NMI interrupt.

Workaround

Clear the NMIFLAG bit once the NMI has been modified.

Affected Silicon Revisions

B	C					

X	X					

1.14.4 Asynchronous Edge Detection Reference:16103

When the asynchronous edge detection is enabled, and the system is in Standby mode, only the first edge will generate an event. The following edges will not generate events until the system wakes up.

Workaround

Asynchronous edge detection does not work, instead use the synchronous edge detection (ASYNCH.ASYNCH[x]=0). To reduce power consumption when using synchronous edge detection, either set the GCLK_EIC frequency as low as possible or select the ULP32K clock (EIC CTRLA.CKSEL=1).

Affected Silicon Revisions

B	C					
X	X					

1.15 True Random Number Generator (TRNG)

1.15.1 Power Consumption in Standby Mode Reference:14827, MATH100-7

When TRNG is disabled, some internal logic could continue to operate causing an over consumption.

Workaround

Disable the TRNG module twice:

- TRNG -> CTRLA.reg = 0;
- TRNG -> CTRLA.reg = 0;

Affected Silicon Revisions

B	C					
X	X					

1.16 Event System (EVSYS)

1.16.1 Synchronous Path Reference:14532

Using synchronous, spurious overrun can appear with generic clock for the channel always on.

Workaround

- Request the generic clock on demand by setting the CHANNEL.ONDEMAND bit to one
- No penalty is introduced

Affected Silicon Revisions

B	C					
X	X					

1.16.2 Overrun Flag Reference:14835

The acknowledge between an event user and the EVSYS clears the CHSTATUS.CHBUSYn bit before this information is fully propagated in the EVSYS one GCLK_EVSYS_CHANNEL_n clock cycle later. As a consequence, any generator event occurring on that channel before that extra GCLK_EVSYS_CHANNEL_n clock cycle will trigger the overrun flag.

Workaround

For applications using event generators other than the software event, monitor the OVR flag.

For applications using the software event generator, wait one GCLK_EVSYS_CHANNEL_n clock cycle after the CHSTATUS.CHBUSYn bit is cleared before issuing a software event.

Affected Silicon Revisions

B	C					
X	X					

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001477A).

Note: Corrections in tables, registers, and text are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

No clarifications to report at this time.

3. Appendix A: Revision History

Rev B Document (05/2019)

The following Errata is updated:

- SUPC: 1.7.1 Buck Converter Mode Reference: CHIP003-311 & CHIP003-314
- 1.9 Timer/Counter (TC)
- 1.15.1 Power Consumption in Standby Mode Reference:14827, MATH100-7

Rev A Document (8/2018)

- This is the initial released version of this document, which lists the silicon errata issues documented in SAM L21 product data sheet (DS60001477A), hence this document supersedes the Chapter 51 of this data sheet.
- Added silicon errata FDPLL Jitter. Reference: 14784
- Added silicon errata Buck Converter Mode. Reference: CHIP003-311 & CHIP003-314
- Added silicon errata MAX Capture Mode. Reference: 15059
- Added silicon errata VOUT Value. Reference: 14917

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To register, access the Microchip web site at http://www.microchip.com/. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.

- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip’s code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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Quality Management System Certified by DNV

ISO/TS 16949

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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