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2.7Gbps Transponder Applications using the MAX3892, MAX3882, and MAX3670 Chipset

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1 Introduction

The MAX3892 and MAX3882 work together to form a fully integrated OC-48 multiplexer/de-multiplexer for applications in SONET optical transport networks (OTN), at OC-48 or OC-48 with forward error correction (FEC) rates. The MAX3670 is a high performance reference clock generator for frequency conversion and noise rejection. The MAX3892, MAX3882 and MAX3670 chipset, in conjunction with the MAX3273 laser driver and MAX3864 transimpedance amplifier (TIA), provides a complete solution for SONET/SDH and WDM transponder cards, and guarantees compliance with the ANSI, Bellcore, and ITU-T specifications at OC-48 rate.

2 OC-48 Transponder

For SONET transponder applications, both local and line timing are required to support synchronization in the transmit direction. Local timing is a mode where the reference clock for the transmitter path is derived from a local crystal oscillator. In the line timing mode, the reference for the transmitter path is derived from a clock recovered from the incoming optical signal.

In both local and line timing operations, the transmitter output must meet the SONET jitter specifications given in GR-253-CORE. Therefore a narrow band noise filter is needed to clean up the jitter on the clock from the recovered optical signal before it is applied to the transmitter as a reference. The MAX3670 in combination with an external VCO is designed for this purpose.

Figure 1 shows the block diagram of a typical OC-48 optical transponder, using the Maxim chipset to provide a low cost, highly-integrated solution for short-, intermediate- and long-reach applications.

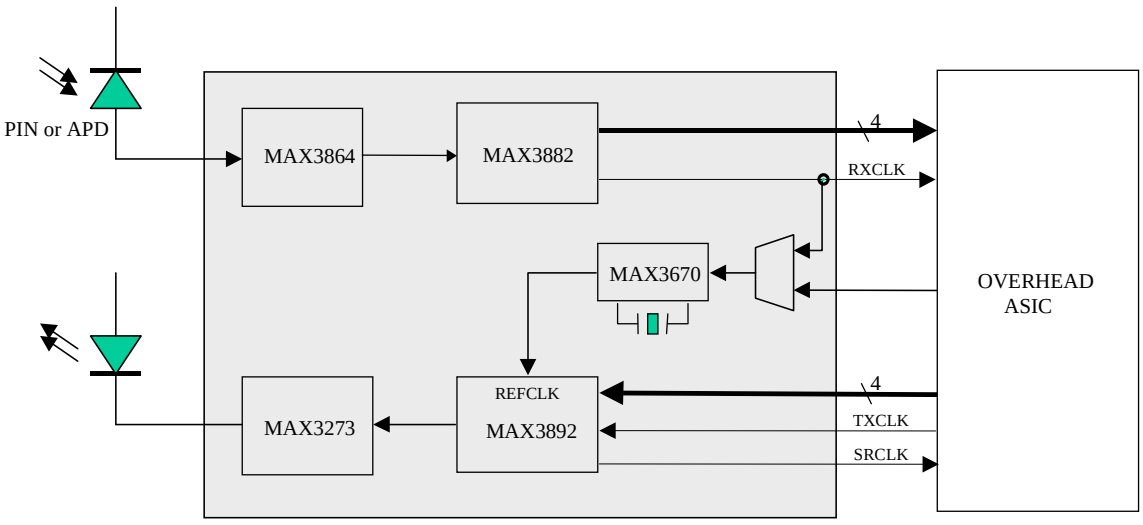

Figure 1. Application block diagram for OC-48 transponder

3 Receiver Operation

The optical receiver converts an optical signal into an electrical signal using a PIN or an APD photo diode. A transimpedance amplifier (TIA), such as the MAX3864, converts the photo current into voltage output. The MAX3882 incorporates a high-gain post amplifier that allows a direct interface with the TIA. A fully-integrated phase lock loop extracts the clock from the 2.488Gbps/2.67Gbps NRZ data input. The amplified signal is then re-timed by the recovered clock and bit de-interleaved into 4-bit parallel output with LVDS interface. The input sensitivity of the MAX3882 is 10mVp-p differential, at which the total high-frequency jitter tolerance is 0.7UI. With no jitter applied to the MAX3882 data input, the input differential swing can drop to $3mV_{p-p}$ and still achieve a $BER \leq 10^{-10}$. The MAX3882 exceeds SONET specifications for jitter tolerance, jitter generation and jitter transfer, providing system designers with sufficient margin to meet the SONET/Bellcore jitter requirement.

The MAX3882 is also designed for long haul transmission systems using optical amplification. It provides a large vertical threshold adjustment (+/-180mV) to compensate for the asymmetrical noise caused by optical amplifiers, thus optimizing the system BER performance. For this type of application, the MAX3882 can be used in conjunction with the MAX3861 AGC amplifier.

To reduce board space and simplify the design, the MAX3882 eliminates the need for an external reference clock. For applications where clock holdover is required, a reference clock of variable frequency can be applied to the MAX3882. Under loss-of-signal or loss-of-lock conditions, the MAX3882 PLL will lock to the reference clock input, providing an accurate clock output to drive the upstream device.

4 Transmitter Operation

The MAX3892 is a low-power 4:1 multiplexer with clock synthesizer. It receives 4-bit parallel LVDS data from the overhead ASIC, and generates 2.488Gbps or 2.67Gbps serial data output to drive a laser driver such as the MAX3273. An on-chip clock synthesizer PLL (CMU) generates 2.488GHz or 2.67GHz clock from the external reference clock, with optional frequencies of 38.88MHz, 77.76MHz, 155.52MHz, 622.08MHz, or the corresponding FEC rate. With Maxim's extremely low-noise VCO design, the MAX3892 achieves a typical jitter generation of $2.5mUI_{rms}$. The clock synthesizer PLL 3dB bandwidth is set at 150kHz, which eliminates the reference clock noise whose frequency components are above 150kHz. The combination of low jitter generation and narrow CMU PLL bandwidth provides greater tolerance to noise on the reference clock, allowing the customer to use some low-cost reference clock sources and still meet the SONET/Bellcore jitter specification.

5 MAX3670 Jitter Clean up PLL

For SONET optical transmission systems, the transmitter output must meet the jitter generation requirements to achieve high quality optical transmission. When the reference clock is noisy, a jitter clean up PLL is needed to attenuate the jitter on a reference clock in order to meet the jitter generation specification at the transmit output.

The MAX3670 is a high-performance reference clock generator used for jitter clean up, frequency conversion and frequency synchronization. The MAX3670 integrates a phase/frequency detector, operational amplifier, prescaler dividers, and input/output buffers. It is designed to accommodate a variety of VCOs with gain transfer ranging from 50ppm/V to 400ppm/V. Using an external VCXO or VCSO, the MAX3670 can be easily configured as a complete PLL for jitter filtering, with 3dB bandwidth programmable from 15Hz to 25kHz. Once the PLL bandwidth is set, the clock output jitter with frequency below the PLL bandwidth is dominated by the reference clock input; and jitter frequency above the PLL bandwidth is dominated by the external VCXO or VCSO.

For additional application information on the MAX3670 refer to HFDN-13.0, Loop-Filter Configuration for the MAX3670 Low-Jitter PLL Reference Clock Generator.

6 Jitter Measurement with Line Timing

Figure 2 shows the measurement setup composed of the MAX3882, MAX3892 and MAX3670. In this setup, the MAX3882 extracts a clock from the serial NRZ data input. The divided-down clock output from MAX3882 is then applied to the MAX3892 reference clock input through a jitter clean-up filter consisting of the MAX3670 and an external VCO.

To demonstrate the jitter performance of the complete transceiver chipset, the jitter at the MAX3892 clock output is measured when a 2.488Gbps (PRBS 2^23 –1) data stream is applied to the MAX3882 serial input, with additional sinusoidal phase modulation at 100Hz, 6kHz, 100kHz, and 1MHz. The jitter filter PLL bandwidth is set around 6kHz. The results are measured using VCOs from Vectron and NDK, at both 155.52MHz and 622.08MHz. Because these VCOs have different gain transfers, the MAX3670 loop filter components were changed for each VCO to maintain 6kHz bandwidth. The values for the loop filter components are shown in Table 1.

The MAX3892 clock output jitter was measured by applying a SONET filter with a bandwidth from 12kHz to 20MHz. The results are presented in Table 2. These results demonstrate that the combination of the MAX3882, MAX3670 and MAX3892 meet SONET jitter specifications, with margin.

7 Conclusion

Together, the MAX3882 and MAX3892 comprise a high performance transceiver chipset for SONET transponder applications at OC-48 rate or OC-48 with FEC. The MAX3670 is a generic low noise clock generator that can be used in OC-48, OC-192 optical transponder modules, Ethernet transponder modules, and backplane interconnects, for reference clock noise rejection, or for frequency conversion. To get the latest information on these devices, please visit the Maxim web site http://www.maxim-ic.com or contact your local Maxim representative.

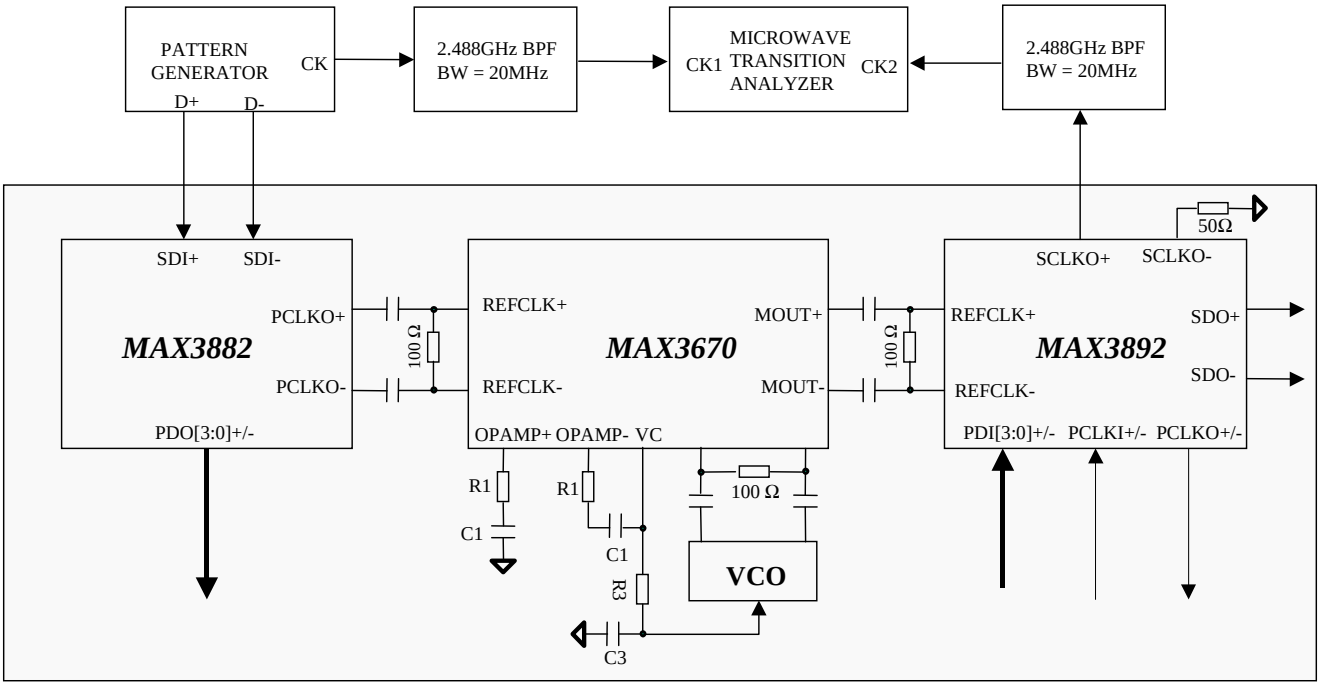

Figure 2. Measurement setup of the MAX3882, MAX3670 and MAX3892 with line timing

Table 1. Loop Filter Components and Control Settings

Type of VCO	R1 (kΩ)	C1 (nF)	R3 (Ω)	C3 (nF)	RSEL	VSEL	GSEL1	GSEL2	GSEL3
VS500A VCSO (155.52MHz)	120	12	330	12	GND	OPEN	OPEN	VCC	VCC
VS500A VCSO (622.08MHz)	91	18	330	12	GND	GND	VCC	VCC	VCC
NDK 7311L VCXO (155.52MHz)	820	18	330	12	GND	OPEN	OPEN	VCC	VCC
NDK 7311E VCXO (622.08MHz)	820	18	330	12	GND	GND	OPEN	VCC	VCC

Table 2. Jitter Measurement Results with SONET Line Timing, using Different VCOs

Input Sinusoidal Jitter		MAX3892 Clock Output Jitter (mUI_{rms})			
Frequency (Hz)	Amplitude (UI_{p-p})	Vectron VCSO VS500Afo=622.08MHz	Vectron VCSO VS500A fo=155.52MHz	NDK VCXO 7311E fo=622.08MHz	NDK VCXO 7311L fo=155.52MHz
0	0	2.6	2.5	2.62	2.51
100	16	5.54	5.45	5.6	5.28
6k	10	4.55	4.82	5.4	6.07
100k	4	3.73	2.68	4.9	2.54
1M	1	3.35	3.45	4.2	2.69