

SN74LS19A, SN74LS24A SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

JANUARY 1981 — REVISED MARCH 1988

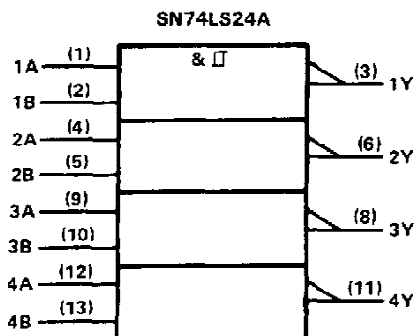
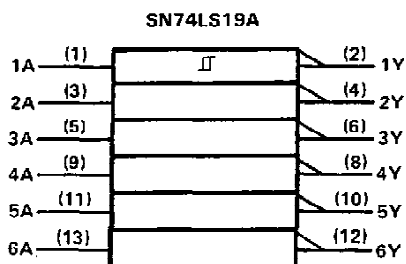
- Functionally and Mechanically Identical to 'LS13, 'LS14, and 'LS132, Respectively
- Improved Line-Receiving Characteristics
- P-N-P Inputs Reduce System Loading
- Excellent Noise Immunity with Typical Hysteresis of 0.8 V

description

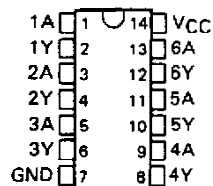
Each circuit functions as a NAND gate or inverter, but because of the Schmitt action, it has different input threshold levels for positive-going (V_{T+}) and for negative-going (V_{T-}) signals. The hysteresis or backlash, which is the difference between the two threshold levels ($V_{T+} - V_{T-}$), is typically 800 millivolts.

These circuits are temperature-compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

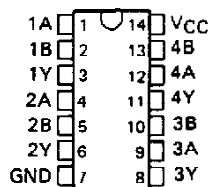
logic symbols †



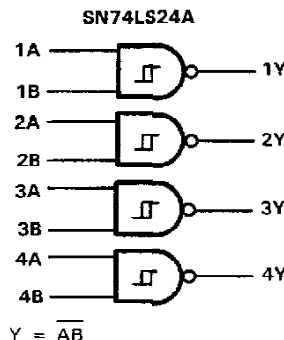
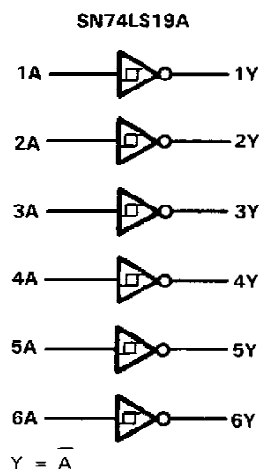
SN74LS19A . . . D, J, OR N PACKAGE
(TOP VIEW)



SN74LS24A . . . D, J, OR N PACKAGE
(TOP VIEW)



logic diagrams (positive logic)



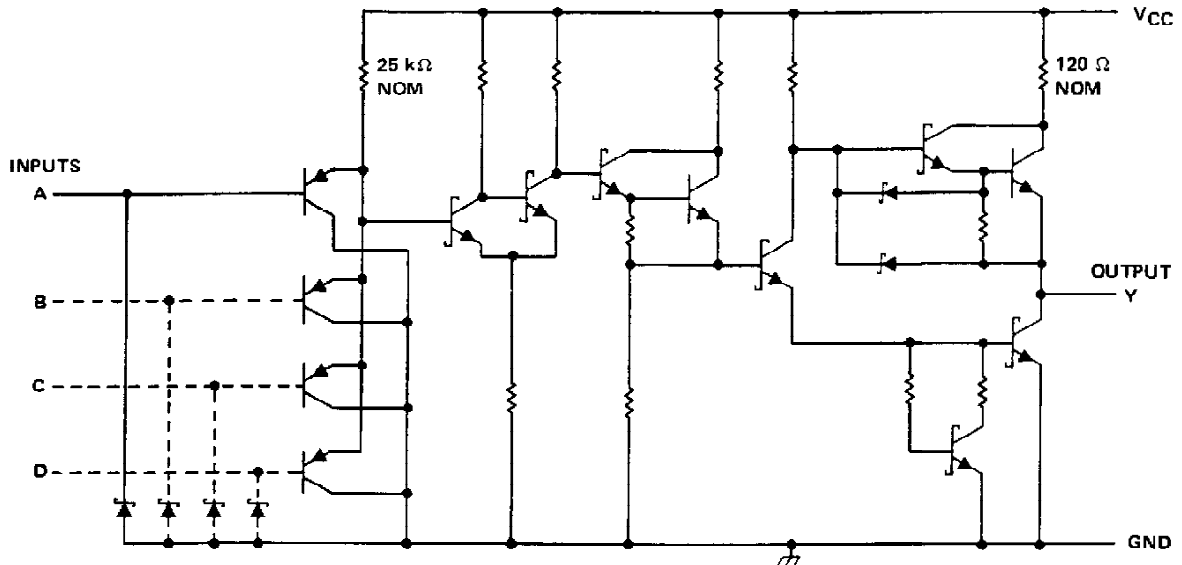
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



SN74LS19A, SN74LS24A
SCHMITT-TRIGGER POSITIVE-NAND GATES
AND INVERTERS WITH TOTEM-POLE OUTPUTS

schematic (each gate)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			-400	μ A
Low-level output current, I_{OL}			8	mA
Operating free-air temperature, T_A	0		70	°C

SN74LS19A, SN74LS24A
SCHMITT-TRIGGER POSITIVE-NAND GATES
AND INVERTERS WITH TOTEM-POLE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN TYP‡ MAX			UNIT
		MIN	TYP‡	MAX	
V_{T+}	$V_{CC} = 5\text{ V}$	1.65	1.9	2.15	V
V_{T-}	$V_{CC} = 5\text{ V}$	0.75	1.0	1.25	V
Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = 5\text{ V}$	0.4	0.9		V
V_{IK}	$V_{CC} = \text{MIN.}$ $I_I = -18\text{ mA}$		-1.5		V
V_{OH}	$V_{CC} = \text{MIN.}$ $V_I = V_{T-\text{min}}$ $I_{OH} = -0.4\text{ mA}$	2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN.}$ $V_I = V_{T+\text{max}}$	$I_{OL} = 4\text{ mA}$	0.25	0.4	V
		$I_{OL} = 8\text{ mA}$	0.35	0.5	
I_{T+}	$V_{CC} = 5\text{ V.}$ $V_I = V_{T+}$		-2	-20	μA
I_{T-}	$V_{CC} = 5\text{ V.}$ $V_I = V_{T-}$		-5	-30	μA
I_I	$V_{CC} = \text{MAX.}$ $V_I = 7\text{ V}$		0.1		mA
I_{IH}	$V_{CC} = \text{MAX.}$ $V_I = 2.7\text{ V}$			20	μA
I_{IL}	$V_{CC} = \text{MAX.}$ $V_I = 0.4\text{ V}$			-50	μA
I_{OS}^{\S}	$V_{CC} = \text{MAX.}$ $V_I = V_O = 0\text{ V}$		-20	-100	mA
I_{CCH}	$V_{CC} = \text{MAX.}$ $V_I = 0\text{ V}$	'LS19A	9.9	18	mA
		'LS24A	6.6	12	
I_{CCL}	$V_{CC} = \text{MAX.}$ $V_I = 4.5\text{ V}$	'LS19A	17	30	mA
		'LS24A	11	20	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5\text{ V.}$ $T_A = 25^\circ\text{C.}$

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5\text{ V,}$ $T_A = 25^\circ\text{C}$ (see Figure 1)

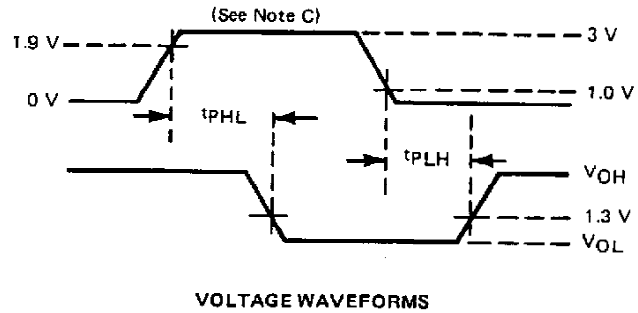
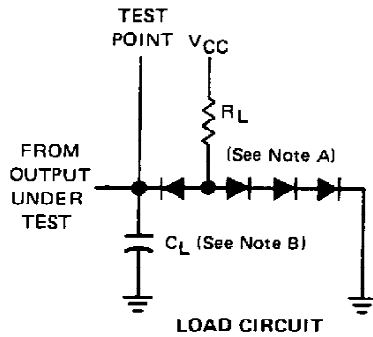
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN74LS19A			SN74LS24A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Any	Y	$R_L = 2\text{ k}\Omega,$ $C_L = 15\text{ pF}$		13	20		13	20	ns
t_{PHL}	Any	Y			18	30		25	40	ns

t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

SN74LS19A, SN74LS24A
SCHMITT-TRIGGER POSITIVE-NAND GATES
AND INVERTERS WITH TOTEM-POLE OUTPUTS

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. All diodes are IN3064 or equivalent.
 B. C_L includes probe and circuit capacitance.
 C. The generator characteristics are: PRR = 1 MHz, $t_r = 15$ ns, $t_p = 6$ ns, $Z_o = 50 \Omega$.

FIGURE 1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS19ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS19A	Samples
SN74LS19AN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS19AN	Samples
SN74LS19ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS19A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS19ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS19ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS19ADR	SOIC	D	14	2500	853.0	449.0	35.0
SN74LS19ANSR	SO	NS	14	2000	853.0	449.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LS19AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS19AN	N	PDIP	14	25	506	13.97	11230	4.32

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated