PCN Number:		20170112001						PCN Date:			Jan 16 2017			
Title: Die Coating change for Select Devices														
Customer Contact: PCN Manager Dept: Quality Services														
Proposed 1 st Ship Date			April :	16 2	2017					_	Date provided at			
			7 ф 111 .	10 2			Ava	<u>ail</u>	ilability: sample request			le request		
Change Type:						D:				7.1	\\\- 6	. D	C:L-	
Assembly Site				Design			닏	Wafer Bump Material						
✓ Assembly Process✓ Assembly Materials				H	Data Sheet			片	Wafer Bump Material Wafer Bump Process					
	hanical S		tion		H	Part number change								
	king/Ship	•				Test P			╠	╡┤	Wafer Fab Materials			
	ting, omp	pilig/ Lu	Dem	19	ш	10001						afer Fab Process		
						PCI	N	Details						
Descrip	tion of C	hange:												
This notification is to announce the change in die coat material set for the 2 groups of devices noted below as follows: Group 1 Devices														
			Current			ŧ		Proposed						
			Die Overcoat			No Die overcoat								
Group 2 Devices:														
			Current			t		Proposed						
			Ро	lyimide	Ove	ercoat		PBO overcoat						
_														
Reason	Reason for Change:													
Group 1: Die Coat not needed with Current Material Set														
Group 2: Move to standardized material set														
Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):														
None														
Anticipated impact on Material Declaration														
Material Declaration pro			proc rele	laterial Declarations or Product Content reports are driven from roduction data and will be available following the production elease. Upon production release the revised reports can be btained from the TI ECO website.										
Changes to product identification resulting from this PCN:														
None	None													

Product Affected:								
Group #1 Device List:								
TL032ACD	TL032AID	TL052ACD	TL052AID					
TL032ACDR	TL032AIDR	TL052ACDR	TL052AIDR					
Group #2 Device	List:			_				
HDC1000YPAR	HDC1008YPAR	HDC1050DMBR	HDC1050DMBT					
HDC1000YPAT	HDC1008YPAT							

Group #1 Qualification Data:

Group #1 Qualification Data:								
Reference Qualification Data: Approved September, 2012								
Qualification Vehicle: LM358DR (MSL 1-260C)								
Package / Die Construction Details								
Assembly Site:	TIN	1exico	d: 4211880					
# Pins-Designator, Family:	8-0	D, SOIC Mount Compound		1: 41478	: 4147858			
Leadframe (Finish, Base):	NiPo	dAu, Cu	Bond Wire	e: 0.96 Mil Dia., Cu				
Qualification: Plan Test Results								
Reliability Test		Conditions		Sample Size (PASS/FAIL)				
				Lot#1	Lot#2	Lot#3		
Steady-state Life Test		150C (168, 300 I	77/0	-	-			
Electrical Characterization		-	30/0	-	-			
**High Temp. Storage Ba	ke	170C (420hrs)	77/0	-	-			
**Biased HAST		130C/85%RH (96	77/0	-	-			
**Autoclave 121C		121C, 2 atm (96	77/0	-	-			
**T/C -65C/150C		-65C/+150C (50	77/0	77/0	77/0			
Visual / Mechanical		-		328/0	-	-		
Lead Pull		# of leads to destruction, min. 3 units		22/0	-	-		
Bond Strength		76 ball bonds, m	76/0	-	-			
Die Shear		-	10/0	-	-			
Manufacturability		(per mfg. Site sp	1/0	-	-			
**Thermal Shock		-65C/+150C (50	77/0	77/0	77/0			
X-ray		(top side only)	5/0	-	-			
Moisture Sensitivity		(level 1 @ 260C	12/0	12/0	12/0			
Notes **- Preconditioni	ng s	equence: Level 1-2						

Group #2 Qualification Data:



TI Information Selective Disclosure

Qualification Report

HDC1010YPA New Product Qualification Approve Date 08-Sep-2016

Product Attributes

Attributes	Qual Device: HDC1010YPA	QBS Product Reference: HDC1000	QBS Process Reference: LM3533
Wafer Fab Supplier	MFAB	MFAB	MFAB
Wafer Process	CMOS9T5V	CMOS9T5V	CMOS9T5V
Assembly Site	TIEM-MALACCA	TIEM-MALACCA	TIEM-MALACCA
Package Family	WCSP	WCSP	WCSP
Flammability Rating	UL 94 V-0	UL 94 V-0	UL 94 V-0

⁻ QBS: Qual By Similarity

Qualification Results Data Displayed as: Number of lots / Total sample size / Total failed

Туре	Test Name / Condition	Duration	Qual Device: HDC1010YPA	QBS Product Reference: HDC1000	QBS Process Reference: LM3533
PC	PreCon Level 1	Level 1-260C	3/924/0	-	-
HTOL	Life Test, 125C	1000 Hours	1/77/0	1/77/0	2/154/0
HAST	Biased HAST, 130C/85%RH	96 Hours	3/231/0	-	-
UHAST	Unbiased HAST 130C/85%RH	96 Hours	3/231/0	-	-
TC	Temperature Cycle, -40/125C	850 Cycles	3/231/0	-	-
HTSL	High Temp Storage Bake 150C	1000 Hours	3/231/0	-	-
HBM	ESD - HBM	1000 V	1/3/0	-	-
CDM	ESD - CDM	750 V	1/3/0	-	-
LU	Latch-up	(per JESD78)	1/6/0	-	-
ED	Electrical Characterization	Per Datasheet Parameters	3/Pass	-	-
MQ	Manufacturability (Assembly)	(per mfg. Site specification)	3/Pass	-	-
MQ	Manufacturability (Wafer Fab)	(per mfg. Site specification)	1/Pass	-	-

⁻ Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

Green/Pb-free Status:

Qualified Pb-Free(SMT) and Green

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

Location	E-Mail
USA	PCNAmericasContact@list.ti.com
Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
Japan	PCNJapanContact@list.ti.com

⁻ Qual Device HDC1010 is qualified at LEVEL1-260C

⁻ The following are equivalent HTOL options based on an activation energy of 0.7eV: 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240

⁻ The following are equivalent HTSL options based on an activation energy of 0.7eV: 150C/1k Hours, and 170C/420 Hours

⁻ The following are equivalent Temp Cycle options per JESD47: -55C/125C/700 Cycles and -65C/150C/500 Cycles Quality and Environmental data is available at TI's external Web site: http://www.ti.com/