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ML5805

5.8GHZ VARIABLE DATA RATE FSK TRANSCEIVER WITH INTEGRATED PA

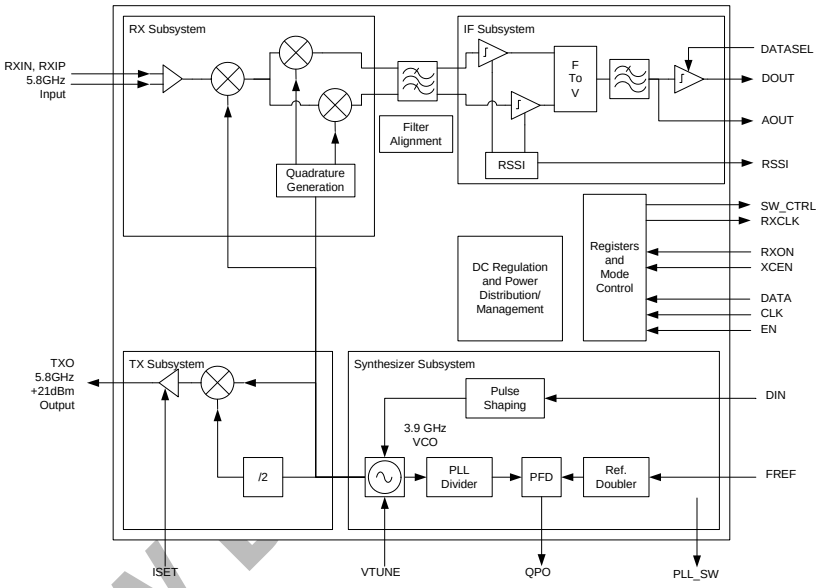
Package: 40 QFN, 6mmx6mm

Features

- Highly Integrated 5.8GHz FSK Transceiver With Selectable Data Rates; 576kbps, 1.125Mbps, 1.536Mbps, 1.75Mbps, 2.048Mbps
- Low-IF Receiver Eliminates External IF Filters
- Fractional-N Synthesizer with 30Hz Resolution
- Fully Integrated Digital FIR Tx Data Filter, IF Filters, FM Discriminator, and Rx Data Filter
- Self-calibrating VCO and Filters Eliminate Tuning
- Operating Modes Include DSSS-DCT, DECT, and High Rate (2.048Mbps) for Wireless Audio and Video
- -97dBm Sensitivity (0.1% BER) With Integrated LNA
- +21dBm Typical Output Power From Integrated PA
- Includes FastWave™ Embedded Wireless Microcontroller Technology
- Simple 3-Wire Control Interface
- TR PIN Diode or FET Switch Driver Outputs
- Analog RSSI Output: 35mV/dB
- Selectable Rx Clock Recovery Output

Applications

- Digital Cordless Telephones DSSS and DECT
- Wireless Streaming Audio and Video
- Wireless Data Links



Functional Block Diagram

Product Description

The ML5805 is a single chip fully integrated Frequency Shift Keyed (FSK) transceiver developed for a variety of applications operating in the 5.725GHz to 5.850GHz unlicensed ISM band. The ML5805 is mode selectable for operation with digital cordless phones (DSSS or DECT) and higher data rate streaming applications like wireless audio and video.

The ML5805 contains a dual-conversion, low-IF receiver with all channel selectivity on chip. IF filtering, IF gain, and demodulation are performed on-chip, eliminating the need for any external IF filters or production tuning. A post detection filter and a data slicer are integrated to complete the receiver.

The ML5805 transmitter uses an adjustment-free closed loop modulator, which modulates the on-chip VCO filtered data. The ML5805 includes an upconversion mixer, a buffer/predriver, and a power amplifier to produce a typical output power of +21dBm. A fully integrated fractional synthesizer is used in both receive and transmit modes. Power supply regulation is included in the ML5805, providing circuit isolation and consistent performance over supply voltages between 2.8V and 3.6V.

Optimum Technology Matching® Applied

☐ GaAs HBT	☑ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ RF MEMS
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
VCC	VSS-0.3 to 3.6	V
VCC_PA	VSS-0.3 to 4.5	V
Junction Temperature	150	°C
Storage Temperature	-65 to +150	°C
Lead Temperature (Soldering, 10s)	260	°C
Ambient Temperature Range (T_A)	-10 to 60	°C
VCC Range [VDD (pin 9,) VCCSYN (pin 13), VCCPLL (pin 19), VCCA (pin 27)]	2.8 to 3.6	V
VCC_PA Range [VCC_PA (pin 31)]	3.0 to 4.5	V
Thermal Resistance (θ_{JA})	36	°C/W

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power Supplies					Unless otherwise specified T_A=25°C and the supply voltage is V_{CC}=3.3V, V_{CC_PA}=3.6V, R_{ISET}=381Ω, F_{REF}=12.288MHz, DATA RATE=1.536Mbps, all measurements are normalized to the IC pins.
Supply current, STANDBY mode (I_{STBY})		2		µA	DC supply connected, XCEN low, RXON high.
Supply current, RECEIVE mode (I_{RX})		69		mA	RX chain active, data being received.
Transmit supply current at VCC pins (I_{TX})		77		mA	
VCC_PA pin		100		mA	P_{OUT}=+21dBm
		78		mA	P_{OUT}=+18dBm (contact factory for configuration settings for this power setting)
Synthesizer					
Charge Pump Sink/Source Current		±0.2		mA	
VCO Input Voltage	0.3		2.5	V	
Lock time for any in band frequency change		110		µsec	From EN asserted to RX valid data (RX) or PAON high (TX)
		55		µsec	NOIVCOC=1 (no incremental VCO cal)
Phase Noise		-85		dBc/Hz	at 100kHz
		-116		dBc/Hz	at 1MHz
		-122		dBc/Hz	at 2MHz
		-134		dBc/Hz	at 10MHz
Reference Signal Frequency		12.288		MHz	Data Rate=1.5360, 1.7554, and 2.0480Mbps
		13.824		MHz	Data Range=576, 1, 152Kbps
Reference Signal Input Level	0.5			V_{P-P}	Clipped sine, AC coupled

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Receiver					
Receive input frequency range	5.725		5.850	GHz	
Input Impedance Differential		100		Ω	
Channel Spacing		1.728		MHz	Data Range=1.1520Mbps
		2.048		MHz	Data Range=1.5360Mbps
		4.096		MHz	Data Range=1.7554Mbps
		4.096		MHz	Data Range=2.0480Mbps
Input Sensitivity		-97		dBm	<0.1% BER at 1.1520 Mbps
		-97		dBm	<0.1% BER at 1.5360 Mbps
		-97		dBm	<0.1% BER at 1.7554 Mbps
		-96		dBm	<0.1% BER at 2.0480 Mbps
RF Input Power			+10	dBm	<0.1% BER at 1.1520Mbps, 1.5360Mbps, 1.7554Mbps, and 2.0480Mbps
Data Slicer Time Constant		6		uS	DATASEL=V_{IH}
		300		uS	DATASEL=V_{IL}
RX conducted emissions at RXI			-50	dBm	RXI terminated in 50Ω
RX Chain Image rejection ratio		28		dB	
RX adjacent channel(s) rejection. Wanted signal=-80dBm, PN20, CW Interfering signal, 0.1% BER		15		dB	±1 channel offset
		40		dB	±2 channels offset
		45		dB	±3 or more channels offset
Co-Channel rejection, 0.1% BER		-9		dB	Wanted signal=-80dBm, Unwanted signal is GFSK modulated with 1.536Mbps PRBS data, BT=0.9
RSSI					
RSSI rise time, 20% to 80%		5	10	µsec	20pF loading on RSSI pin RF off to -15dBm
RSSI fall time, 80% to 20%		5	10	µsec	20pF loading on RSSI pin -15dBm to RF off
RSSI maximum voltage		2.7		V	-10dBm into RXI
RSSI midrange voltage		2.5		V	-40dBm into RXI
RSSI minimum voltage		0.2		V	No signal applied
RSSI sensitivity		35		mV/dB	(V_{-40dBm} - V_{-50dBm})/10dB
RSSI accuracy		±3		dB	Deviation from best fit straight line
Transmitter					
Transmit input frequency range	5.725		5.850	GHz	
TX output power at 5.8GHz		21		dBm	Matched into 50Ω
Transmit Modulation Deviation		±400		kHz	Data Range=1.1520Mbps
		±512		kHz	Data Range=1.5360Mbps
		±596		kHz	Data Range=1.7554Mbps
		±680		kHz	Data Range=2.0480Mbps
Output Impedance		TBD		Ω	At TXO pin
Transmit Filter Bandwidth/Symbol Rate Ratio		0.5			Data Range=1.1520Mbps
		0.9			Data Range=1.5360Mbps
		0.8			Data Range=1.7554Mbps
		0.7			Data Range=2.0480Mbps

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Transmitter, cont.					
PLL reference spurious		-70		dBc	V_{FREF} < 2Vp-p clip-sine
TX LO feed through, LO harmonics and sub-harmonics		-40		dBc	P_{TXO} = +21dBm, FSPUR = 1/3, 2/3, 4/3, and 5/3 $F_{TXO.}$ TX frequency = F_{TXO}, TX power = P_{TXO}
TX Harmonics, PTXO = +21dBm		-45		dBc	2nd Harmonic
		-25		dBc	3rd Harmonic
Interface Logic Levels					
CMOS Digital Input Pins (XCEN, RXON, DIN, DATASEL)					
Input High Voltage	V_{DD} * 0.7		V_{DD}	V	
Input Low Voltage	0		V_{DD} * 0.3	V	
Input Bias Current	-5		+5	µA	All states
Input Capacitance		4		pF	1MHz test frequency
CMOS Digital Output Pins (SW_CTRL, RXCLK, DOUT))					
SW_CTRL output high voltage	V_{DD}-0.4			V	Sourcing 5.0mA
SW_CTRL output low voltage			0.4	V	Sinking 5.0mA
SW_CTRL source/sink current	±5.0	±8.0		mA	
RXCLK (recovered clock) output high voltage	VCC-0.4			V	Sourcing 0.1mA
RXCLK (recovered clock) output low voltage			0.4	V	Sinking 0.1mA
DOUT (data output) output high voltage	VDD-0.4			V	Sourcing 0.1mA
DOUT (data output) output low voltage			0.4	V	Sinking 0.1mA
Analog Output Pins (AOUT)					
Quiescent output voltage at AOUT		1.15		V	
Output voltage swing at AOUT		0.8		V_{P-P}	
3 Wire Serial Bus Timing					
CLK Input Rise Time (Note 1)			15	ns	
CLK Input Fall Time (Note 1)			15	ns	
CLK Period	50			ns	
EN Pulse Width	200			ns	
Delay from last Clock Rising Edge to Rise of EN	15			ns	
EN Setup Time to Ignore next Rising CLK	15			ns	
Data-to-CLK Setup Time	15			ns	
Data-to-CLK Hold Time	15			ns	

Note 1: Serial I/O clock maximum rise and fall times are based on the minimum clock period. Longer rise and fall times can be accommodated for slower clocks provided the rise and fall times remain less than 20% of the clock period and all set up and hold time minimums are met with respect to the CMOS switching points (V_{IL} MAX and V_{IH} MIN). The serial I/O clock rise and fall times are limited to an absolute maximum of 100ns.

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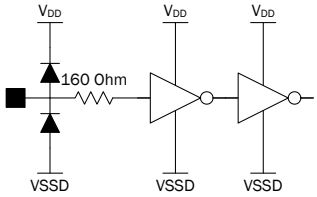
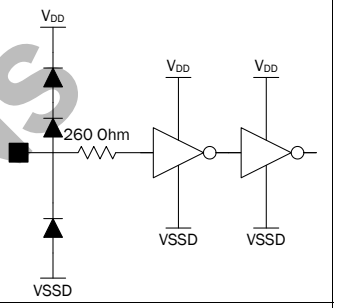
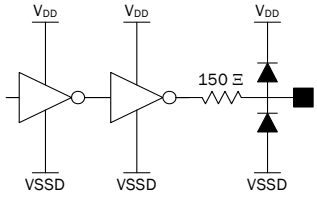
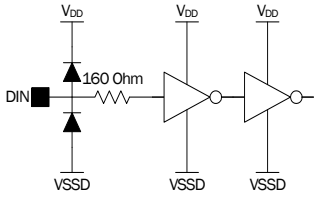
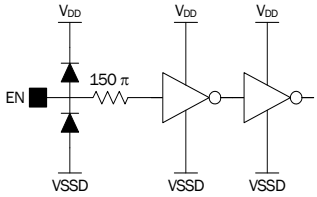
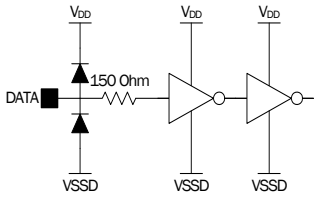
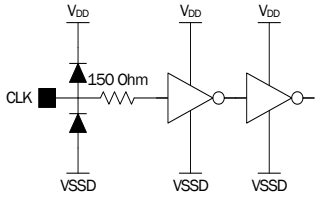
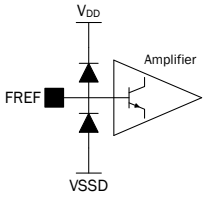
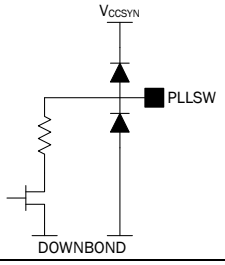
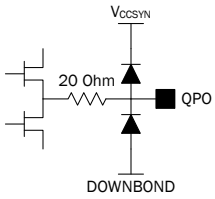
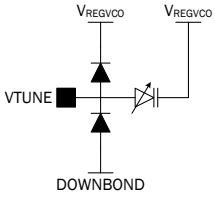
Pin	Function	Description	Interface Schematic
1	XCEN	Transceiver Enable input. Enables the bandgap reference and voltage regulators when high, enabling normal control functions. Consumes only leakage current in STANDBY mode when low. Operating mode=V_{IH} Standby mode=V_{IL}	
2	RXON	TX/RX Control Input. Switches the transceiver between TRANSMIT and RECIEVE mode. Receive mode=V_{IH} Transmit mode=V_{IL}	
3	SW_CTRL_P	TR switch control output, positive polarity. Logic high (V_{OH}) while transmitting Logic low (V_{OL}) while receiving	
4	DIN	Transmit Data Input.	
5	VSSD	Digital ground for all digital I/O circuits and control logic.	
6	EN	Control Bus Enable. Enable pin for the three-wire serial control bus. The control registers are loaded on the rising edge of this signal. Serial control bus data is ignored when this signal is high (V_{IH}).	
7	DATA	Serial Control Bus Data.	

Pin	Function	Description	Interface Schematic
8	CLK	Serial control bus data is clocked in on the rising edge and only when EN is low.	
9	VDD	3.3V_{DC} power supply input.	
10	VREG_1P8	1.8V_{DC} regulator output. Place capacitor between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	
11	VBG_1P8	1.13V_{DC} bandgap voltage output. Place capacitor between this pin and ground to decouple (bypass) noise.	
12	FREF	Input reference frequency.	
13	VCCSYN	2.7V_{DC} power supply input. Must be connected to VREGPLL pin externally.	
14	PLL_SW	Loop filter control switch.	
15	QPO	Charge pump output of the phase detector. This is connected to the external PLL loop filter.	
16	VTUNE	VCO Tuning Voltage input from the PLL loop filter. This pin is very sensitive to noise coupling and leakage currents.	
17	VREGVCO	2.5V_{DC} regulator output. Place capacitor between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	
18	VREGPLL	2.7V_{DC} power supply output. Place capacitor between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	
19	VCCPLL	3.3V_{DC} power supply input. Place capacitor between this pin and ground to decouple (bypass) noise.	
20	VBG_VCO	1.13V_{DC} bandgap voltage output. Place capacitor between this pin and ground to decouple (bypass) noise.	

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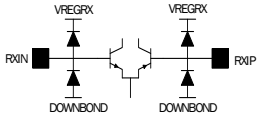
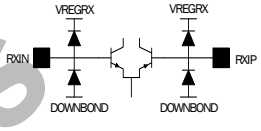
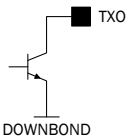
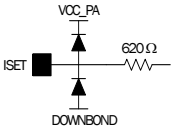
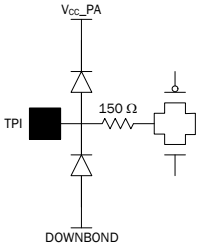
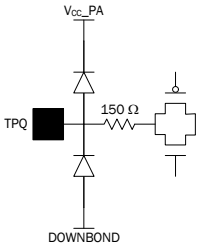
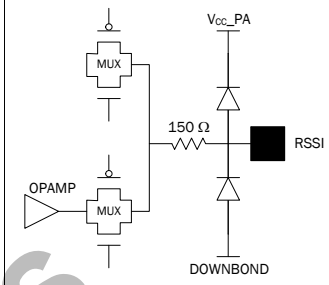
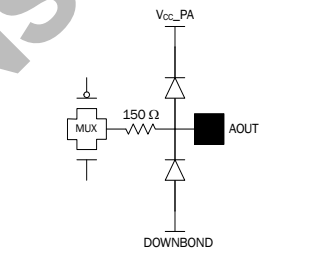
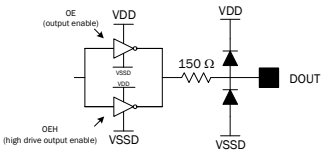
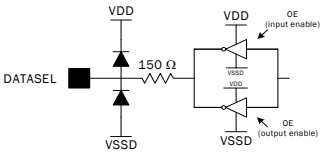
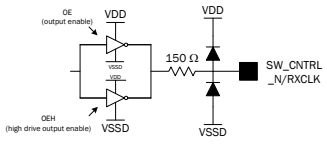
Pin	Function	Description	Interface Schematic
21	VREGLNA	2.7V_{DC} regular output. Place capacitor between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	
22	RXIN	Differential receive RF Input.	
23	RXIP	Differential receive RF Input.	
24	VREGRX	2.7V_{DC} regular output. Place capacitor between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	
25	VBG_RF	Bandgap 1.24V decouple voltage. Decoupled to ground with a capacitor.	
26	VREGTX	2.7V_{DC} power supply input. Must be connected to VREGRX pin externally.	
27	VCCA	3.3V_{DC} power supply input.	
28	TXO	TX RF open-collector output. Connect this pin to VCC using an (RF blocking) inductor.	
29	ISET	TX I_{SET} resistor.	
30	VBG_PA	1.13V_{DC} bandgap voltage output. Place capacitor between this pin and ground to decouple (bypass) noise.	
31	VCC_PA	Unregulated Battery DC Power Supply Input.	
32	VREGPA	Programmable 3.67V_{DC}*/3.44V_{DC}/3.3V_{DC} regulator output. Place capacitor between this pin and ground to decouple (bypass) noise and to stabilize the regulator. *Not recommended for use - Exceeds Absolute Maximum Ratings.	
33	VREGIF	2.7V_{DC} regular output. Place capacitor between this pin and ground to decouple (bypass) noise and to stabilize the regulator.	
34	TPI	RX/TX test port. Used to test or apply test signals to both RX and TX sections.	
35	TPQ	RX/TX test port. Used to test or apply test signals to both RX and TX sections.	

Pin	Function	Description	Interface Schematic
36	RSSI	Receive Signal Strength Indicator. Also used as RX/TX test port.	
37	AOUT	Analog data output.	
38	DOUT	Serial digital output after demodulation, bit rate filtering and center data slicing. CMOS levels with controlled slew rates.	
39	DATASEL or PLL_Lock	When TCMOD=4 or 5, this pin becomes an input and it controls the time constant of the data slicer. When TCMOD=4 or 5; DATASEL=V_{IH} selects 6uS time constant DATASEL=V_{IL} selects 300uS time constant -else- When TCMOD is not set to value 4 or 5, this pin becomes PLL Lock/Unlock output PLL_Lock=V_{DH} indicates PLL is locked PLL_Lock=V_{DL} indicated PLL is not locked	
40	SW_CNTRL_N or RXCLK	TR switch control output, negative polarity. V_{OL} while transmitting V_{OH} while transceiving -or- Recovered RXCLK clock output is multiplexed in this pin. When configured for RXCLK output, clock pulses may be observed for 6uS to 8uS after the falling edge of RXON before setting to logic high (V_{IH}).	

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Functional Description

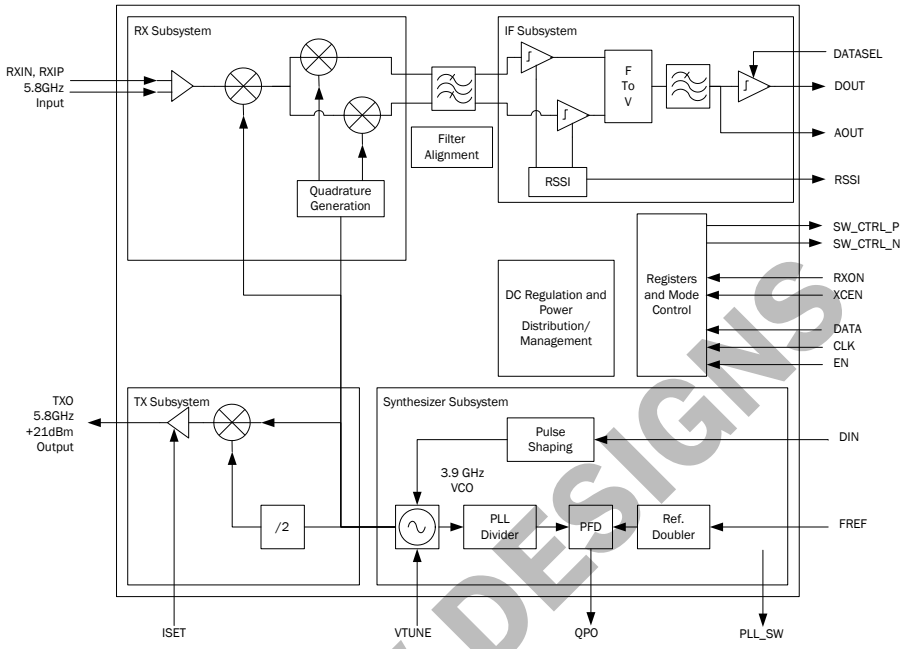

Figure 1 ML5805 Block Diagram

The ML5805 is a single chip wireless digital transceiver. The ML5805 integrates all the frequency generation, receiver and transmit functions requiring only a TR switch to form a complete 5.725GHz to 5.850GHz ISM radio band. The ML5805 is designed to transmit and receive 576kbps to 2.048Mbps signals using channels spaced from 1.728MHz to 4.096MHz.

Receiver

The ML5805 contains a dual conversion, low_IF receiver with all channel selectivity on-chip. The signal enters through a differential LNA to the 1st mixer which down-converts the 5.8GHz input t a high 1st IF of 1.9GHz, followed by an image reject 2nd mixer that brings this IF signal down to a low IF frequency. On chip IF filtering, gain, and demodulation are performed at 864kHz IF frequency for the 576kbps and 1.152Mbps data rate, a1.024MHz IF frequency for the 1.536Mbps data rate, or a 2.048MHz IF frequency for the 1.755Mbps and 2.048Mbps data rates.

No external filters or production tuning are requires. A post detection filter and data slicer are also provided to complete the receiver. The DATASEL pin allows selection between two different time constraints in the data slicer. Rx clock recovery is optionally performed for the 1.152Mbps, 1.536Mbps, 1.755Mbps, 2.048Mbps data rate to aid those applications using a simple microcontroller based MODEM. A receive signal strength indication (RSSI) signal is also provided. RSSI (an indication of field strength) can be used by the system to determine transmit power control (conserve battery life) and/or determine if a given channel is occupied.

Automatic VCO and Filter Alignment

The VCO and IF filters are calibrated to remove process and temperature variation. IF filter and VCO calibration occurs when the chip is first powered on and at specified intervals during normal operation. The calibration is transparent to the normal operation of the ML5805 and is absorbed in the system timing shown in Figure 2, Figure 3, and Table 2. The self-calibration adjusts:

- VCO center frequency
- Discriminator center frequency
- IF filter center frequency and bandwidth

- Receiver data low-pass filter bandwidth

Transmitter and PA

The ML5805 transmitter consists of an up-conversion mixer followed by a programmable gain amplifier, to allow factory calibration of the output power, and a power amplifier (PA). The input data is filtered before being sent to an adjustment free VCO modulator. An FIR Gaussian pulse shaping filter is used followed by DAC and interpolation filter for clock rejection. The output of modulator is up-converted by a mixer and amplified with a PA to deliver 21dBm output power. A complementary T/R switch control output with adjustable timing is provided to control the external T/R switch.

PLL/Synthesizer

A single, on-chip 3.9GHz fractional-N synthesizer is used to generate the receiver LO and transmit carrier. The VCO has an on-chip resonator, active devices and tuning circuitry for a completely integrated VCO function. All required DC voltage regulation is within the IC. The PLL center frequency is programmes with a 23 bit word written via the SPI port during either standby or active operation.

A lock detect circuit monitors the state of the PLL loop allowing the PA to be disables prior to the PLL achieving lock in TRANSMIT mode. In RECEIVE mode, the synthesizer produces a low side LO frequency offset (compared to TX mode) to produce the required IF frequency.

Modes of Operation

The ML5805 has three key modes of operation:

- STANDBY: All circuits powered down except the control interface (static CMOS)
- RECEIVE: Receiver circuits active
- TRANSMIT: Transmitter circuits active

Mode Control

The two operational modes controlled by RXON are RECEIVE and TRANSMIT. XCEN is the chip enable/disable control pin which sets the device to either operational or STANDBY modes. The relationship between the parallel control lines and the mode of operation of the IC is summarized in Table 1.

Table 1: Modes of Operation

XCEN	RXON	MODE NAME	FUNCTION
0	X	STANDBY	Control interfaces active, all other circuits powered down
1	1	RECEIVE	Receiver time slot
1	0	TRANSMIT	Transmit time slot

STANDBY Mode

In STANDBY mode, the ML5805 transceiver is powered down. The only active circuits are the control interfaces, which are static. CMOS to minimize power consumption. The serial control interface and control registers remain powered up and will accept and retain programming data as long as the VDD and VCCA are present.

RECEIVE Mode

In RECEIVE mode, the received signal at 5.8GH is down converted, band pass filtered (IF filtered), fed to the frequency-to-voltage converter, and then low-pass filtered. the output of the low-pass filter is available at both the AOUT pin and to the on-chip data slicer that produces NRZ digital data presented at the DOUT pin. An RSSI output voltage is also provided.

TRANSMIT Modes

In TRANSMIT mode, the PLL loop is closed to eliminate frequency drift. A closed loop FSK modulator modulates both the VCO and the fractional-N PLL. the VCO is directly modulated with filtered FSK transmit data. The PLL is driven by a sigma-delta modulator, which ensures that the PLL follows the mean frequency of the modulated VCO.

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Control Interface

There are two types of input/output (I/O) signals to control and monitor the ML5805; discrete I/O and serial input.

- Discrete I/O: XCEN, RXON, SW_CTRL_P, SW_CTRL_N, DATASEL
- Serial Control Bus: EN, DATA, CLK

The ML5805 transceiver is used in time division duplex (TDD) mode, where the transceivers at each end of a radio link alternately transmit and receive. Prior to entering receive mode, the ML5805 goes through a "self-calibration" sequence, where the VCO, IF, and data filters are frequently aligned. This occurs in the time period just before the PLL settles to the LO frequency. These calibration cycles are triggered by logic transitions on the control interface. Figure 2 and Figure 3 show the normal operating cycle for the ML5805. Figure 2 shows the timing when register variable PAFIRST is set to 0, causing the switch control signals to change state before the PA is enabled. Figure 3 shows the timing when register variable PAFIRST is set to 1, causing the switch signals to change state after the PA is enabled.

RF Control: XCEN, RXON, SW_CTRL

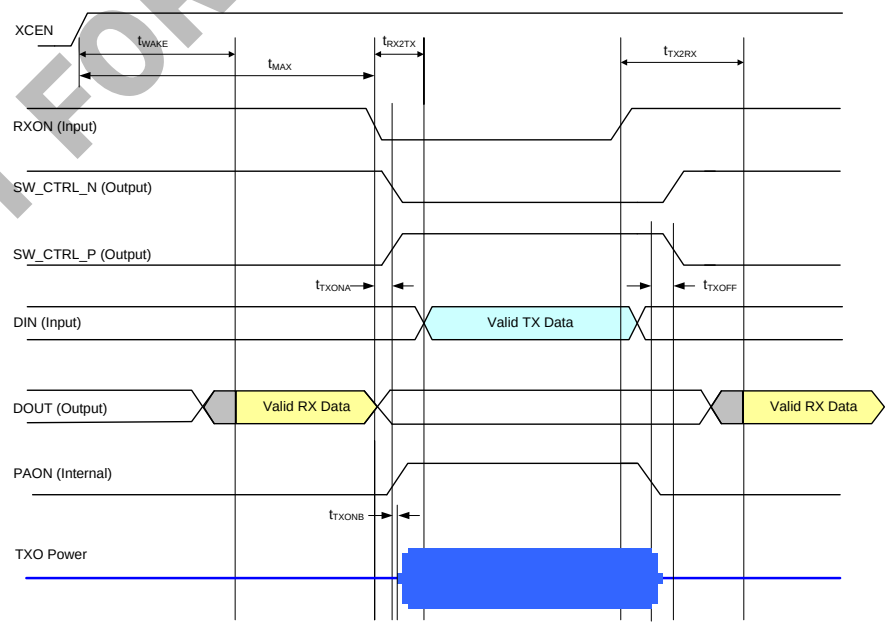
The XCEN pin enables/disables the ML5805 and places the device in either STANDBY or ACTIVE modes.

The RXON pin determines which active mode the ML5805 is in: RECEIVE or TRANSMIT.

SW_CTRL_P and SW_CTRL_N are complimentary CMOS outputs with 5mA drive capability that controls an off-chip T/R switch. They can be directly drive PIN diodes. SW_CTRL_P outputs a logic high when RXON is asserted low and a logic low at all other times. the time delays between RXON and SW_CTRL_P are programmable and are shown in Figure 2, Figure 3, and Table 3. These outputs are inhibited when the PLL is not locked.

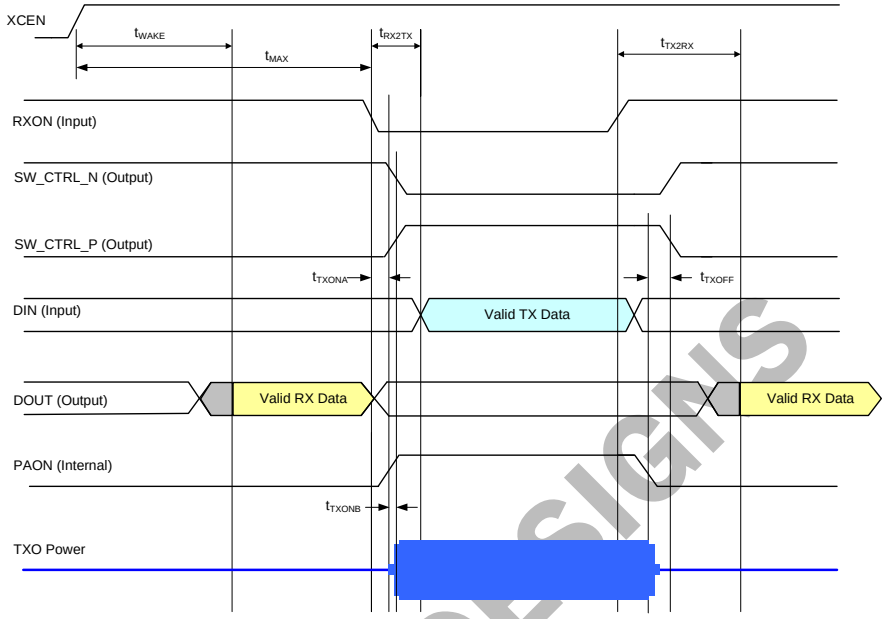
ML5805 Initialization after Power On (VCC=Low to High)

After power on, the microcontroller must first initialize the ML5805 configuration registers and PLL frequency word while CE=0. At a minimum, register # 0 and the PLL frequency register must be written. Other registers may be changed at this time, also. After registers are written, CE is asserted (high) for a period of 257usec minimum to perform a one-time internal calibration. After this time, the CE signal may be de-asserted (CE=0) to save current.



PAFIRST = 0 (The external switch controls SW_CTRL_P/N are switched before PA is turned on).

Figure 2 Control Timing for TDD Operation, PAFIRST=0



PAFIRST = 1 (PA turns on before external switch controls, SW_CTRL_P/N are switched.

Figure 3 Control Timing for TDD Operation, PAFIRST=1

Table 2 shows the minimum time required between control interface transitions.

Table 2: Transceiver Control Interface Timing (using default register values).

SYMBOL	PARAMETER	TIME	UNITS
t_{WAKE}	Time from XCEN asserted to valid RECEIVE data out	325	µsec
t_{FH}	Time from rising edge of Serial Bus EN to valid RECEIVE data out (channel scan mode, one channel hop, PLL re-locking triggered by rising EN). NOIVCOC=0	110	µsec
t_{FH}	Time from rising edge of Serial Bus EN to valid RECEIVE data out (channel scan mode, one channel hop, PLL re-locking triggered by rising EN). NOIVCOC=1	55	µsec
t_{TX2RX}	Time from rising edge of RXON to valid RECEIVE data out. NOIVCOC=0	90	µsec
t_{TX2RX}	Time from rising edge of RXON to valid RECEIVE data out. NOIVCOC=1	80	µsec
t_{RX2TX}	Time from falling edge on RXON to start of valid data on DIN pin. Some RF energy will be present on TXO during this period but PAON will be unasserted.	70	µsec
t_{TXONA}	For the case where PAFIRST=0: t_{TXONA} defines the time between falling edge of RXON and rising edge of RF output power. For the case where PAFIRST=1: t_{TXONA} defines the time between rising edge of RF output power and rising edge of SW_CTRL_P. $t_{TXONA}=44\mu S+TTXONA*8/f_{ref}$ where TTXONA is an interger with a range from 0 to 63	44 to 85	µsec
t_{TXONB}	For the case where PAFIRST=0: t_{TXONB} defines the time between rising edge of SW-CTRL_P and rising edge of RF output power. For the case where PAFIRST=1: t_{TXONB} defines the time between rising edge of RF output power and rising edge of SW_CTRL_P. $t_{TXONB}=3.5\mu S+TTXOFF*8/f_{ref}$ where TTXOFF is an interger with range from 0 to 31	4.2 to 24.2	µsec
t_{TXOFF}	Time between falling edge of RF output power and falling edge of SW_CTRL_P signal. $t_{TXOFF}=3.5\mu S+TTXOFF*40/f_{ref}$ where TTXOFF is an interger with range from 0 to 3	3.5 to 13.5	µsec

Channel Scan Timing in Receive Mode

To implement channel scanning the ML5805 is kept in RECEIVE mode (XCEN and RXON high) and the PLL is reprogrammed to select a different RF channel. A VCO and filter calibration cycle is initiated periodically after the serial bus writes to the register

controlling the PLL. Any serial bus writes to the other registers (while XCEN=V_{IL}(0)) will trigger a complete calibration cycle. Non-PLL register writes (R0 to R4) are only performed when XCEN=V_{IL}(0). Otherwise unstable operation will occur.

Signal diagram for channel scanning is shown in Figure 4.

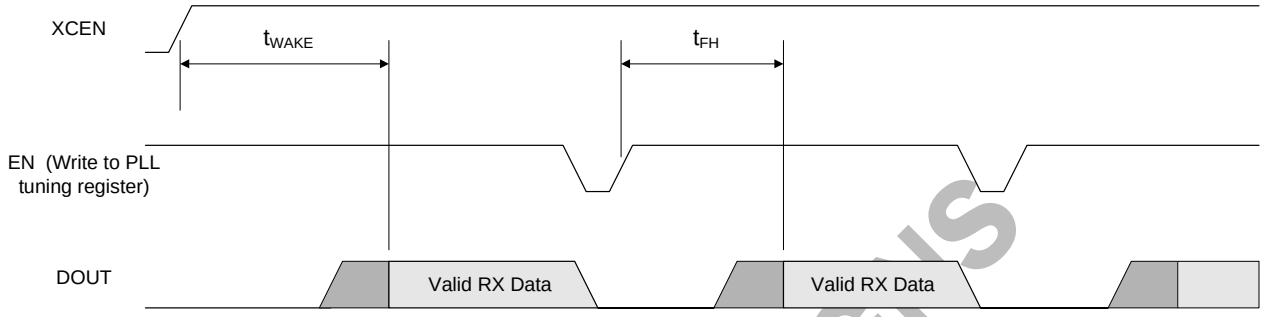


Figure 4 Control Timing when Channel Scanning

Transmit and Receive Data Interfaces

There are two sets of transmit and receive data interfaces for the ML5805:

- Baseband Data: DIN, DOUT, AOUT, RXCLK, FREF, RSSI
- RF Data: RXIN, RXIP, TXO

Please refer to application schematic shown in Figure 5 for recommended component values.

Baseband Data: DIN, DOUT, AOUT, RXCLK

The DIN pin is a CMOS logic level serial data input for 2-FSK modulation on the radio channel. This DIN pin drives data bits into the transmit modulator. There is no re-timing of the chips, so the transmitted 2-FSK chips take their timing from this DIN pin.

The DOUT pin is a corresponding CMoS level digital data output. In DS-FSK mode the ML5805 is designed to operate as a Direct Sequence Spread Spectrum FSK transceiver in the 5.725GHz to 5.850GHz ISM band. The chip rate, bit rate, and spreading code are determined in the baseband processor and the FM deviation and transmit filtering are determined in the ML5805 transceiver.

Setting the AOUT bit in the serial register turns the AOUT pin into a buffered, single-ended output from the data filter. This can be used to drive an off-chip data slicer or an ADC input for a DSP data slicer.

When using the digital output DOUT, FM demodulation, data filtering and center slicing take place in the ML5805 receiver. A clock recovery circuit at the data slicer output extracts the receiver clock RXCLK for those application that do not have access to clock recovery circuitry.

The FREF pin is the master reference frequency (f_{ref}) input for the transceiver. It supplies the frequency for the RF channel frequency and the on-chip filter tuning. The FREF pin is a clipped sine input with on-chip biasing resistors. It can be driven by an AC-coupled sine-wave or a CMOS* logic source. FREF is used as a calibration frequency and as a timing reference in the control circuits. The reference source must be accurate to 20PPM.

The RSSI (Received Signal Strength Indicator) pin supplies a voltage that indicates the amplitude of the received RF signal. The RSSI voltage is proportional to the logarithm of the received power level. it can be connected to the input of an ADC on the baseband IC and is used during channel scanning to detect clear channels on which the radio can transmit.

*For V(f_{ref})>1.5Vp-p, the level of the reference spurious response ($f_{TX}\pm f_{ref}$) increases in proportion to V(f_{ref}). V(f_{ref}) levels that exceed 2.0Vp-p will cause the typical reference spur to be greater than -70dBc.

RF Data: RXIN, RXIP, TXO

The RXIN and RXIP receive input and the TXO transmit outputs are the only RF I/O pins. The RXIN and RXIP pins require a single-ended to differential conversion from a 50Ω input impedance and a matching network for best input noise figure and the TXO pin also requires a matching network for maximum power output into 50Ω (see Figure 5).

Transmit PA Power Supply

To operate the PA with a 3.3V to 3.6V regulated per supply connect V_BATT to the regulated supply and install jumper 1. In this configuration the V_BATT can not exceed the Absolute Maximum rating of 3.6V.

To operate the PA with an Unregulated Battery DC Power Supply connect VCCPA to the unregulated supply and install jumper 2 as shown in Figure 5.

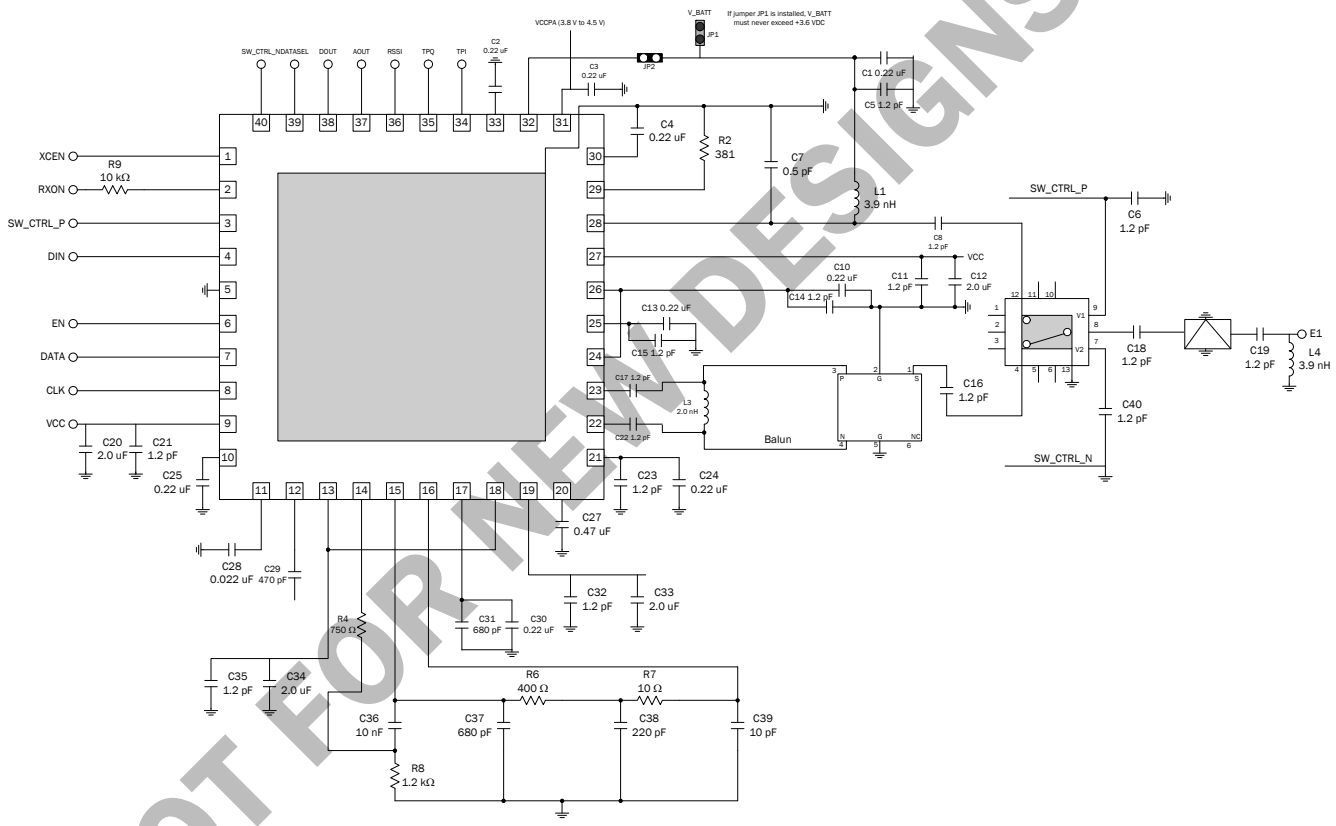


Figure 5 ML5805 Application Schematic

Serial Bus Control: EN, DATA, CLK

A 3-wire serial interface is used for programming the ML5805 configuration registers, which control device mode of operation, pin functions, PLL and reference dividers, internal test modes, and filter alignment. Data words are entered beginning with MSB. The 24 bit configuration register word consists of 5 bit address and 16 bit data fields. When the address field has been decoded the destination register is loaded on the rising edge of EN. Note: Providing less than 24 bits of data will result in unpredictable behavior when EN goes high.

Data and clock signals are ignored when EN is high. When EN is low, data on the DATA pin is clocked into a shift registered by rising edges on the CLK pin. The information is loaded into the addressed latch when EN returns high. This serial interface bus is an industry standard bus commonly found on PLL devices. It can be efficiently programmed by either byte or 24-bit word oriented serial bus hardware. The data latches are implemented in CMos and use minimal power when the bus is inactive (see Figure 6 and Table 3).

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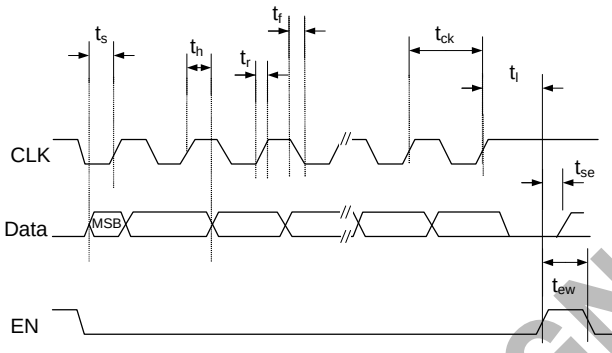

Figure 6 Serial Bus Timing Diagram

Symbol	Parameter	Min	Max	Units
Bus Clock (CLK)				
t_r	Clock input rise time (Note 1)		15	ns
t_r	Clock input fall time (Note 1)		15	ns
t_{ck}	Clock period	50		ns
Enable (EN)				
t_{ew}	Minimum pulse width	200		ns
t_r	Delay from last clock rising edge to rise of EN	15		ns
t_{se}	Enable set up time to ignore next rising clock	15		ns
Bus Data (DATA)				
t_s	Data to clock set up time	15		ns
t_n	Data to clock hold time	15		ns

Note 1: Serial I/O clock maximum rise and fall times are based on the minimum clock period. Longer rise and fall times can be accommodated for slower clocks provided the rise and fall times remain less than 20% of the clock period and all set up and hold time minimums are met with respect to the CMOS switching points (V_{IL} MAX and V_{IH} MIN). The serial I/O clock rise and fall times are limited to an absolute maximum of 100ns.

Serial Frequency Word and Configuration Registers

Bit				
23	22	21	20:16	15:0
0	PLL Frequency Word			
1	Reset	Wen	Address	CDATA (see Table 5)

Register	Bit															
(default)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0	TCMOD			RATE			UWD POL	PLLUL ACT	Reserved	Reserved	Reserved		Reserved			
(0x010E)	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	0
R1	CDRDLY				CDR EN	TXPADRV			RSSI DLY	PA FIRST	TXFILT EDGE	TXFILT POL	NOI VCOC	UW1 ERR	IFREGESEL	
(0x8080)	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
R2	Reserved		AOUT EN	TTXONB					TTXOFF		TTXONA					
(0x4080)	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0
R3	Reserved								DIVBASEOFFS				Reserved		Reserved	
(0x8886)	1	0	0	0	1	0	0	0	1	0	0	0	0	1	1	0
R4	MDCALV								Reserved							
(0xC008)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Serial Word Definitions

There are two types of serial words used, specified by the state of Bit 23. Bit 23=0 sets the serial word type to “frequency” and Bit 23=1 specifies the serial transaction type as a “configuration word”.

Bit	Definition
23	Specifies whether this serial transaction is type PLL frequency or type configuration register.
22:0	Data

Value	Definition
0	PLL frequency specification word.
1	Configuration register specification word.

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PLL Frequency Word
The PLL Frequency Word may be sent during standby (XCEN=0) or operation (XCEN=1).

Bit	Value	Definition
23	0	Specifies PLL frequency word.
22:20	IPART	Interger part of the PLL programming variable.
19:0	FPART	Fractional part of the PLL programming variable.

The frequency of the channel controlled by the configuration PLL Frequency Word, defined above, and the input reference frequency. The expression for the channel frequency is:

$$f_{ch} = 3f_{ref}\left[H + I + \frac{N}{2^{20}}\right]MHz$$

where:

N=FPART (the fractional part of the DSM programming value),

I=IPART (the interger part of the DSM programming value),

H=DIVBASEOFFS + 147 for f_{ref}=12.288MHz (RATE=2, 3, or 4),

DIVBASEOFFS + 130 for f_{ref}=13.824MHz (RATE=0 or 1),

DIVBASEOFF=a variable defined in Register 3 (default=8),

RATE=a variable defined in Register 0 (default=0),

f_{ref}=12.288MHz or 13.82MHz

Configuration Register Serial Word
The configuration registers are written only during standby mode (XCEN=0). These data registers are volatile and will erase when VCC is removed. The format is shown below:

Bit	Value	Definition
23	1	This is a configuration register transaction.
22	RESET	
21	1	Must be set to write to register.
20:16	ADDRESS	Register address (value=0, 1, 2, 3, or 4).
15:0	CDATA	Configuration Register data.

Value	Definition
0	Normal operation.
1	Perform reset operation. Must be asserted on first serial transfer.

All registers (R0, R1, R2, R3, and R4) will be loaded with default values and need to be initialized by the system base band hardware for the data rate used. See Table 6 following this section.

Register 0

Register 0 is a special because some of the hardware is controlled directly from this register. Since those specific bits are connected physically to active hardware, they must always be written first after power on. If register 0 is not initialized first by the band hardware the ML5805 will not operate correctly.

Bit	Variable	Default	Definition
15:13	TCMOD	0	Selects one of eight possible data slicer time constant combinations.
12:10	RATE	0	Selects one of eight possible bit rate combinations. Selected bit rates are dependent on external crystal frequency supplied.
9	UWDPOL	0	1: Invert the default DECT Unique Word (UWD) pattern. 0: Use the default DECT Unique Word (UWD) pattern.
8	PLLULACT	1	
7	(spare)	0	Spare bit
6	RESERVED	0	RESERVED
5:4	RESERVED	0	RESERVED
3:0	RESERVED	0xE	RESERVED

Value	Definition
0	Forces 300µS
1	Forces 6µS
2	Forces 3µS
3	Forces 2µS
4	External selection between 300µS and 6µS
5	External selection between 300µS and 3µS
6	Use Unique Word Detect mode and force 6µS
7	Use Unique Word Detect mode and forces 3µS

Value	Definition
0	576kbps (at 13.824MHz)
1	1,152kbps (at 13.82MHz)
2	1,536kbps (at 12.288MHz)
3	1,755kbps (at 12.288MHz)
4	2,048kbps (at 12.288MHz)
5	Not defined.
6	Not defined.
7	Not defined.

Value	Definition
0	PA will always turn on.
1	If the PLL does not lock the PA does not turn on.

Register 1

Bit	Variable	Default	Definition
15:12	CDRDLY	8	Recovered Data Clock Delay (RDC_{delay}) is the delay between the rising edge of RX data and the rising edge of the recovered RX data clock. The CDRDLY variable sets this delay as follow: $RDC_{delay}=CDRCLY/(2xf_{ref})$ [default $RDC_{delay}=325ms$]
11	CDREN	0	1: enable RDC_{delay} 0: RDC_{delay} is not used
10:8	TXPADRV	0	Current setting for PA.
7	RSSIDLY	1	1: RSSI output is masked until the PLL is finished tuning. 0: RSSI will function during the PLL tuning change time.
6	PAFIRST	0	1: the PA turns on before the external switch controls change. 0: the external switch controls change before the PA is turned on.
5	TXFILTEDGE	0	1: clock TX data on the falling edge of the reference clock. 0: clock TX data on the rising edge of the reference clock.
4	TXFILTPOL	0	1: Invert the data before filtering. 0: no data inversion applied.
3	NOIVCOC	0	1: no incremental VCO calibration, only incremental IF calibration 0: perform both VCO and IF incremental calibrations.
2	UW1ERR	0	1: one error is allowed for the DECT unique word detection. 0: zero errors are allowed for the DECT unique word detection.
1:0	IFREGSEL	0	IF and PA Circuit Regulator Voltages. *Not Recommended for Use - exceeds Absolute Maximum Ratings

Value	Definition
0	Bias current setting=63uA
1	Bias current setting=280uA
2	Bias current setting=368uA
3	Bias current setting=605uA
4	Bias current setting=605uA
5	Bias current setting=822uA
6	Bias current setting=930uA
7	Bias current setting=1177uA

Value	Definition
0	Regular output=3.3V
1	Not valid
2	Regular output=3.44V
3	Regular output=3.67V

Register 2

Bit	Variable	Default	Definition
15:14	RESERVED	1	RESERVED
13	AOUTEN	0	1: use the analog output 0: use the digital output
12:8	TTXONB	0	PA on to T/R switch delay (see Table 2)
7:6	TTXOFF	2	PA off to T/R switch delay (see Table 2)
5:0	TTXONA	0	RX to TX delay time (see Table 2)

Register 3

Bit	Variable	Default	Definition
15:12	RESERVED	0	RESERVED
11:8	RESERVED	0	RESERVED
7:4	DIVBASEOFFS	8	Offset to interger portion of PLL programming.
3:2	RESERVED	1	RESERVED
1:0	RESERVED	2	RESERVED

Register 4

Bit	Variable	Power-on Default	Rate Variable	Definition
15:8	MDCALV	0x38 0x45 0x5D 0x60 0x50 0x00 0x00 0x00	0 1 2 3 4 5 6 7	Frequency Modulation Deviation value. Small adjustments to MDCALV will tune the modulation spectrum. Note: At power-on, the MDCALV default value corresponding to the RATE variable of Register 0 is written to this register. Factory optimized values for MDCALV are shown in Table 6.
7:0	RESERVED	0		RESERVED

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Recommended Configuration Register Values

Register	Data Rate (kbps)				
	576	1152	1536	1755	2048
R0	0x817E	0x857E	0x897E	0x8D7E	0x917E
R1	0xF482	0xF482	0xC482	0x8482	0x8482
R2	0x4000	0x4000	0x4000	0x4000	0x4000
R3	0x8880	0x8880	0x8880	0x8880	0x8880
R4	0x3600	0x4800	0x5F00	0x6400	0x5200

Please consult with an RFMD application engineer for updates to these values or if you have special configuration requirements. The recommended register settings in Table 6 initialize the ML5805 as follows:

- DOUT enabled (AOUT disabled)
- 6µs/300µs data slicer time constant
- CDR disabled
- RSSI muting while PLL is not locked
- 3.44V PA regulator
- Minimum RX to TX delay
- Minimum PA on to T/R switch delay
- Minimum PA off to T/R switch delay

Recommended use model to achieve optimum performance

The focus will be on protocol frame preamble header field optimization based on a key subset of the feature and trade-offs that are available with the ML5805. The baseline optimizations can be expanded to meet the application requirements.

The transmit frame ramp and preamble header fields are key. The trade-offs are based on the system requirements, selected features, etc. In the receive frame header fields the number of received bits of one/zero preamble and the switching of the data slicer time constant are key. In designs where maximum reliable data transfer is required the frame preamble header field timing can be reduced and optimized with the trade-off of a little added complexity.

The trade-offs for the following examples will be explored in detail:

Example 1 - DOUT, CDR disabled, Incremental VCO Calibration

Example 2 - DOUT, CDR enabled, Incremental VCO Calibration

Example 3 - DOUT, CDR disabled, No Incremental VCO Calibration

Background

With XCEN active and when RXON is asserted the ML5805 switch from transmit to receive mode, the receiver is powered on and prior to entering receive mode, the ML5805 goes through a “self-calibration” sequence and then enters receive mode. At this point the on-chip data slicer that produces the digital data presented at the DOUT pin needs to establish a slice point. The condition to establish a slice point at is that the receiver must be receiving the frame header preamble field one/zero pattern for the required interval which is determined by the selected time constant. The data slicer was designed so the slice point can be established with one time constant then seamlessly switched to another without disturbing the establish reference. There are two methods for switching the time constants. It can be directly set to a fixed value by programming register 0 or by setting the state of the DATASEL pin 39. The modes that are available for the DATASEL pin are configured also by register 0. There are eight possible data slicer time constant combinations; refer to Register 0 - TCMOD bits above in the “Serial Frequency Word and Configuration Registers” section.

The ML5805 allows for the control of the "self-calibration" sequence, where the VCO, IF and data filters are frequency aligned.One option allows for the Incremental VCO Calibration to be turned off. This can greatly reduce the transition times from TX to RX but extreme care must be exercised and provisions need to be included in the protocol design. The primary function of the Incremental VCO Calibration is to make sure the ML5805 selected VCO can tune the full frequency range. When XCEN is first asserted, the ML5805 does a full calibration cycle. The selected VCO will be able to tune the full frequency range. Over time, if the temperature changes while the ML5805 is active and Incremental VCO Calibration is turned off, the Incremental VCO Calibration will need to be turned on for a single burst. This protocol will need to accommodate the required longer time for that burst. This time interval for this burst is based on the system requirement but in general the time interval should be less than what is expected for a change of 15°C. If the temperature change is unqualifiable or indeterminate then it is recommended that Incremental VCO Calibration is always used. Refer to Register 1 - NOIVCOC bit above in the "Serial Frequency Word and Configuration Registers" section.

The ML5805 receiver has a clock recovery circuit at the data slicer output that can extract the receiver clock RXCLK on pin 40 for those applications that do not have access to clock recovery circuitry. The CDR is available shortly after RXON although it is free running. After the clock acquisition window the CDR is aligned with the valid RX data. The duty cycle of RX data is not always fixed no matter how many training bits are given so the CDR falling edge is not always in the middle of RX data even using the optimized CDRDLY. The CDR can track approximately a ±500ppm frequency error. Beyond that error limit the BER starts to degrade. The use of the CDR will introduce additional considerations in the protocol. Refer to Register 1 - CDREN bit above in the "Serial Frequency Word and Configuration Registers" section.

Recommended Operation

Example 1 - DOUT, CDR disabled, Incremental VCO Calibration

Design a 1,536kbps system that will be robust, provide high reliability, immune to temperature change, providing maximum signal detectibility and sensitivity. Develop a transmit frame ramp and preamble header field that will provide the minimum receive frame header preamble field of the one/zero pattern. Define the data slicer time constant requirements to provide optimum performance.

Based on the provide maximum signal detectibility and sensitivity the data slicer time constant mode in register 0 - TCMOD 4 - DATASEL selects between 300µs and 6µs data slicer time constant is chosen. The transmit frame ramp and preamble header field will need to be a minimum of 50µs of a one/zero pattern. This will meet the receive frame header preamble field requirement of a minimum of 20µs of a one/zero pattern needed to establish the data slice point at the 6ms data slicer time constant. After the 20µs of a one/zero pattern have been received, the time constant needs to be switched to 300µs by setting DATASEL=VIL to receive the reset of the frame. Refer to Figure 7.

Example 2 - DOUT, CDR enabled, Incremental VCO Calibration

Design a 1,536kbps system that will be robust, provide high reliability, be immune to temperature change, provide maximum signal detectibility, maximum sensitivity, and provides a recovered data clock. Develop a transmit frame ramp and preamble header field that will provide the minimum receive frame header preamble field of the one/zero pattern. Define the data slicer time constant requirements to provide optimum performance.

Based on the provide maximum signal detectibility and sensitivity the data slicer time constant mode in register 0 - TCMOD 4 - DATASEL selects between 300µs and 6µs data slicer time constant is chosen. The transmit frame ramp and preamble header field will need to be a minimum of 50µs of a one/zero pattern. This will meet the receive frame header preamble field requirement of a minimum of 20µs of a one/zero pattern needed to establish the data slice point at the 6µs data slicer time constant. The one/zero pattern will need to be detected as illustrated in Figure 7 - Pattern_Valid. The clock recovery acquisition window ends and a valid RXCLK is available approximately 100µs after the one/zero pattern is valid. Following the 20µs of a one/zero pattern which has been received and before the end of the clock recovery acquisition window the time constant needs to be switched to 300µs by setting DATASEL=VIL to receive the reset of the frame. Refer to Figure 7.

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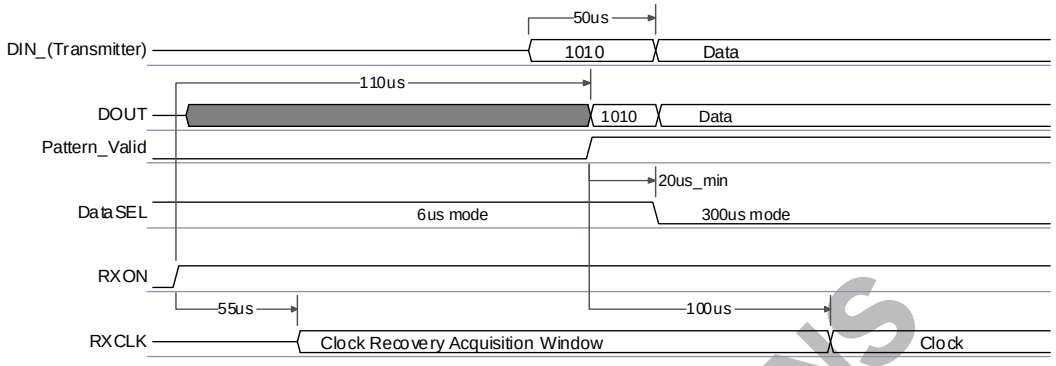
Figure 7 Recommended Timing



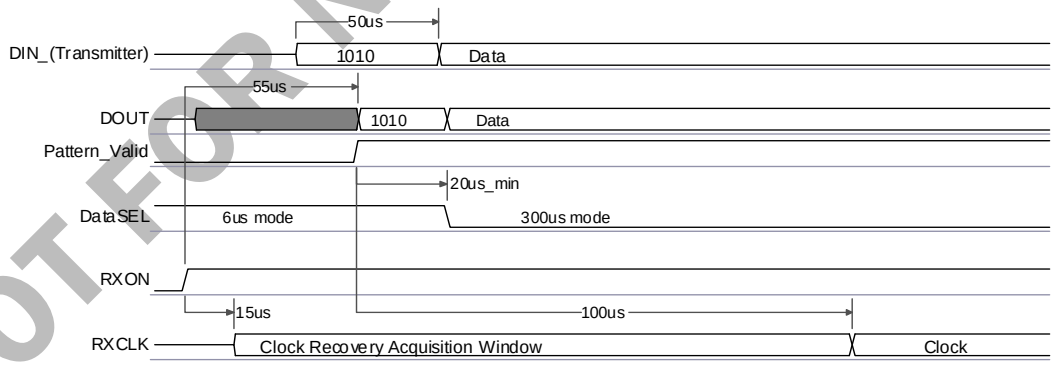
Operation with no Incremental VCO Calibration option

Example 3 - DOUT, CDR disabled, No Incremental VCO Calibration

Design a 1,536kbps system that will provide high reliability, maximum data through put, maximum signal detectibility and sensitivity. Maximum rate of temperature change is 5°C/min. Develop a transmit frame ramp and preamble header field that will provide the minimum receive frame header preamble of the one/zero pattern. Define the data slicer time constant requirements to provide optimum performance.

Based on the provide maximum signal detectibility and sensitivity the data slicer time constant mode in register 0 - TCMOD 4 - DATASEL selects between 300µs and 6µs data slicer time constant is chosen. The transmit frame ramp and preamble header field will need to be a minimum of 50µs of a one/zero pattern. This will meet the receive frame header preamble field requirement of a minimum of 20µs of a one/zero pattern needed to establish the data slice point at the 6ms data slicer time constant. After the 20µs of a one/zero pattern has been received the time constant needs to be switched to 300µs by setting DATASEL=VIL to receive the reset of the frame. Every three minutes a data frame that meets the timing of Example 1 will be sent. Refer to Figure 8.

Figure 8 Optional Timing with no Incremental VCO Calibration



Additional Areas of Optimization

As can be seen on by the examples above the protocol requirements are very similar and based on the application requirements, there are a number of trade-offs. Based on Data Rates, Signal to Noise, Signal dEtectibility, and Sensitivity drive many of the design needs. For example, if the system has a high signal = –80dBm, then the data slicer time constant mode in register 0 - TCMOD 5 - DATASEL selects between 300µs and 3µs. Data slicer time constant could have been chosen for the above examples. The effect would reduce the transmit frame ramp and preamble header field from a minimum of 50µs to 25µs of a one/zero pattern. This would meet the receive frame header preamble field reduced requirement from a minimum of 20µs to 10µs of a one/zero pattern needed to establish the data slice point at the 3µs data slicer time constant.

Also, depending on the system conditions, it has been found that the CDR acquisition window time and performance can be improved by using a mix of different data patterns in the frame preamble header field. In one instance the frame ramp and preamble header field started with the one/zero pattern to set the data slicer time constant and switched to a 1100 pattern for the rest of the CDR acquisition window which reduces the lock time.

Typical Performance Data

Unless otherwise specified T_A=25°C and the supply voltage is VCC=3.3V, VCC_PA=3.6V, R_{ISET}=381Ω, FREF=12.288MHz, DATA RATE=1.536Mbps, all measurements are normalized to the IC pins.

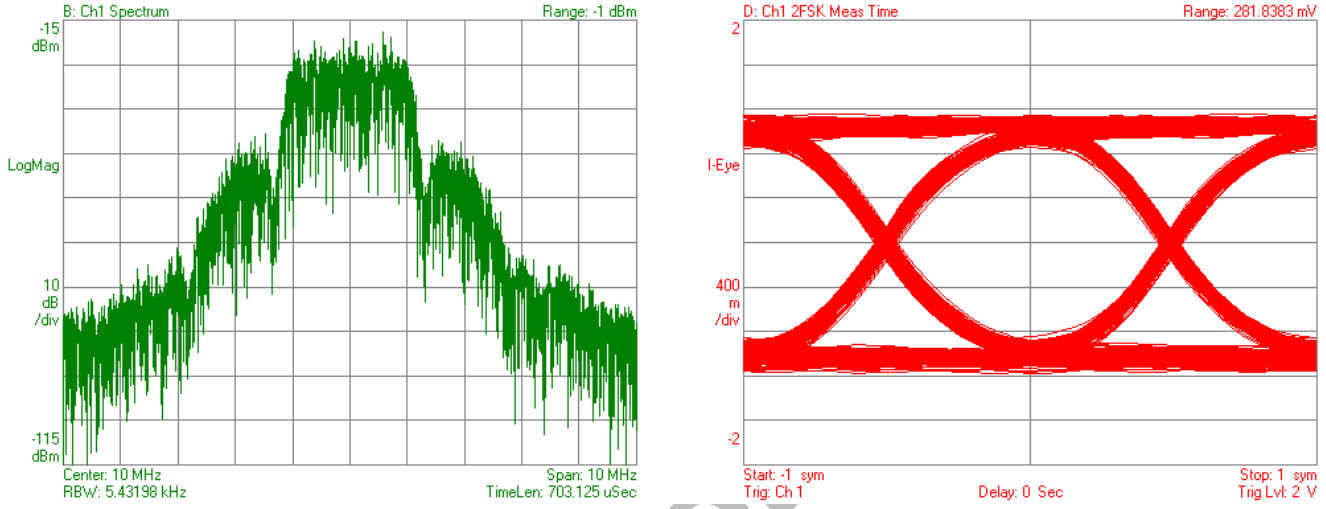


Figure 9 TX output spectrum and eye diagram for 2.048Mbps, PN20 digital mode.

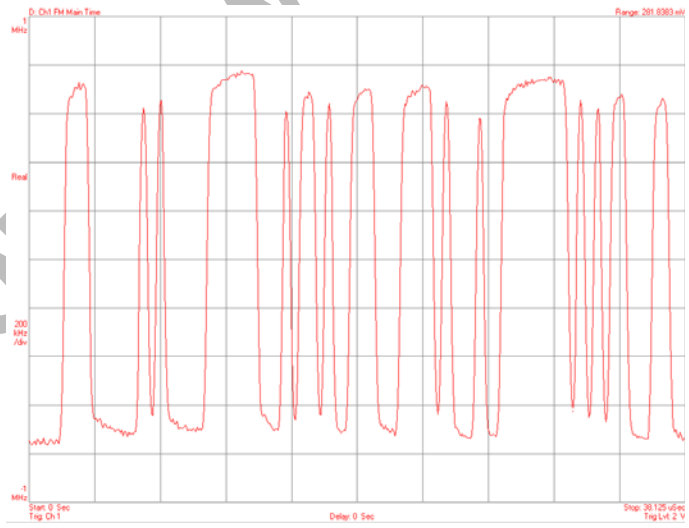


Figure 10 Measured frequency deviation in the time domain for 2.048Mbps, PN20 digital mode.

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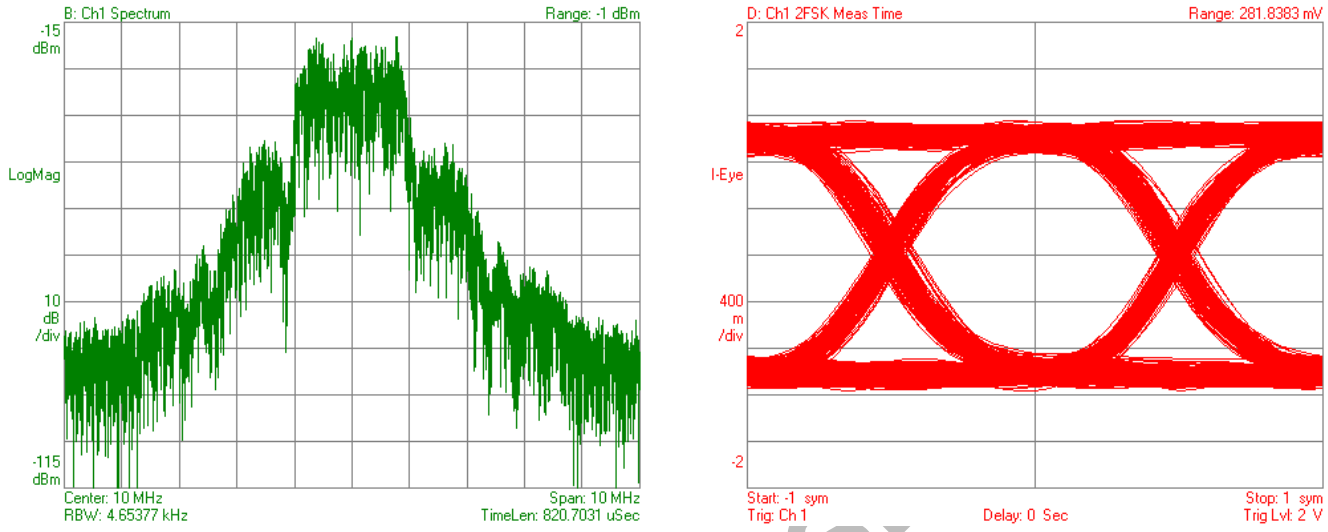

Figure 11 TX output spectrum and eye diagram for 1.755 Mbps, PN20 digital mode.

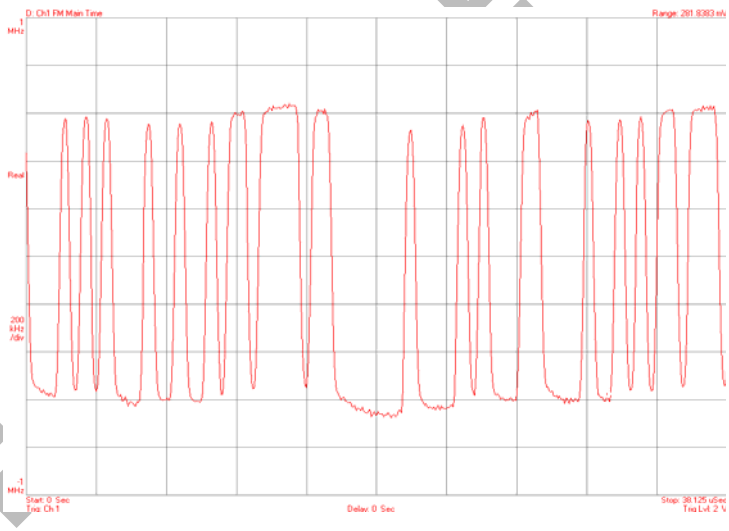

Figure 12 Measured frequency deviation in the time domain for 1.755 Mbps, PN20 digital mode.

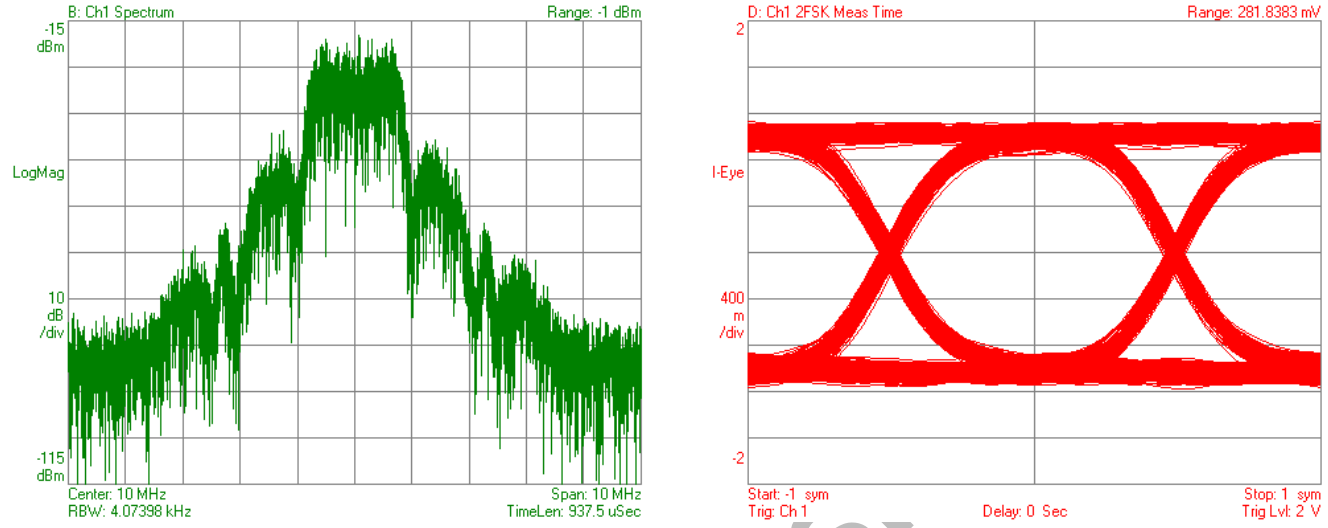

Figure 13 TX output spectrum and eye diagram for 1.536Mbps, PN20 digital mode.

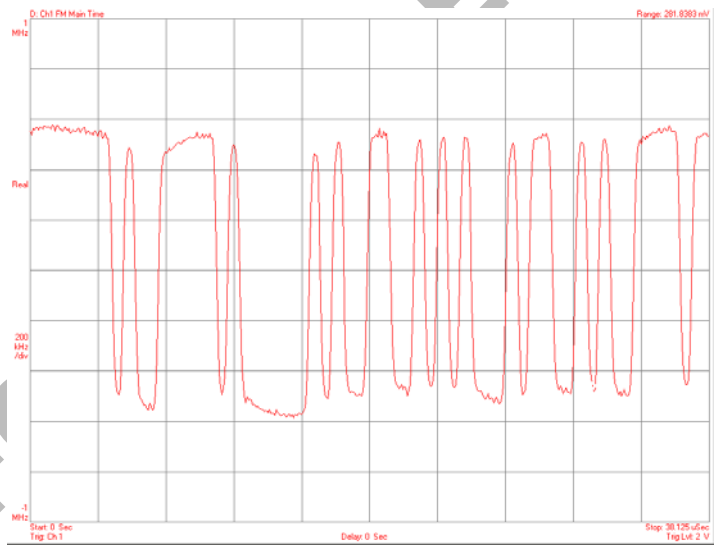

Figure 14 Measured frequency deviation in the time domain for 1.536Mbps, PN20 digital mode.

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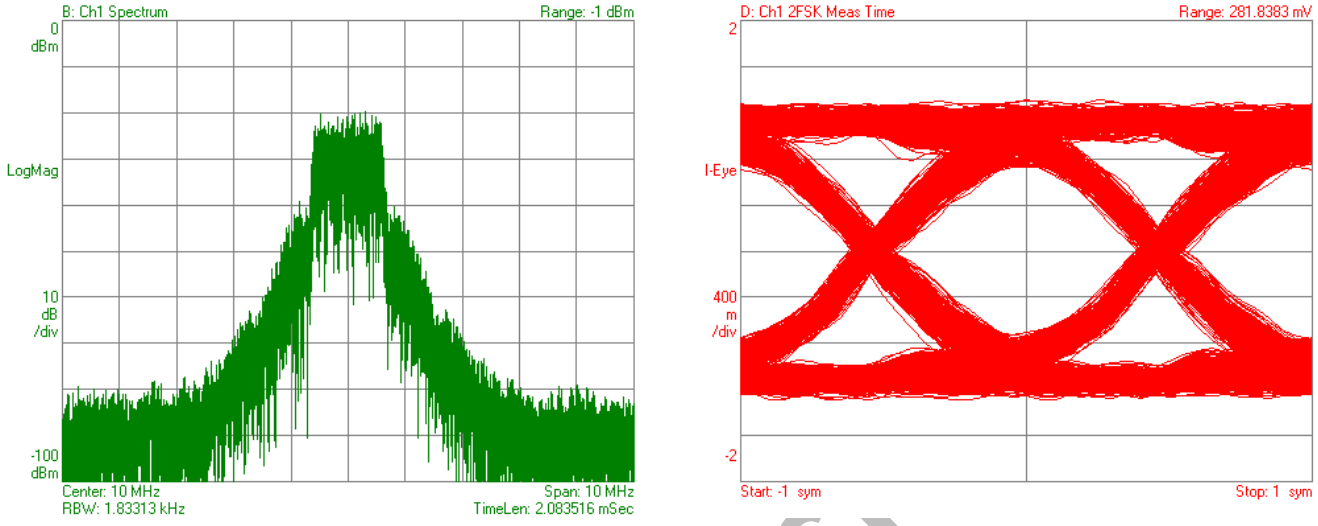

Figure 15 TX output spectrum and eye diagram for 1.152 Mbps, PN20 digital mode.

Figure 16 Measured frequency deviation in the time domain for 1.152 Mbps, PN20 digital mode.

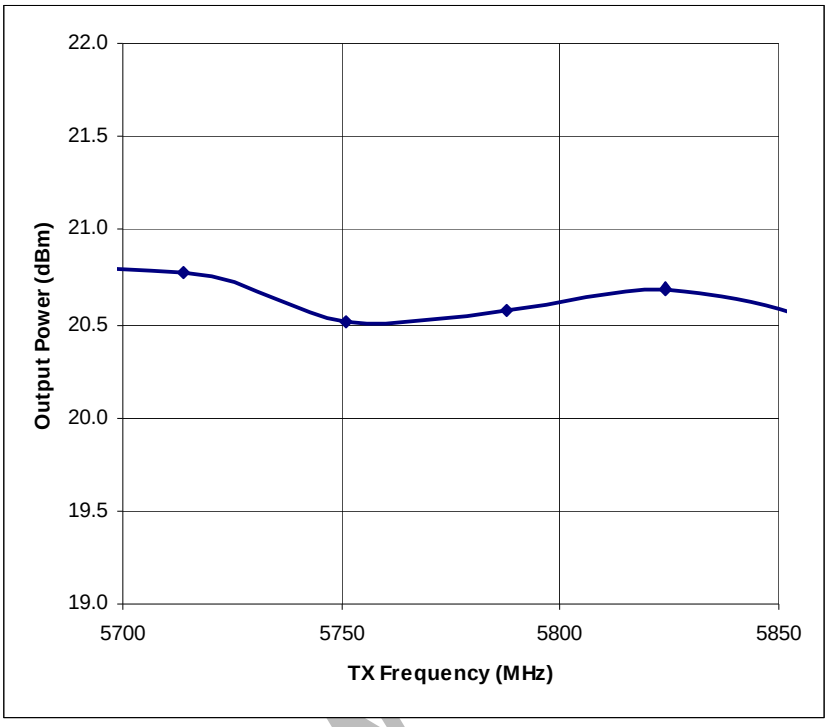

Figure 17 Transmit Power versus Frequency

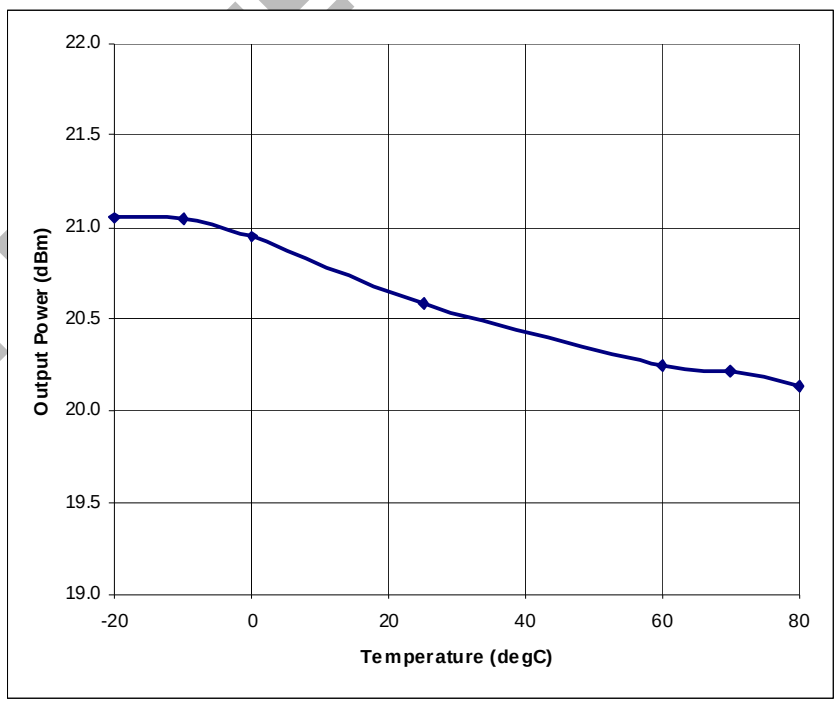

Figure 18 Transmit Power versus Temperature

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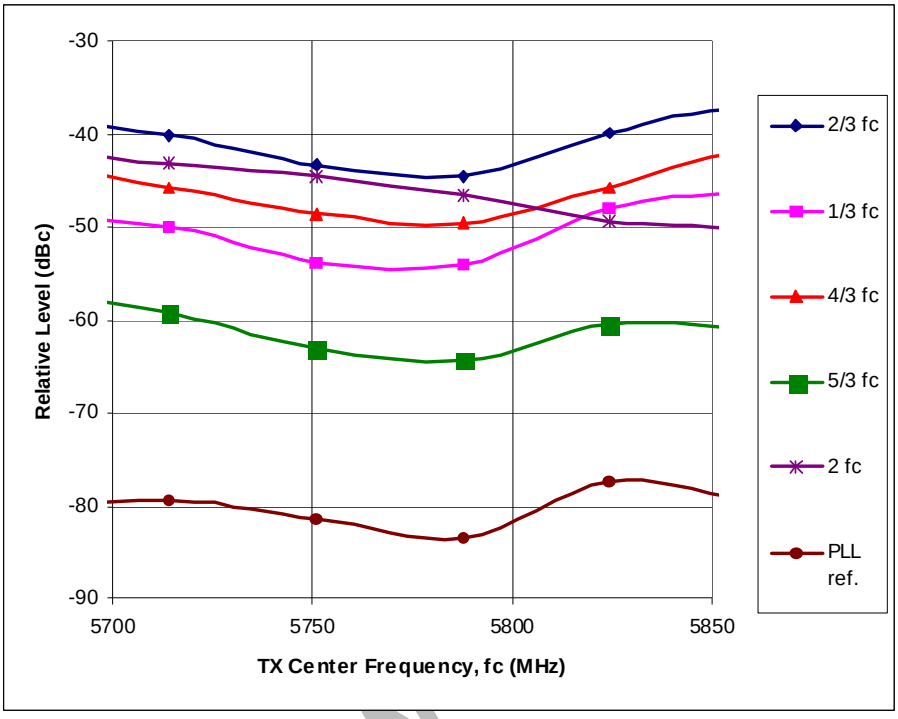

Figure 19 TX Harmonics and Sub-Harmonics versus Frequency

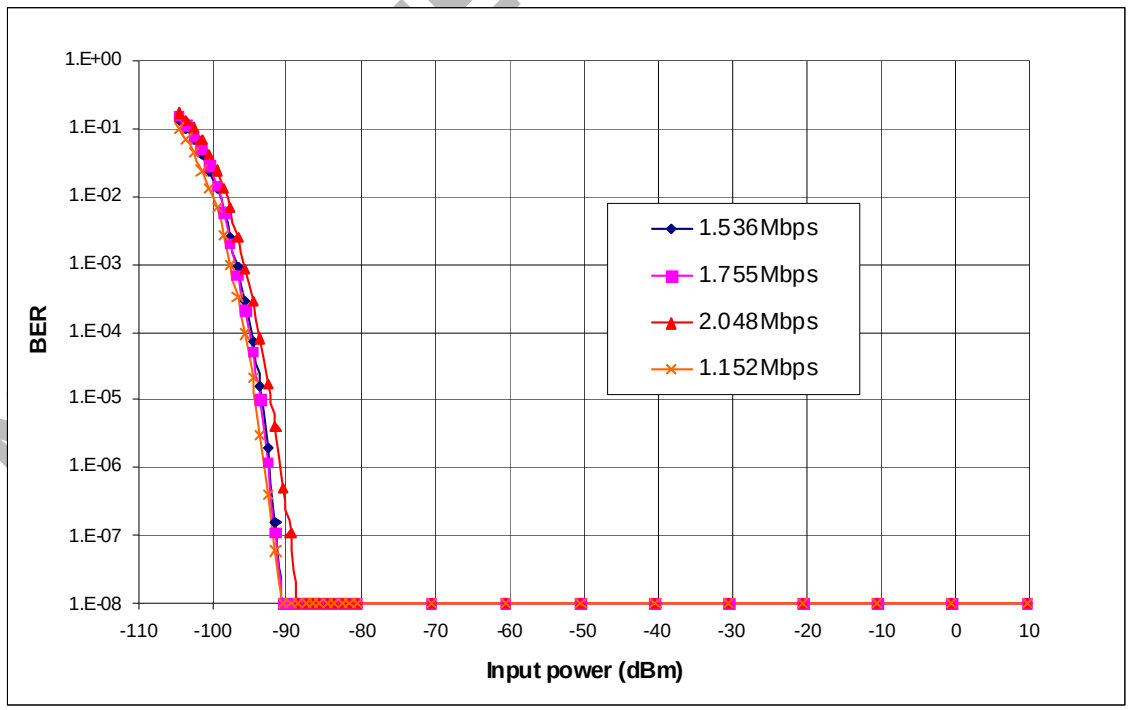

Figure 20 Bit Error Rate versus Data Date

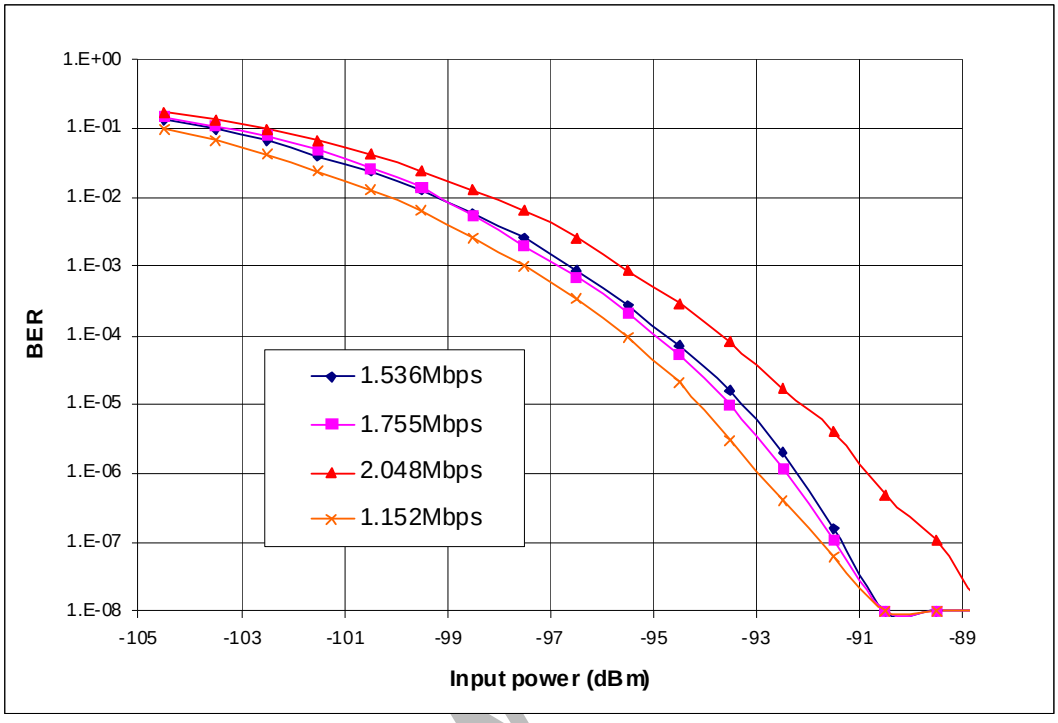

Figure 21 Bit Error Rate versus Data Rate

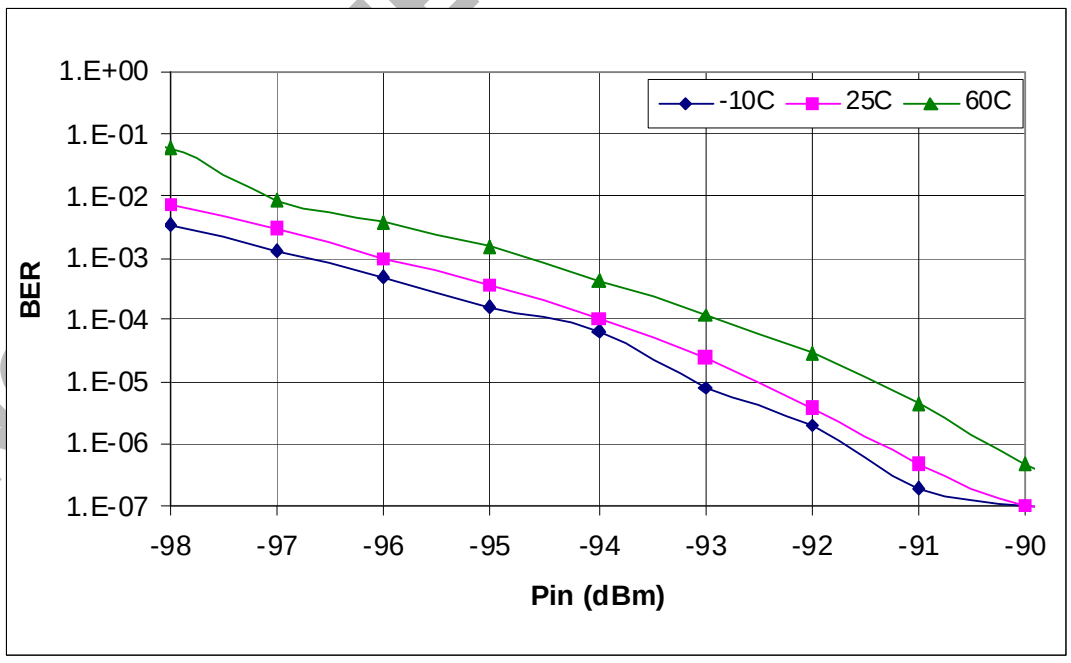

Figure 22 Bit Error Rate versus Temperature (2.048Mbps)

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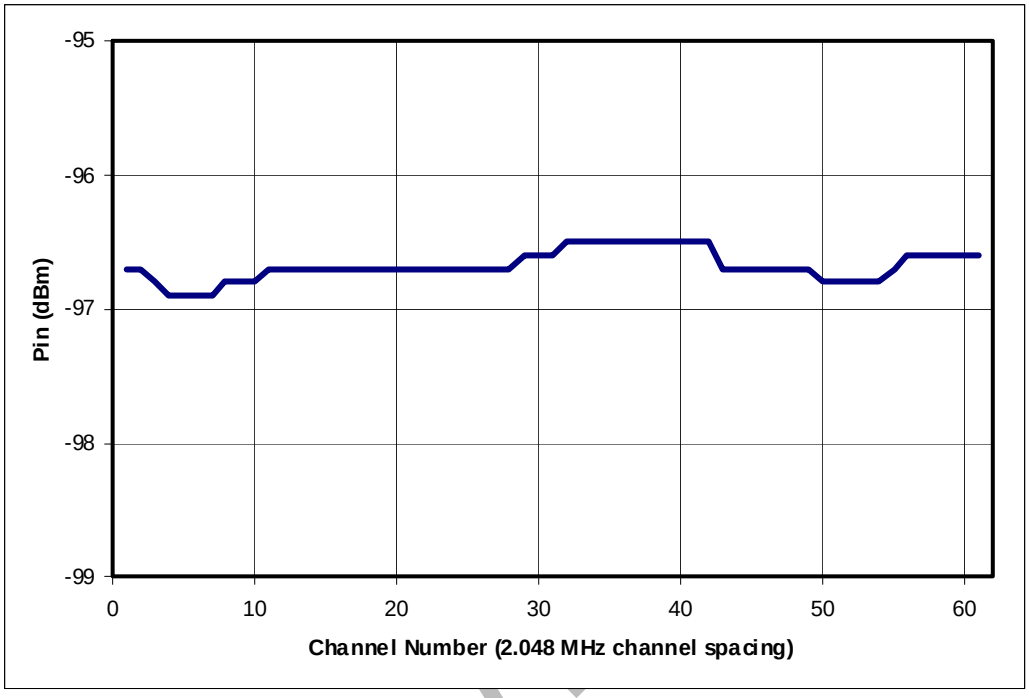

Figure 23 0.10% Bit Error Rate versus Channel)1.536Mbps

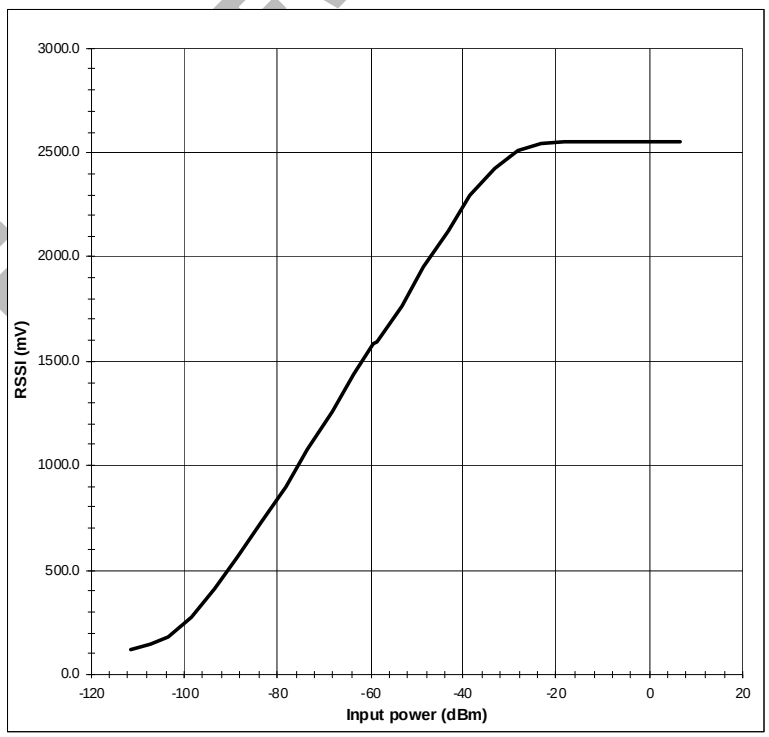

Figure 24 RSSI versus Input Power

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Physical Dimensions

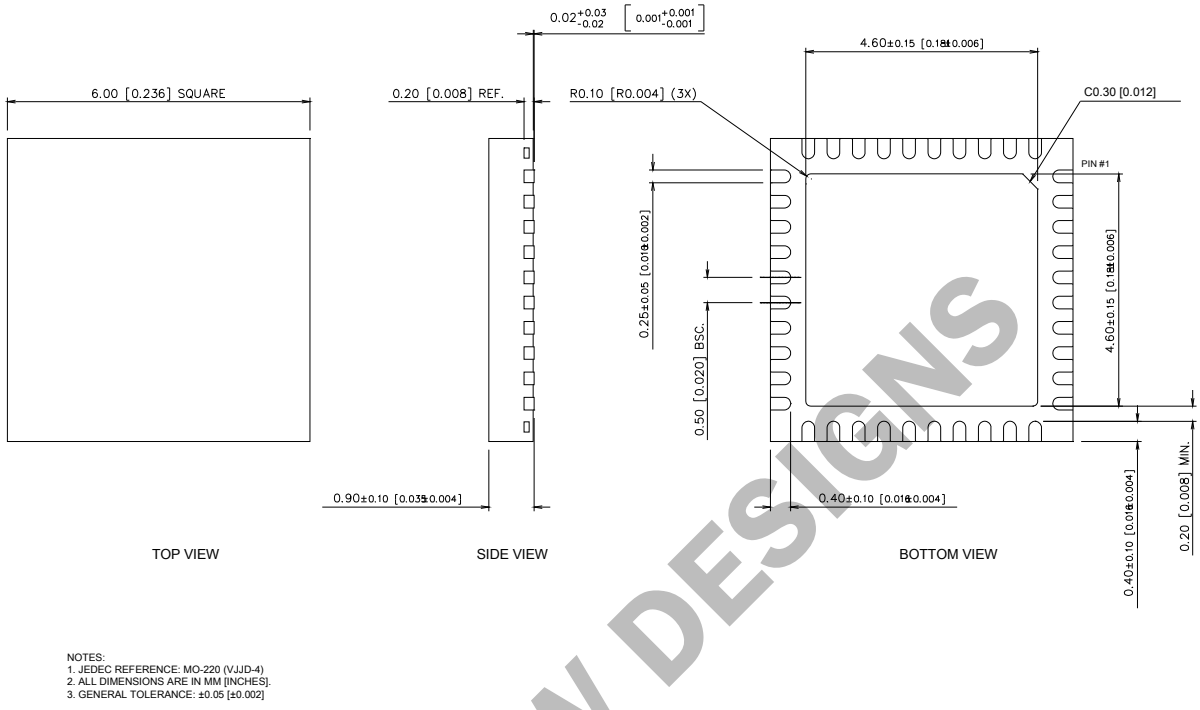

Figure 25 40-Pin QFN Package Dimensions

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