PCN Number:	20190805001	PCN Date:	Aug. 6, 2019
Title:	Datasheet for LMK04610		
Customer Contact:	PCN Manager	Dept:	Quality Services
Proposed 1st Ship Date:	Nov. 6, 2019		
Change Type:			

☐	Assembly Site	☐	Design	☐	Wafer Bump Site
☐	Assembly Process	☒	Data Sheet	☐	Wafer Bump Material
☐	Assembly Materials	☐	Part number change	☐	Wafer Bump Process
☐	Mechanical Specification	☐	Test Site	☐	Wafer Fab Site
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Materials
				☐	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing a change.
The product datasheet(s) is being updated as summarized below.

TEXAS INSTRUMENTS

LMK04610

SNAS699B – JANUARY 2017 – REVISED JULY 2019

Changes from Revision A (June 2017) to Revision B **Page**

- Removed bulleted list under the *Dual Loop PLL Architecture* feature bullet 1
- Added *Ultra Low Noise* feature bullets 1
- Changed VCO frequency units from: 5.8 to 6.175 GHz to: 5870 MHz to 6175 MHz 1
- Added LMK04616 device configuration information 4
- Changed VCO frequency from: 5800 MHz to: 5870 MHz 4
- Added PACKAGE column to device configuration information table 4
- Added LMK04616 row to device configuration information table 4
- Added Footnote and link to LMK04616 datasheet 4
- Added OSCout polarity information to the OSCout/OSCout* pin description 6
- Changed PLL1 phase detector maximum frequency from 40 MHz to 4 MHz 11
- Changed VCO tuning range minimum from: 5800 to: 5870 11
- Changed V_{OD} symbol to $V_{OD,pp}$ to match mVpp units. 12
- Changed V_{OD} symbol to $V_{OD,pp}$ to match mVpp units. 13
- Added content to the *HSDS 4/6/8mA* section 20
- Added content to the *HCSL* section 21
- Changed the *VCXO Buffered Output* section 22

- Changed VCO frequency to 5870 MHz to 6175 MHz and updated max output frequency to 2058 MHz 23
- Added content to the *Programmable Output Formats* section 23
- Changed *HSDS to LVPECL With Bias Voltage Vb* graphic caption 31
- Changed *HCSL to LVPECL* graphic 31
- Changed *HSDS to LVPECL With Bias Voltage Vb* graphic caption 32
- Changed *HSDS to LVPECL* graphic 32
- Added content to the *OSCout* section 35
- Added OSCin to OSCout differential results in clock inversion from OSCin to OSCout. 35
- Added Note to use TICS Pro EVM tool to calculate SDPLL loop filter values. 38
- Changed PLL1_PROP max from 255 to 127. 38
- Added PLL1_PROP_FL to table. 38
- Changed PLL1_FBCLK_INV and CLKinx_PLL1_INV for Low Pulse mode 38
- Changed PLL1_FBCLK_INV and CLKinx_PLL1_INV for High Pulse mode 38
- Deleted Examples of PLL1 Setting 38
- Changed the tuning range of the oscillator from: 5800 MHz to: 5870 MHz 40
- Added PLL2 DLD programming information and updated the PLLx DLD flowchart graphic 41
- Changed PLL1_STORAGE_CELL description from 40-bit thermometer code to 6-bit decimal value 44
- Clarified CTRL_VCXO represented as PLL1_STORAGE_CELL value 44
- Changed section from: *Low Skew Mode* to: *Zero Delay Mode (ZDM)* 49
- Changed Set Prop/Store-CP from "fast lock" value to "non-fast lock" value at end of flowchart 51
- Deleted references to tunable crystal 52
- Deleted reference to CLKin2 and CLKin3 52
- Deleted use of external VCO for PLL2. 52
- Added register 0x85, 0x86, 0xF6, and 0xAD for PLL2 DLD to recommended programming sequence 55
- Changed PLL1_PROP from 8 bit to 7 bit field in register map 59
- Changed PLL1_PROP_FL from 8 bit to 7 bit field in register map 59
- Changed PLL1_STORAGE_CELL 40 bit to 6 bit field. Not a 40 bit thermometer code. Set registers 0x66, 0x67, 0x68, 0x69 to RSRVD in register map 59
- Changed PLL2_PROP from 8 bit to 6 bit field in register map 60
- Changed PLL2_INTG from 8 bit to 5 bit field in register map 60
- Added register 0xAC for field PLL1_TSTMODE_REF_FB_EN in register map 61
- Added register 0xAD for fields RESET_PLL2_DLD, PLL2_TSTMODE_REF_FB_EN, and PD_VCO_LDO in register map 61
- Added register 0xF6 for PLL2_DLD_EN in register map 61
- Deleted unused DEVID values 65
- Changed reset value for CHIPID from 0x1 to 0x3 65
- Changed reset value for CHIPVER from 0x1 to 0x1B 65
- Changed PLL1_PROP from 8 bit to 7 bit field in register definition 85
- Changed PLL1_PROP_FL from 8 bit to 7 bit field in register definition 85
- Deleted 'PLL1 Start-up in Holdover.' text from the PLL1_STARTUP_HOLDOVER_EN bit description 85
- Changed PLL2_PROP field size from 8 bits to 6 bits in register definition 90
- Changed PLL2_INTG field from 8 bit to 5 bit field in register 0x80 definition 92
- Added definition and requirement for setting PLL2_LD_WNDW_SIZE = 0 in register 0x85 definition 93
- Added definition and requirement for setting PLL2_LD_WNDW_SIZE_INITIAL = 0 in register 0x86 definition 93
- Added note for using PLL1/2 REF/FB(SYS) status output for STAT0 96
- Added note for using PLL1/2 REF/FB(SYS) status output for STAT1 97

- Added note for using PLL1/2 REF/FB(SYS) status output for SYNC 100
- Added register 0xAC to register description. New field PLL1_TSTMODE_REF_FB_EN. 101
- Added register 0xAD to register description. New fields RESET_PLL2_DLD, PLL2_TSTMODE_REF_FB_EN, and PD_VCO_LDO..... 101
- Added register 0xF6 to register description. New field PLL2_DLD_EN 102
- Added register 0xF7 to register description. New field PLL2_DUAL_LOOP_EN 102
- Changed Channel 5 and 6 FBClock Buffers from: Low Skew to: Zero Delay Mode..... 112
- Changed registers for WINDOW SIZE and LOCK COUNT. Updated equation to reflect the more general WINDOW SIZE and LOCK COUNT names and count frequency. Removed reference to holdover. Updated descriptive text 116
- Updated minimum lock time calculation example to reflect updated register names and count frequency 116
- Simplified HSDS format description 121

The datasheet number will be changing.

Device Family	Change From:	Change To:
LMK04610	SNAS699A	SNAS699B

http://www.ti.com/product/LMK04610RTQT

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

Electrical specification performance changes as indicated above.

Changes to product identification resulting from this PCN:

None.

Product Affected:

LMK04610RTQR	LMK04610RTQT		

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your Field Sales Representative.

Location	E-Mail
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