Process Change Notification

PCN Number: PCN-2016-33 **PCN Notification Date:** 03/07/2016

Initial PCN

Wafer Level Chip Scale Package Bump Assembly Site Transfer

Dear Customer,

This is notification of the Wafer Level Chip Scale Package (WLCSP) Bump Assembly Site Transfer from Siliconware Precision Industries Co., Ltd (SPIL) Chung Shan (CS) site to the Zhong Ke (ZK) site location in Taichung Taiwan.

The described change(s) within this PCN will not take effect (i.e. Shipped) any earlier than **90** days from the completion date of the Cirrus Logic qualification, unless a customer agreement has been reached on an earlier implementation of the identified process change or successful completion of the defined qualification has been realized.

Any negotiated alternative change requirements will be provided via the customer's defined process. Customers with previously negotiated, special requirements will be handled separately.

Cirrus Logic requests acknowledgement of receipt for this PCN notification within 30 calendar days and acceptance of the identified change(s) within 90 days contingent on the successful completion of the defined qualification; lack of acknowledgement / communication is considered as acceptance.

Cirrus Logic would like to take this opportunity to thank our customers for their cooperation and assistance in this respective matter. Any specific or immediate inquiries should be directed to your local Field Sales Representative.

Sincerely,

Quality Systems Administrator
Cirrus Logic Corporate Quality
Phone: +1(512) 851-4000

Process Change Notification

PCN Number: PCN-2016-33 **PCN Notification Date:** 03/07/2016

Products Affected:

The devices listed on this page are the complete list of affected devices. According to our records, these are the devices that you have purchased within the past twenty-four (24) months. The corresponding customer part number is also listed, if available.

Technical details of this Process / Product Change follow on the next page(s).

Title:	Wafer Level Chip Scale Package Bump Assembly Site Transfer from the Siliconware Precision Industries Co., Ltd (SPIL) Chung Shan (CS) site to the Zhong Ke (Ke) site location in Taichung Taiwan.				
Customer Contact:	Local Field Sales Representative	**Phone:**	(512) 851-4000	**Dept:**	Corporate Quality
Proposed 1st Ship Date:	OCT 2016	**Estimated Sample Availability Date:**	Q2 2016		
Change Type:	Site Transfer: Change Type = Major, but considered Minor; as the subcontractor (SPIL) is an existing qualified supplier for Cirrus Logic and there are no changes to the equipment or material.				

	Assembly Site		Assembly Process		Assembly Materials
	Wafer Fab Site		Wafer Fab Process		Wafer Fab Materials
X	Wafer Bump Site		Wafer Bump Process		Wafer Bump Material
	Test Site		Test Process		Design
	Electrical Specification		Mechanical Specification		Part Number
	Packing/Shipping/Labeling		Other		
Comments:					

PCN Details

Description of Change:

Cirrus Logic is qualifying the Wafer Level Chip Scale Package (WLCSP) Bump Assembly Site transfer from the Chung Shan (CS) site to the Zhong Ke (ZK) site location in Taichung Taiwan.

Below you will find an outline of the described changes for these components:
Special Note: Change Type = Major, but considered Minor.
The subcontractor (SPIL) is an existing qualified supplier and all material as well as equipment associated with the Bump Assembly process will not change.

- **Bump Assembly Site Change:**

  From: **SPIL Chung Shan (CS) site location in Taichung Taiwan**
  To: **SPIL Zhong Ke (ZK) site location in Taichung Taiwan**

Reason for Change:

Cirrus Logic's Wafer Level Chip Scale Package (WLCSP) Bump Assembly Site subcontractor - Siliconware Precision Industries Co., Ltd (SPIL) will transfer to their Zhong Ke (ZK) site from their existing Chung Shan (CS) site by the end of calendar year 2016.

Special Note:

Earlier production level material may be available from the qualified Zhong Ke (ZK) site location, but shipment(s) from Cirrus Logic are contingent on successful qualification completion of the designated site transfer.

Anticipated Impact on Form, Fit, Function, Quality or Reliability:

No anticipated adverse impact to the Quality and/or Reliability of said product; as the transfer site is part of an already existing Cirrus Logic qualified subcontractor Siliconware Precision Industries Co., Ltd. (SPIL) and there are no changes to the equipment or material.

Product Affected:

Device	Cirrus Logic Part Number	Customer Part Number
1	CS48L10-CWZ[R]	
2	CS48LV12-CWZ[R]	
3	CS48LV13-CWZ[R]	

Changes To Product Identification Resulting From This PCN:

The Cirrus Logic component symbolization on the external face of the device reflects the designated Assembly Site.

There is "NO CHANGE" to the external face of the designated components.

Below you will find a representative example:

Our part: **CS48L10-CWZ[R], CS48LV12-CWZ[R] and CS48LV13-CWZ[R]**
Mark format: **305[C]**

Line 1: Part Number (8 spaces max.)
Line 2: Package Mark (8 spaces max.)
Line 3: COO = Country Of Origin (3 characters)

Qualification Data:

This qualification has been specifically developed for the validation of this change. The qualification data validates that the proposed change meets the applicable released technical specifications.				
Qualification Schedule	**Start:**	May 2016	**End:**	July 2016

Qualification Device Construction Details		
Detail Description	**Device 1**	**Device 2**
Part Number(s):	CS48L10-CWZ[R], CS48LV12-CWZ[R] and CS48LV13-CWZ[R]	
Wafer Fab Site Code/Name:	TSMC	
Wafer Technology:	0.065um	
Die Size:	4.67 mm	
Assembly Site Code/Name:	SILICONWARE (Taiwan)	
Package Type/Code:	20 WLCSP (Wafer Level Chip Scale Package)	

The Qualification Plans are designed using JEDEC and other applicable industry standards. An overall summary of the Qualification results will be submitted upon completion.

CS48LXXX-CWZ[R] Qualification

CS48LXXX-CWZ [R] Qualification: ☒ **Plan** ☐ **Test Results**			
DIE & Package level Qualification Reliability Test			Sample Size (PASS/FAIL)
Pre-Conditioning	JEDEC J-STD-020 JESD22-A113	24Hr +125'C; MSL 3 192Hr 30'C / 60% RH Soak, (Reflow 260'C x 3) (3 Lots)	693 / 0
Temperature Cycle	JEDEC JESD22-A104	-40°C to +125°C for 850 cycles (3 Lots – 77pcs/Lot)	231 / 0
UHAST	JEDEC JESD22- A118	+110'C/85% RH, 17.7 PSIA, 264Hrs (3 Lots – 77pcs/Lot)	231 / 0
HAST	JEDEC JESD22 - A110	+110'C/85% RH, 17.7 PSIA, 264Hrs (3 Lots – 77pcs/Lot)	231 / 0
SD (Solderability)	JEDEC J-STD-002D	Condition C Section 4.2.9 Test S1: 95% Coverage (3 Lots – 5pcs/Lot)	15 Units / 0
SBS (Solder Ball Shear)	JEDEC JESD22-B117B AEC Q100-010	Characterization (3 Lots – 5pcs/Lot)	15 units / 0
PPD (Package Physical Dimensions)	Case Outline Drawing	Document Review / Meet all Case Outline drawing tolerances (3 Lots – 20pcs/Lot)	60 units / 0
HTSL (High Temperature Storage Life)	JEDEC JESD22-A103	+150°C for 1000Hrs (Read Points 500Hrs, 1000Hrs) (2 Lots – 45pcs/Lot)	90 / 0

Board Level Reliability Test			Sample Size (PASS/FAIL)
TC (Temperature Cycle)	JEDEC JESD22-A104 and Appendix 3	-40°C to +125°C for 1000 cycles Cycle Time 30mins (1 Lot – 45pcs)	45 Units / 0
Mechanical Shock	JEDEC JESD22-B111	Impact: > 1500 G (1 Lots – 45pcs/Lot)	45 Units / 0

Notes:

- Qualification tests "pass" on zero fails for each test