

NLAS3699B

Dual DPDT Ultra-Low R_{ON} Switch

The NLAS3699B is a dual independent ultra-low R_{ON} DPDT analog switch. This device is designed for low operating voltage, high current switching of speaker output for cell phone applications. It can switch a balanced stereo output. The NLAS3699B can handle a balanced microphone/speaker/ring-tone generator in a monophone mode. The device contains a break-before-make feature.

Features

- Single Supply Operation
1.65 to 4.5 V V_{CC}
Function Directly from LiON Battery
- Maximum Breakdown Voltage: 5.5 V
- Tiny 3 x 3 mm QFN Pb-Free Package
Meet JEDEC MO-220 Specifications
- Low Static Power
- This is a Pb-Free Device*

Typical Applications

- Cell Phone Speaker/Microphone Switching
- Ringtone-Chip/Amplifier Switching
- Four Unbalanced (Single-Ended) Switches
- Stereo Balanced (Push-Pull) Switching

Important Information

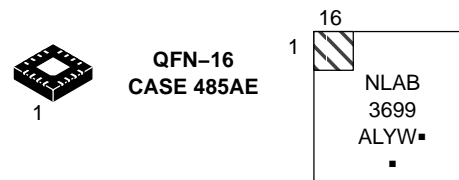
- ESD Protection:
HBM (Human Body Model) > 8000 V
MM (Machine Model) > 400 V
- Continuous Current Rating Through each Switch ± 300 mA
- Conforms to: JEDEC MO-220, Issue H, Variation VEED-6
- Pin for Pin Compatible with STG3699



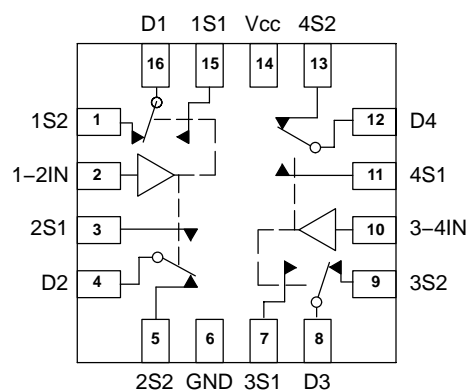
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAMS



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package
(Note: Microdot may be in either location)



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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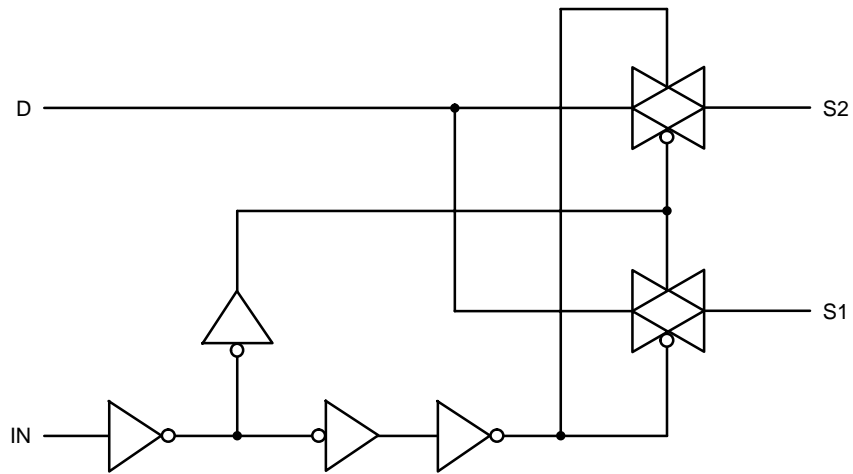


Figure 1. Input Equivalent Circuit

PIN DESCRIPTION

| QFN PIN # | Symbol | Name and Function |
|---------------------------|------------------------|-------------------------|
| 1, 3, 5, 7, 9, 11, 13, 15 | 1S1 to 4S1, 1S2 to 4S2 | Independent Channels |
| 2, 10 | 1-2IN, 3-4IN | Controls |
| 4, 8, 12, 16 | D1 to D4 | Common Channels |
| 6 | GND | Ground (V) |
| 14 | V _{CC} | Positive Supply Voltage |

TRUTH TABLE

| IN | S1 | S2 |
|----|--------|--------|
| H | ON | OFF(*) |
| L | OFF(*) | ON |

*High impedance.

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MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit | | | | |
|----------------|--|--|---|---|----|---|----|
| V_{CC} | Positive DC Supply Voltage | - 0.5 to +5.5 | V | | | | |
| V_{IS} | Analog Input Voltage (V_{NO} , V_{NC} , or V_{COM}) | $-0.5 \leq V_{IS} \leq V_{CC}$ | V | | | | |
| V_{IN} | Digital Select Input Voltage | $-0.5 \leq V_I \leq +5.5$ | V | | | | |
| I_{anI1} | Continuous DC Current from COM to NC/NO | ± 300 | mA | | | | |
| $I_{anI-pk 1}$ | Peak Current from COM to NC/NO, 10 duty cycle (Note 1) | ± 500 | mA | | | | |
| I_{clmp} | Continuous DC Current into COM/NO/NC with respect to V_{CC} or GND | ± 100 | mA | | | | |
| t_r, t_f | Input Rise or Fall Time, SELECT | $V_{CC} = 1.6\text{ V} - 2.7\text{ V}$ $V_{CC} = 3.0\text{ V} - 4.5\text{ V}$ | <table border="1"> <tr> <td>0</td> <td>20</td> </tr> <tr> <td>0</td> <td>10</td> </tr> </table> | 0 | 20 | 0 | 10 |
| 0 | 20 | | | | | | |
| 0 | 10 | | | | | | |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Defined as 10% ON, 90% off duty cycle.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit | | | | |
|------------|------------------------------------|--|---|--------------------|----|---|----|------|
| V_{CC} | DC Supply Voltage | 1.65 | 4.5 | V | | | | |
| V_{IN} | Digital Select Input Voltage | GND | V_{CC} | V | | | | |
| V_{IS} | Analog Input Voltage (NC, NO, COM) | GND | V_{CC} | V | | | | |
| T_A | Operating Temperature Range | -40 | +85 | $^{\circ}\text{C}$ | | | | |
| t_r, t_f | Input Rise or Fall Time, SELECT | $V_{CC} = 1.6\text{ V} - 2.7\text{ V}$ $V_{CC} = 3.0\text{ V} - 4.5\text{ V}$ | <table border="1"> <tr> <td>0</td> <td>20</td> </tr> <tr> <td>0</td> <td>10</td> </tr> </table> | 0 | 20 | 0 | 10 | ns/V |
| 0 | 20 | | | | | | | |
| 0 | 10 | | | | | | | |

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DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

| Symbol | Parameter | Condition | V _{CC} | Guaranteed Limit | | Unit |
|------------------|---|---|-----------------|------------------|-------|------|
| | | | | –40°C to 25°C | <85°C | |
| V _{IH} | Minimum High-Level Input Voltage, Select Inputs | | 1.8 | 1.2 | 1.2 | V |
| | | | 2.5 | 1.7 | 1.7 | |
| | | | 3.6 | 2.2 | 2.2 | |
| | | | 4.3 | 2.6 | 2.6 | |
| V _{IL} | Maximum Low-Level Input Voltage, Select Inputs | | 1.8 | 0.4 | 0.4 | V |
| | | | 2.5 | 0.5 | 0.5 | |
| | | | 3.6 | 0.7 | 0.7 | |
| | | | 4.3 | 0.9 | 0.9 | |
| I _{IN} | Maximum Input Leakage Current, Select Inputs | V _{IN} = V _{CC} or GND | 4.3 | ±0.1 | ±1.0 | μA |
| I _{OFF} | Power Off Leakage Current | V _{IN} = V _{CC} or GND | 0 | ±0.5 | ±2.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current (Note 2) | Select and V _{IS} = V _{CC} or GND | 1.65 to 4.5 | ±1.0 | ±2.0 | μA |

DC ELECTRICAL CHARACTERISTICS – Analog Section

| Symbol | Parameter | Condition | V _{CC} | Guaranteed Maximum Limit | | | | Unit |
|--|--|--|-----------------|--------------------------|------|-------|------|------|
| | | | | –40°C to 25°C | | <85°C | | |
| | | | | Min | Max | Min | Max | |
| R _{ON} | NC/NO On-Resistance (Note 2) | V _{IN} ≤ V _{IL} or V _{IN} ≥ V _{IH} V _{IS} = GND to V _{CC} I _{IN} ≤ 100 mA | 2.5 | | 0.65 | | 0.75 | Ω |
| | | | 3.0 | | 0.6 | | 0.75 | |
| | | | 4.3 | | 0.55 | | 0.70 | |
| R _{FLAT} | NC/NO On-Resistance Flatness (Notes 2, 4) | I _{COM} = 100 mA V _{IS} = 0 to V _{CC} | 2.5 | | 0.15 | | 0.15 | Ω |
| | | | 3.0 | | 0.15 | | 0.15 | |
| | | | 4.3 | | 0.15 | | 0.15 | |
| ΔR _{ON} | On-Resistance Match Between Channels (Notes 2 and 3) | V _{IS} = 1.3 V; I _{COM} = 100 mA V _{IS} = 1.5 V; I _{COM} = 100 mA V _{IS} = 2.2 V; I _{COM} = 100 mA | 2.5 | | 0.06 | | 0.06 | Ω |
| | | | 3.0 | | 0.05 | | 0.05 | |
| | | | 4.3 | | 0.05 | | 0.05 | |
| I _{NC(OFF)} I _{NO(OFF)} | NC or NO Off Leakage Current (Note 2) | V _{IN} = V _{IL} or V _{IH} V _{NO} or V _{NC} = 0.3 V V _{COM} = 4.0 V | 4.3 | –10 | 10 | –100 | 100 | nA |
| I _{COM(ON)} | COM ON Leakage Current (Note 2) | V _{IN} = V _{IL} or V _{IH} V _{NO} 0.3 V or 4.0 V with V _{NC} floating or V _{NC} 0.3 V or 4.0 V with V _{NO} floating V _{COM} = 0.3 V or 4.0 V | 4.3 | –10 | 10 | –100 | 100 | nA |

2. Guaranteed by design. Resistance measurements do not include test circuit or package resistance.

3. ΔR_{ON} = R_{ON(MAX)} – R_{ON(MIN)} between nS1 or nS2.

4. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

| Symbol | Parameter | Test Conditions | V_{CC} (V) | V_{IS} (V) | Guaranteed Maximum Limit | | | | | Unit |
|-----------|--------------------------------|---|-----------------|-----------------|--------------------------|------|-----|-------|-----|------|
| | | | | | -40°C to 25°C | | | <85°C | | |
| | | | | | Min | Typ* | Max | Min | Max | |
| t_{ON} | Turn-On Time | $R_L = 50 \Omega$, $C_L = 35$ pF (Figures 3 and 4) | 2.3 – 4.5 | 1.5 | | | 50 | | 60 | ns |
| t_{OFF} | Turn-Off Time | $R_L = 50 \Omega$, $C_L = 35$ pF (Figures 3 and 4) | 2.3 – 4.5 | 1.5 | | | 30 | | 40 | ns |
| t_{BBM} | Minimum Break-Before-Make Time | $V_{IS} = 3.0$ $R_L = 50 \Omega$, $C_L = 35$ pF (Figure 2) | 3.0 | 1.5 | 2 | 15 | | | | ns |

| | | Typical @ 25, $V_{CC} = 4.5$ V | | |
|----------|---|--------------------------------|--|----|
| C_{IN} | Control Pin Input Capacitance | 7.0 | | pF |
| C_{SN} | SN Port Capacitance | 72 | | pF |
| C_D | D Port Capacitance When Switch is Enabled | 230 | | pF |

*Typical Characteristics are at 25°C.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

| Symbol | Parameter | Condition | V_{CC} (V) | 25°C | Unit |
|-----------|---|---|-----------------|---------|------|
| | | | | Typical | |
| BW | Maximum On-Channel -3dB Bandwidth or Minimum Frequency Response (Figure 12) | V_{IN} centered between V_{CC} and GND (Figure 5) | 1.65 – 4.5 | 20 | MHz |
| V_{ONL} | Maximum Feed-through On Loss | $V_{IN} = 0$ dBm @ 100 kHz to 50 MHz V_{IN} centered between V_{CC} and GND (Figure 5) | 1.65 – 4.5 | -0.06 | dB |
| V_{ISO} | Off-Channel Isolation (Figure 13) | $f = 100$ kHz; $V_{IS} = 1$ V RMS; $C_L = 5$ pF V_{IN} centered between V_{CC} and GND (Figure 5) | 1.65 – 4.5 | -62 | dB |
| Q | Charge Injection Select Input to Common I/O (Figure 8) | $V_{IN} = V_{CC}$ to GND, $R_{IS} = 0 \Omega$, $C_L = 1$ nF $Q = C_L \times \Delta V_{OUT}$ (Figure 6) | 1.65 – 4.5 | 50 | pC |
| THD | Total Harmonic Distortion THD + Noise (Figure 7) | $F_{IS} = 20$ Hz to 20 kHz, $R_L = R_{gen} = 600 \Omega$, $C_L = 50$ pF $V_{IS} = 2$ V _{PP} | 4.5 | 0.01 | % |
| VCT | Channel-to-Channel Crosstalk | $f = 100$ kHz; $V_{IS} = 1$ V RMS, $C_L = 5$ pF, $R_L = 50 \Omega$ V_{IN} centered between V_{CC} and GND (Figure 5) | 1.65 – 4.5 | -62 | dB |

5. Off-Channel Isolation = $20 \log_{10} (V_{com}/V_{no})$, V_{com} = output, V_{no} = input to off switch.

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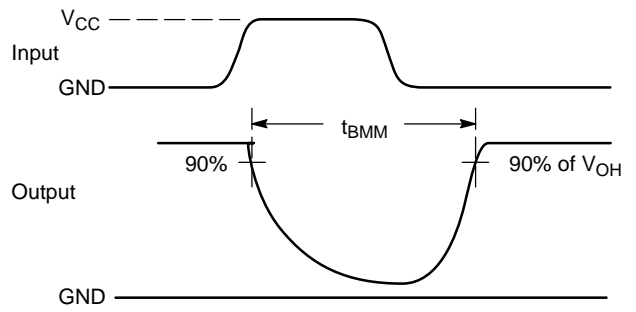
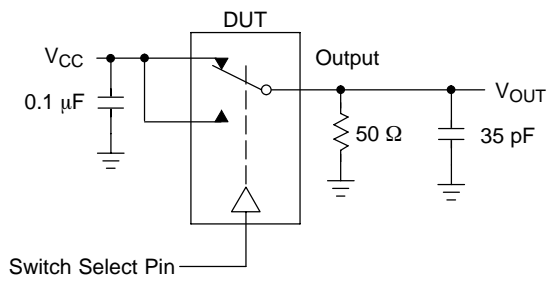


Figure 2. t_{BMM} (Time Break-Before-Make)

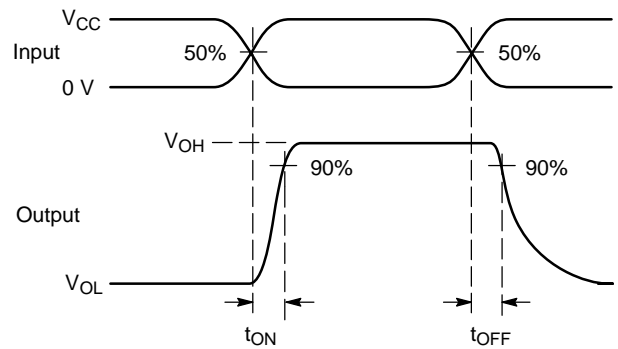
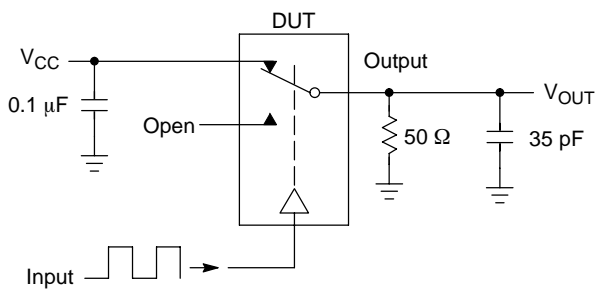


Figure 3. t_{ON}/t_{OFF}

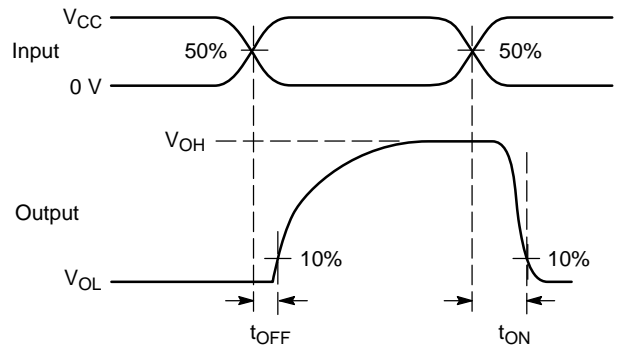
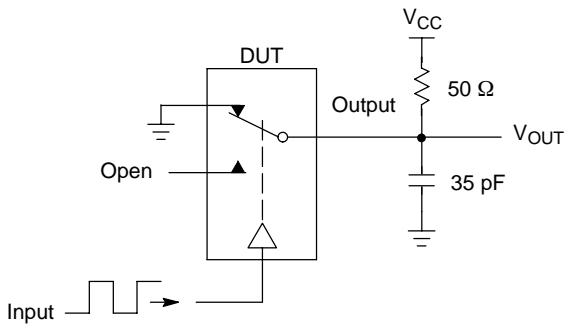
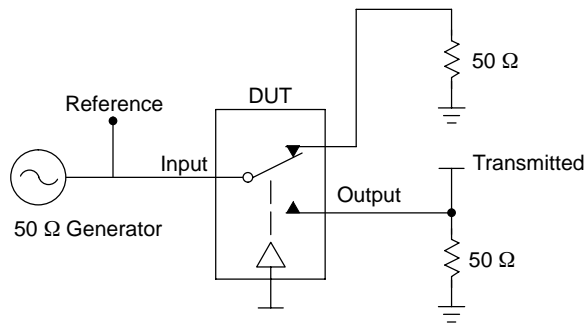


Figure 4. t_{ON}/t_{OFF}

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Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO} , Bandwidth and V_{ONL} are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 5. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ V_{ONL}

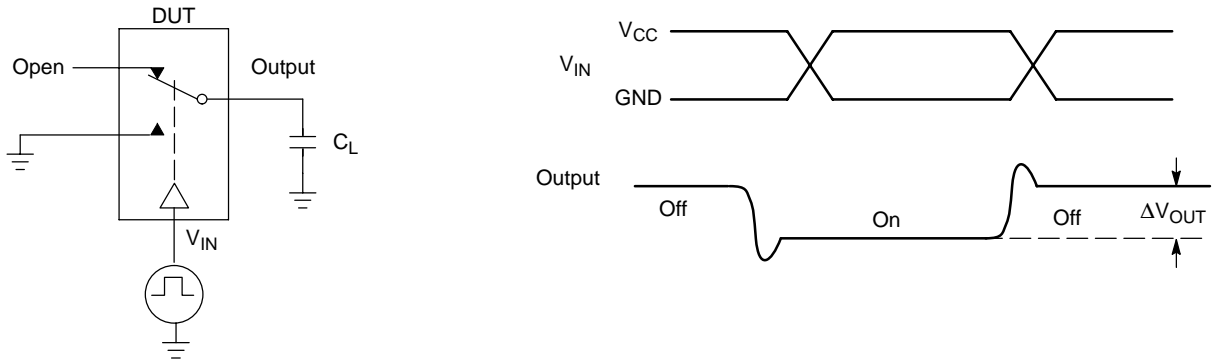


Figure 6. Charge Injection: (Q)

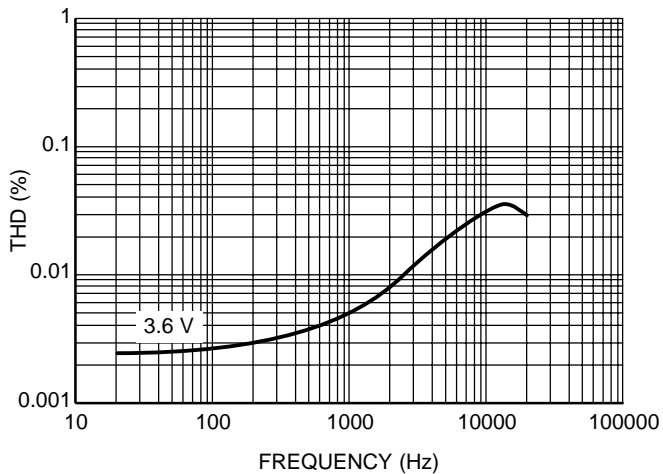


Figure 7. Total Harmonic Distortion Plus Noise Versus Frequency

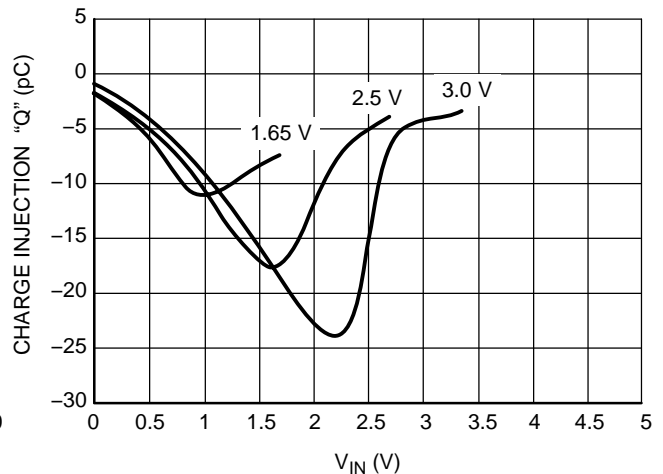


Figure 8. Charge Injection versus V_{is}

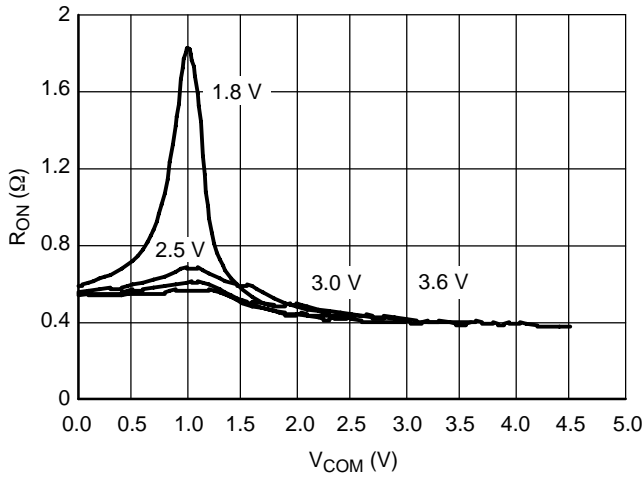


Figure 9. On-Resistance vs. COM Voltage

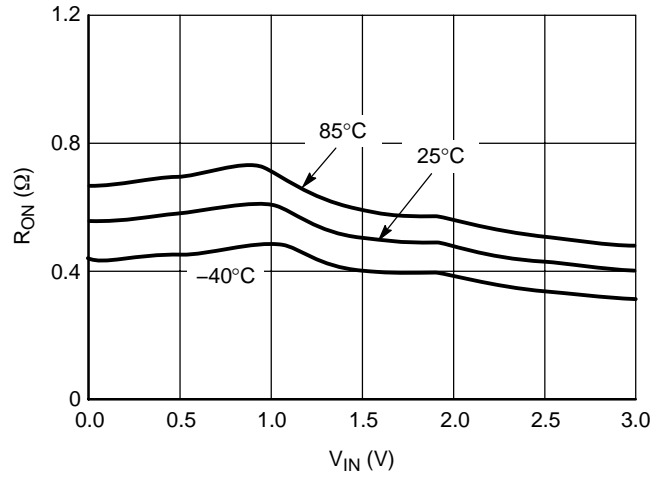


Figure 10. R_{ON} vs. V_{IN} vs. Temperature @ $V_{CC} = 3.0$ V

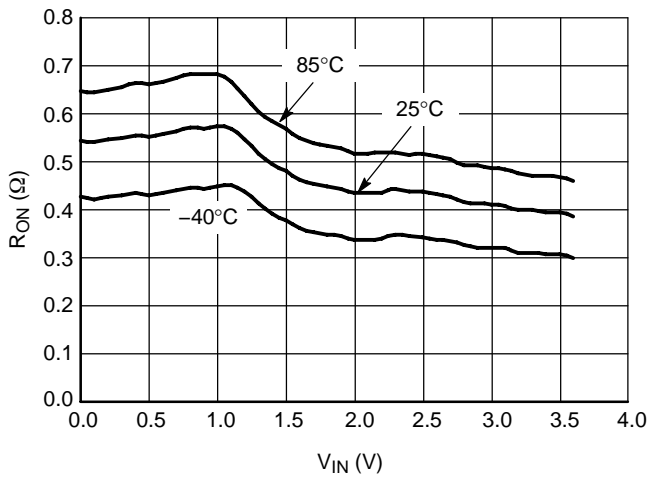


Figure 11. R_{ON} vs. V_{IN} vs. Temperature @ $V_{CC} = 3.6$ V

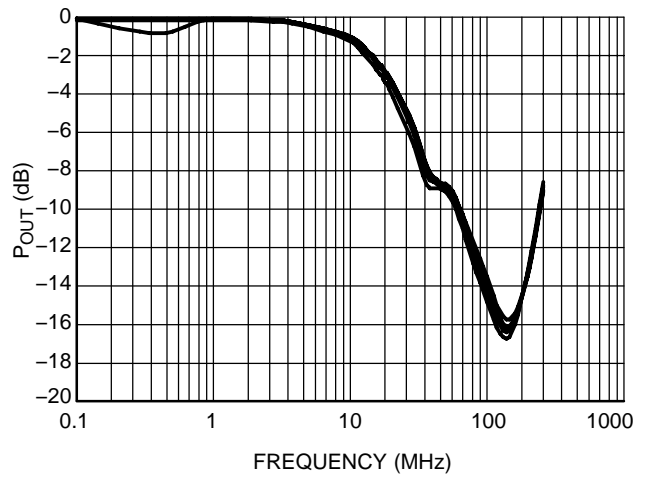


Figure 12. Bandwidth vs. Frequency @ $V_{CC} = 1.65$ V to 3.6 V

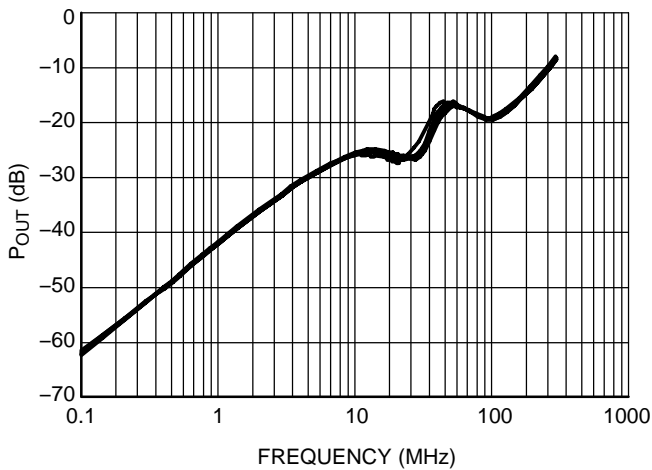


Figure 13. Off-Isolation vs. Frequency @ $V_{CC} = 1.65$ V to 3.6 V

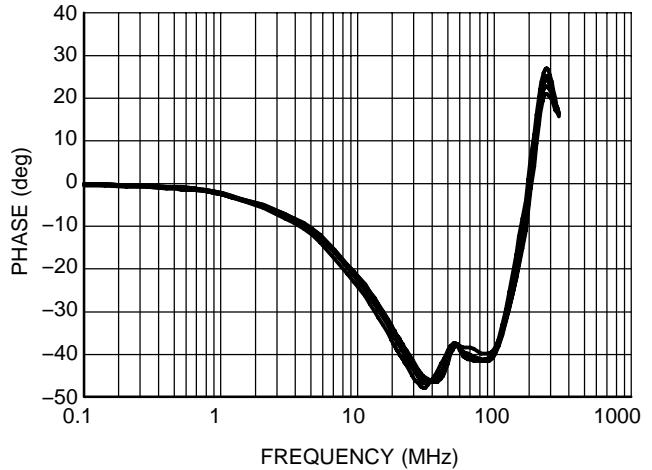


Figure 14. Phase Angle vs. Frequency @ $V_{CC} = 1.65$ V to 3.6 V

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DEVICE ORDERING INFORMATION

| Device Order Number | Device Nomenclature | | | | | Package Type | Tape & Reel Size† |
|---------------------|---------------------|------------|-----------------|----------------|--------------------|------------------|-------------------|
| | Circuit Indicator | Technology | Device Function | Package Suffix | Tape & Reel Suffix | | |
| NLAS3699BMN1R2G | NL | AS | 3699B | MN1 | R2G | QFN (Pb-Free) | 3000 Unit / Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

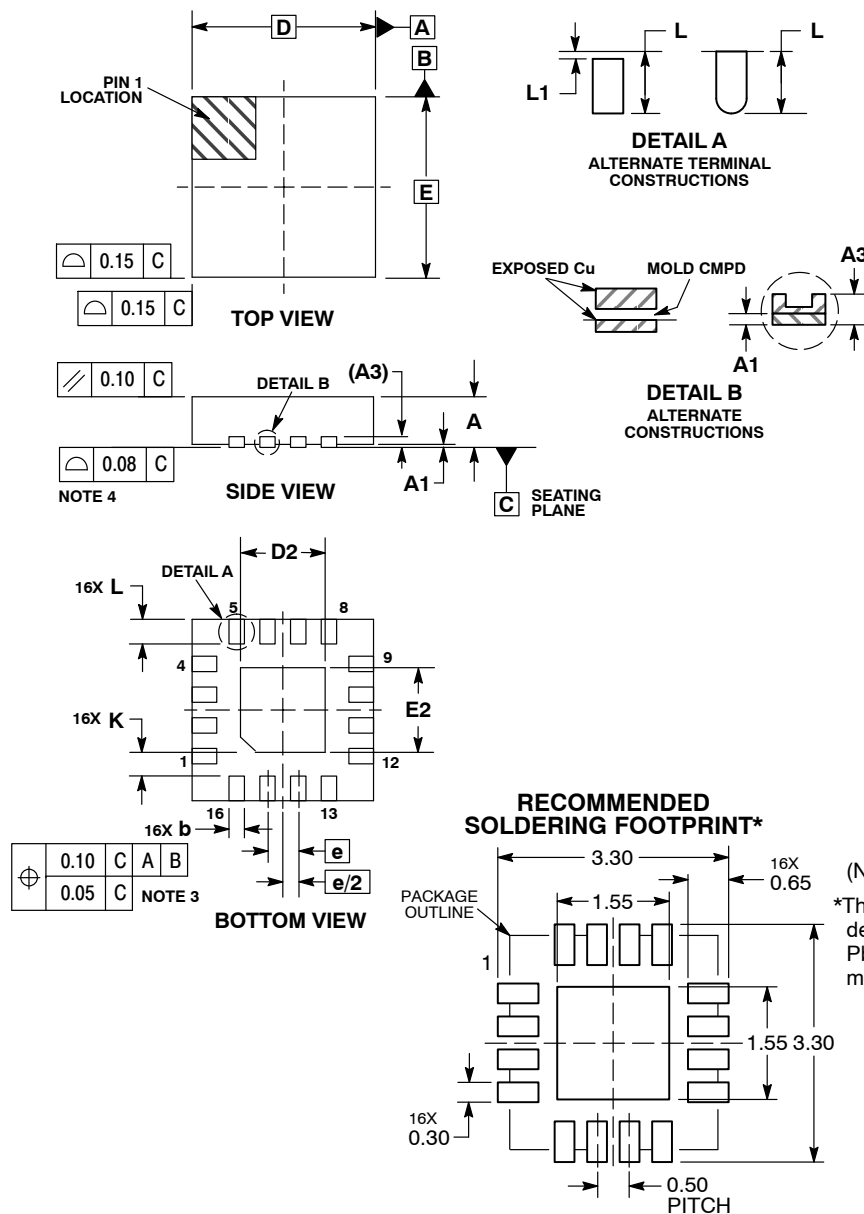
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1
SCALE 2:1

QFN16 3x3, 0.5P
CASE 485AE
ISSUE C

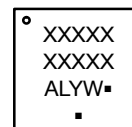
DATE 24 JUN 2016



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
 4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
 5. OUTLINE MEETS JEDEC DIMENSIONS PER MO-220, VARIATION VEED-6.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 | REF |
| b | 0.18 | 0.30 |
| D | 3.00 | BSC |
| D2 | 1.25 | 1.55 |
| E | 3.00 | BSC |
| E2 | 1.25 | 1.55 |
| e | 0.50 | BSC |
| K | 0.20 | --- |
| L | 0.30 | 0.50 |
| L1 | 0.00 | 0.15 |

GENERIC MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
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| DESCRIPTION: | QFN16 3X3, 0.5P | PAGE 1 OF 1 |

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