Data Sheet

1.5MHz, 2.5A, Step-down DC-DC Converter AUR9718B

General Description

The AUR9718B is a high efficiency step-down DC-DC voltage converter. The chip operation is optimized by peak-current mode architecture with built-in synchronous power MOSFET switchers.

The oscillator and timing capacitors are all built-in providing an internal switching frequency of 1.5MHz that allows the use of small surface mount inductors and capacitors for portable product implementations. Additional features including Soft Start (SS), Under Voltage Lock Out (UVLO), Thermal Shutdown Detection (TSD) and short circuit protection are integrated to provide reliable product applications.

The device is available in adjustable output voltage versions ranging from 0.8V to V_{IN} when input voltage range is from 2.7V to 5.5V, and is able to deliver up to 2.5A.

The AUR9718B is available in DFN-3×3-6 package.

Features

- High Efficiency Buck Power Converter
- Low $R_{DS(ON)}$ Internal Switches : 100mΩ
- Output Current: 2.5A
- Adjustable Output Voltage from 0.8V to V_{IN}
- Wide Operating Voltage Range: 2.7V to 5.5V
- Built-in Power Switchers for Synchronous Rectification with High Efficiency
- Feedback Voltage Allows Output: 800mV
- 1.5MHz Switching Frequency
- Thermal Shutdown Protection
- Low Drop-out Operation at 100% Duty Cycle
- No Schottky Diode Required
- Input Over Voltage Protection

Applications

- LCD TV
- Set Top Box
- Post DC-DC Voltage Regulation
- PDA and Notebook Computer

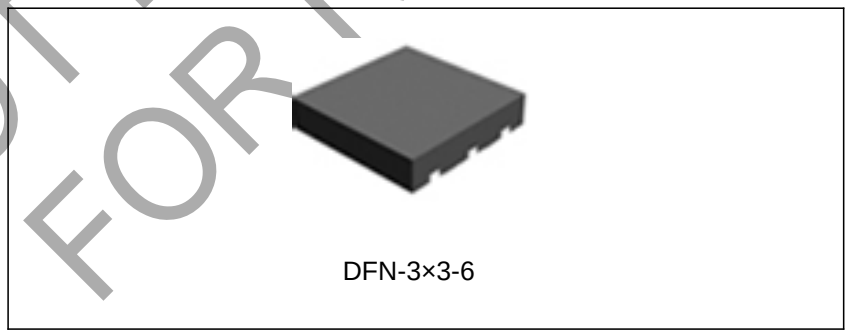


Figure 1. Package Type of AUR9718B

Pin Configuration

D Package
(DFN-3×3-6)

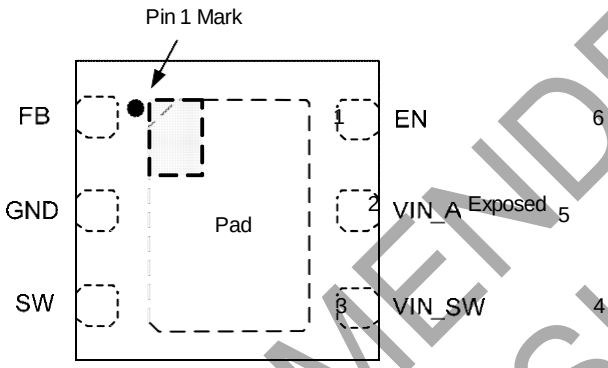


Figure 2. Pin Configuration of AUR9718B (Top View)

Pin Description

Pin Number	Pin Name	Function
1	FB	Output voltage feedback pin
2	GND	Ground pin
3	SW	Switch output pin
4	VIN_SW	Power supply input for the MOSFET switch
5	VIN_A	Supply input for the analog circuit
6	EN	Enable pin, active high

1.5MHz, 2.5A, Step-down DC-DC Converter AUR9718B

Functional Block Diagram

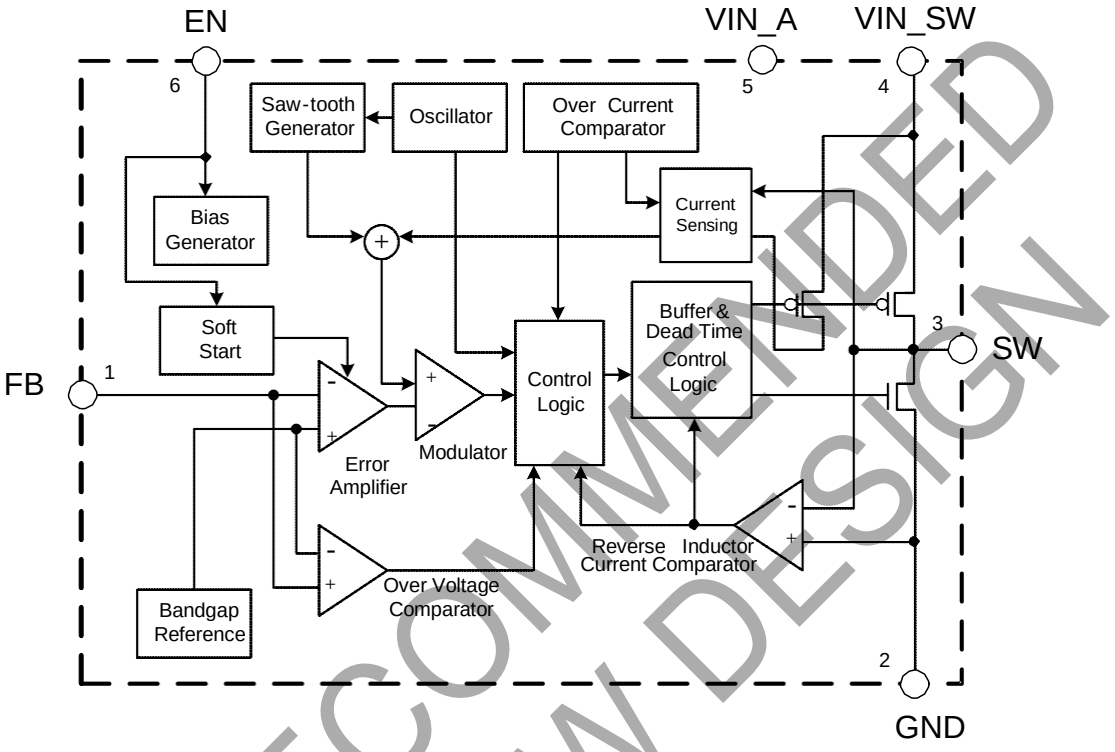


Figure 3. Functional Block Diagram of AUR9718B

Ordering Information

AUR9718B □ □

Circuit Type

Package
D: DFN-3×3-6
G: Green

Package	Temperature Range	Part Number	Marking ID	Packing Type
DFN-3×3-6	-40 to 80℃	AUR9718BGD	9718B	Tape & Reel

BCD Semiconductor's Pb-free products, as designated with "G" in the part number, are RoHS compliant and green.

Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Value	Unit
Supply Input Voltage (pin VIN_SW)	V_{IN_SW}	0 to 6.5	V
Supply Input Voltage (pin VIN_A)	V_{IN_A}	0 to 6.5	V
SW Pin Switch Voltage	V_{SW}	-0.3 to V_{IN_SW}+0.3	V
Enable Voltage	V_{EN}	-0.3 to V_{IN_A}+0.3	V
SW Pin Switch Current	I_{SW}	3.5	A
Power Dissipation (On PCB, T_A=25℃)	P_D	2.49	W
Thermal Resistance (Junction to Ambient, Simulation)	θ_{JA}	40.11	℃/W
Operating Junction Temperature	T_J	150	℃
Operating Temperature	T_{OP}	-40 to 85	℃
Storage Temperature	T_{STG}	-55 to 150	℃
ESD (Human Body Model)	V_{HBM}	2000	V
ESD (Machine Model)	V_{MM}	200	V

Note 1: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Input Voltage	V_{IN}	2.7	5.5	V
Junction Temperature Range	T_J	-40	125	℃
Ambient Temperature Range	T_A	-40	80	℃

Electrical Characteristics

V_{IN_SW}=V_{IN_A}=V_{EN}=5V, V_{OUT}=1.2V, V_{FB}=0.8V, L=3.3μH, C_{IN}=4.7μF, C_{OUT}=22μF, T_A=25℃, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.7		5.5	V
Shutdown Current	I_{OFF}	V_{EN}=0V			1	μA
Active Current	I_{ON}	V_{FB}=0.95V		310		μA
Regulated Feedback Voltage	V_{FB}	For Adjustable Output Voltage	0.784	0.8	0.816	V
Regulated Output Voltage Accuracy	$\Delta V_{OUT}/V_{OUT}$	V_{IN}=2.7V to 5.5V, I_{OUT}=10mA to 2.5A	-3		3	%
Peak Inductor Current	I_{PK}		3.0	3.5		A
Oscillator Frequency	f_{OSC}		1.2	1.5	1.8	MHz
PMOSFET R_{ON}	$R_{ON(P)}$	I_{SW}=0.75A		100		mΩ
NMOSFET R_{ON}	$R_{ON(N)}$	I_{SW}=0.75A		100		mΩ
EN High-level Input Voltage	V_{EN_H}		1.5			V
EN Low-level Input Voltage	V_{EN_L}				0.4	V
EN Input Current	I_{EN}				1	μA
Soft-start time	t_{SS}			400		μS
Maximum Duty Cycle	D_{MAX}		100			%
Under Voltage Lock Out	V_{UVLO}	Rising		2.4		V
		Falling		2.3		
Hysteresis		Hysteresis		0.1		V
OVP Threshold	V_{OVP}		5.8	5.9	6.0	V
Hysteresis on OVP			300	400	500	mV
Thermal Shutdown	T_{SD}	Hysteresis=30℃		150		℃

Typical Performance Characteristics

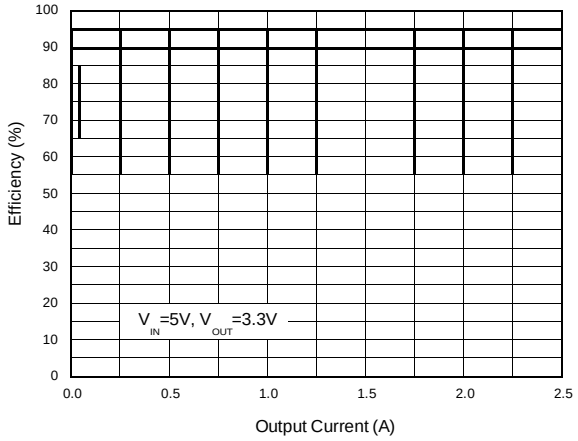


Figure 4. Efficiency vs. Output Current

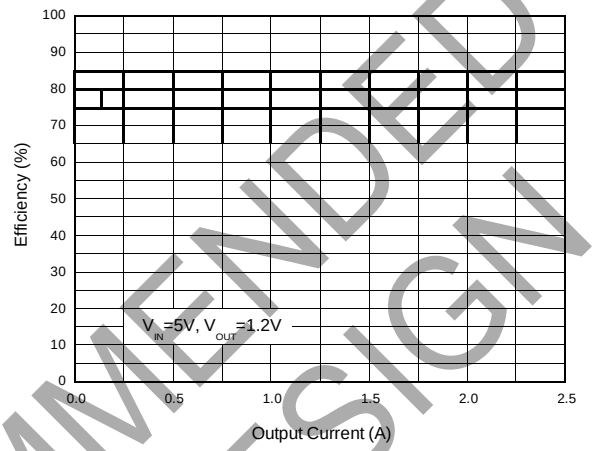


Figure 5. Efficiency vs. Output Current

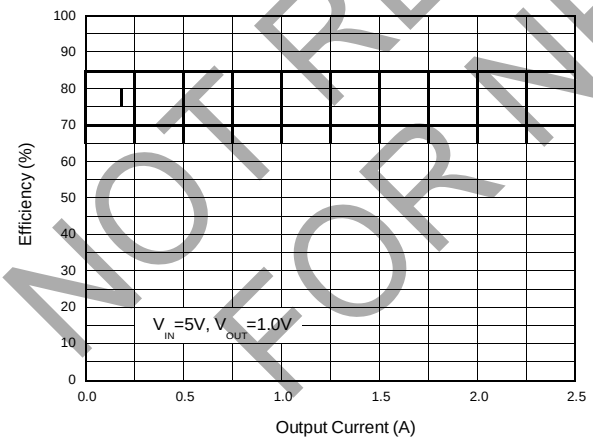


Figure 6. Efficiency vs. Output Current

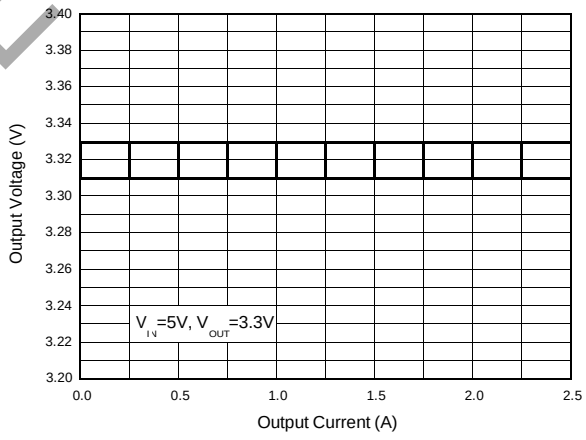


Figure 7. 3.3V Load Regulation

Typical Performance Characteristics (Continued)

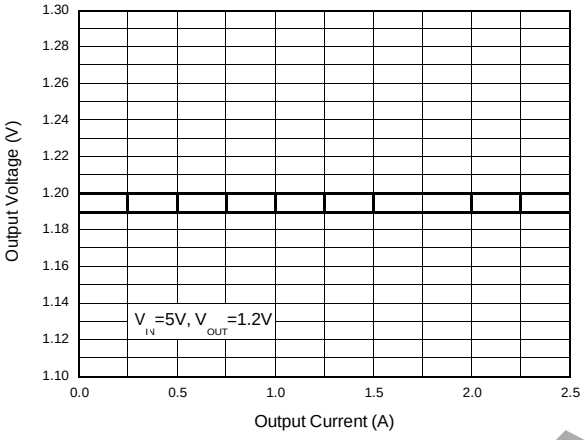


Figure 8. 1.2V Load Regulation

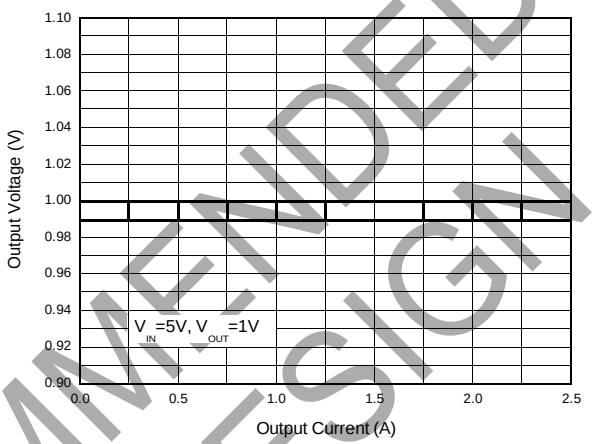


Figure 9. 1.0V Load Regulation

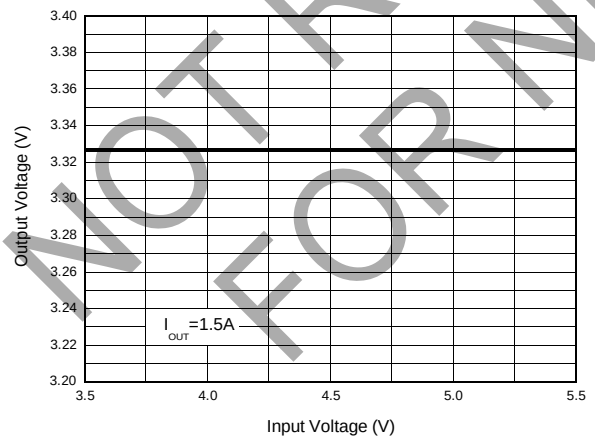


Figure 10. 3.3V Line Regulation

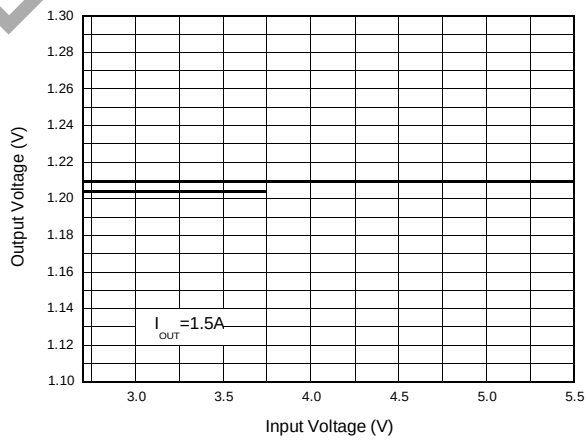


Figure 11. 1.2V Line Regulation

Typical Performance Characteristics (Continued)

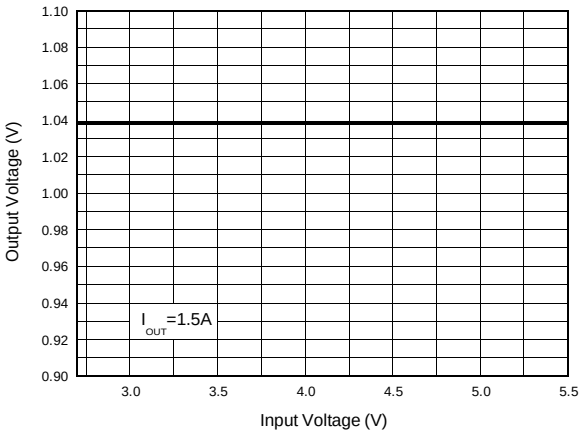


Figure 12. 1.0V Line Regulation

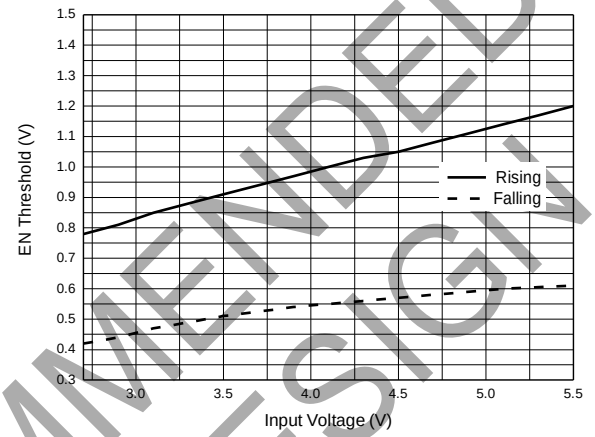


Figure 13. EN Threshold vs. Input Voltage

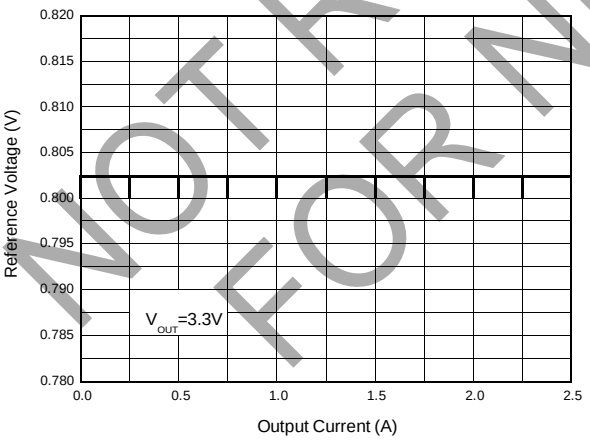


Figure 14. Reference Voltage vs. Output Current

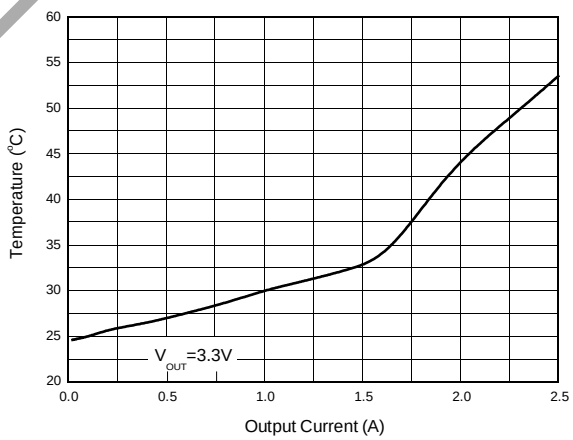


Figure 15. Temperature vs. Output Current

Typical Performance Characteristics (Continued)

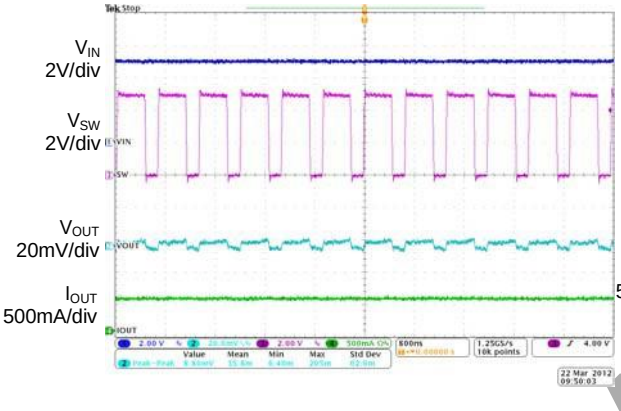


Figure 16. V_{OUT} Ripple
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=500mA)

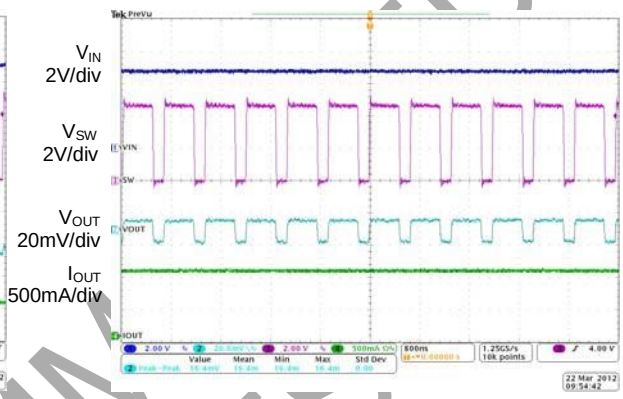


Figure 17. V_{OUT} Ripple
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=1000mA)

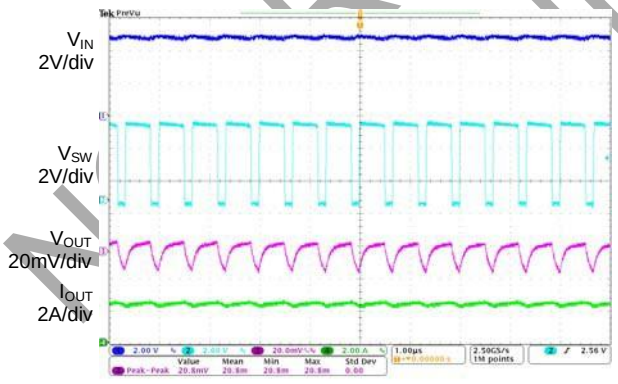


Figure 18. V_{OUT} Ripple
(I_{OUT}=2500mA)

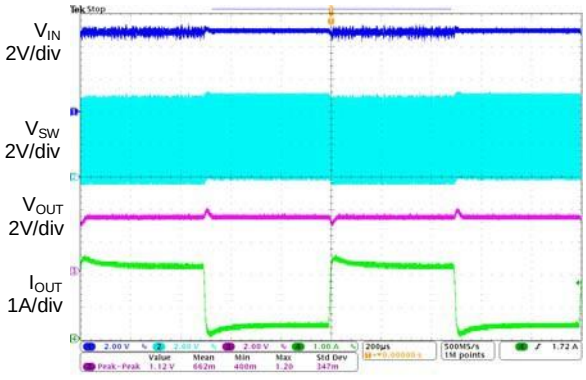


Figure 19. Dynamic Mode
(I_{OUT}=500mA to 2500mA)

Typical Performance Characteristics (Continued)

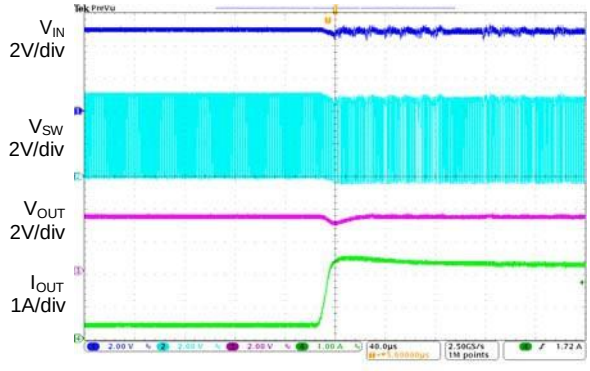


Figure 20. Dynamic Mode (Rising)

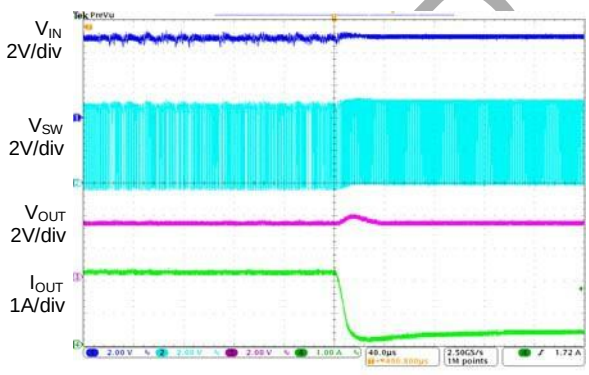


Figure 21. Dynamic Mode (Falling)

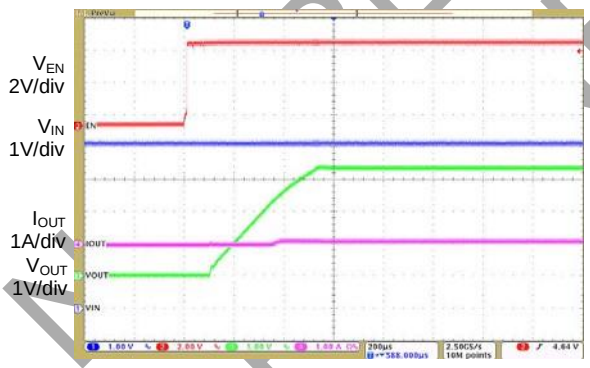


Figure 22. EN Pin L to H
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=100mA)

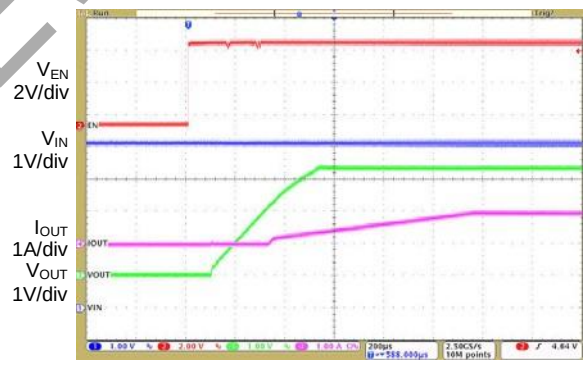


Figure 23. EN Pin L to H
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=1000mA)

Typical Performance Characteristics (Continued)

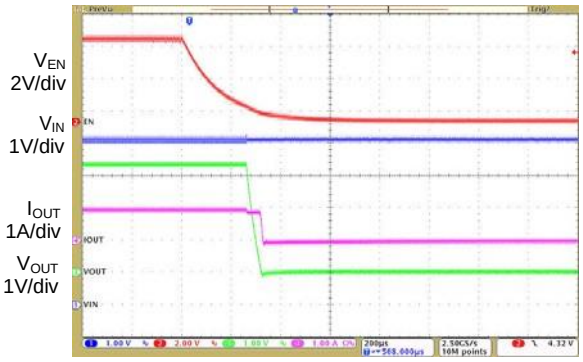


Figure 24. EN Pin H to L
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=1A)

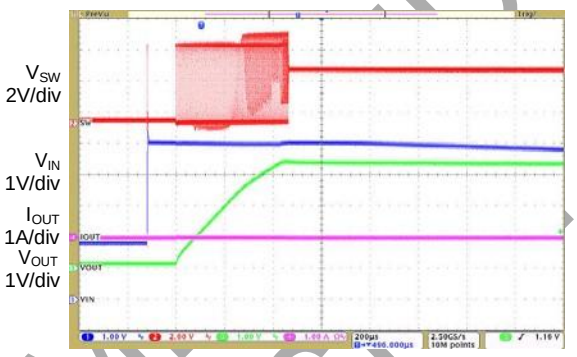


Figure 25. Soft Start Function
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0A)

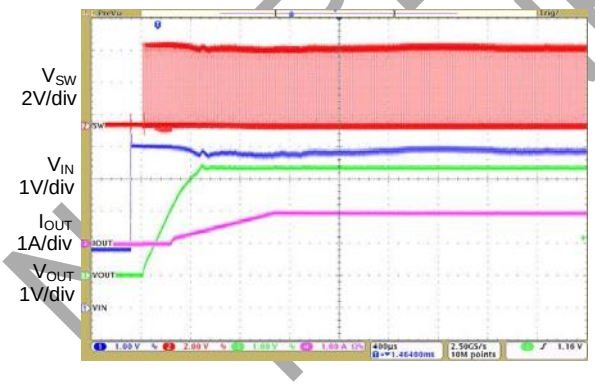


Figure 26. Soft Start Function
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=1A)

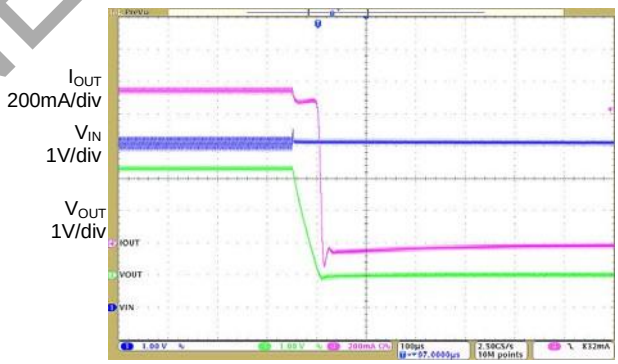


Figure 27. OTP Function

Typical Performance Characteristics (Continued)

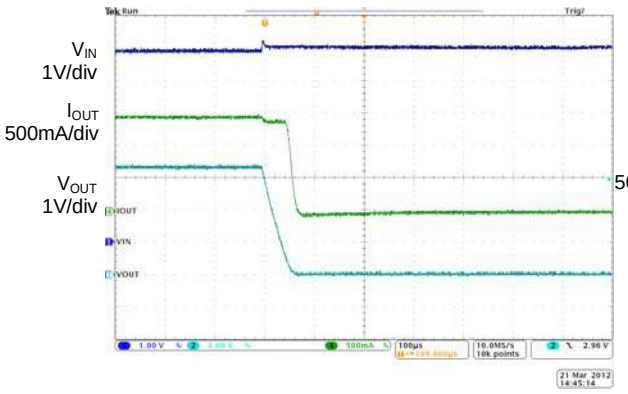


Figure 28. OVP Function
(V_{IN}=5V to 6V)

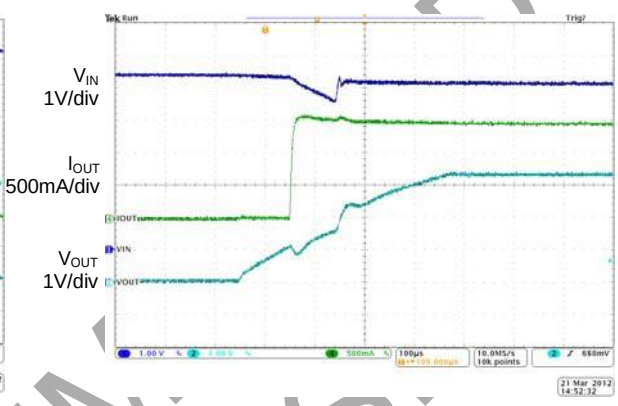


Figure 29. Leave OVP Function
(V_{IN}=6V to 5V)

Application Information

The basic AUR9718B application circuit is shown in Figure 34.

1. Inductor Selection

For most applications, the value of inductor is chosen based on the required ripple current with the range of 1.0μH to 6.8μH.

$$\Delta I_L = \frac{1}{f \times L} V_{OUT}(1 - \frac{V_{OUT}}{V_{IN}})$$

The largest ripple current occurs at the highest input voltage. Having a small ripple current reduces the ESR loss in the output capacitor and improves the efficiency. The highest efficiency is realized at low operating frequency with small ripple current. However, larger value inductors will be required. A reasonable starting point for ripple current setting is $\triangle I_L$=40%I_{MAX} . For a maximum ripple current stays below a specified value, the inductor should be chosen according to the following equation:

$$L = [\frac{V_{OUT}}{f \times \Delta I_L(MAX)}][1 - \frac{V_{OUT}}{V_{IN}(MAX)}]$$

The DC current rating of the inductor should be at least equal to the maximum output current plus half the highest ripple current to prevent inductor core saturation. For better efficiency, a lower DC-resistance inductor should be selected.

2. Capacitor Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} = I_{OMAX} \times \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{\frac{1}{2}}}{V_{IN}}$$

It indicates a maximum value at V_{IN}=2V_{OUT}, where I_{RMS}=I_{OUT}/2. This simple worse-case condition is commonly used for design because even significant deviations do not much relieve. The selection of C_{OUT} is determined by the Effective Series Resistance (ESR) that is required to minimize output voltage ripple and load step transients, as well as the amount of bulk capacitor that is necessary to ensure that the control loop is stable. The output ripple, $\triangle V_{OUT}$, is determined by:

$$\Delta V_{OUT} \le \Delta I_L [ESR + \frac{1}{8 \times f \times C_{OUT}}]$$

The output ripple is the highest at the maximum input voltage since $\triangle I_L$ increases with input voltage.

3. Load Transient

A switching regulator typically takes several cycles to respond to the load current step. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\triangle I_{LOAD}$×ESR, where ESR is the effective series resistance of output capacitor. $\triangle I_{LOAD}$ also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During the recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

4. Output Voltage Setting

The output voltage of AUR9718B can be adjusted by a resistive divider according to the following formula:

$$V_{OUT} = V_{REF} \times (1 + \frac{R_1}{R_2}) = 0.8V \times (1 + \frac{R_1}{R_2})$$

The resistive divider senses the fraction of the output voltage as shown in Figure 30.

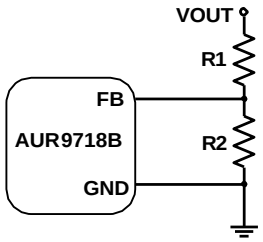


Figure 30. Setting the Output Voltage

Application Information (Continued)

5. Short Circuit Protection

When AUR9718B output node is shorted to GND, as V_{FB} drops under 0.4V, the chip will enter soft-start to protect itself; when short circuit is removed, and V_{FB} rises over 0.4V, the chip will enter normal operation again. If AUR9718B reaches OCP threshold while short circuit, it will enter soft-start cycle and last until the current drops under OCP threshold.

6. Efficiency Considerations

The efficiency of switching regulator is equal to the output power divided by the input power times 100%. It is usually useful to analyze the individual losses to determine what is limiting efficiency and which change could produce the largest improvement. Efficiency can be expressed as:

Efficiency=100%-L1-L2-…..

Where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the regulator produce losses, two major sources usually account for most of the power losses: V_{IN} quiescent current and I^2R losses. The V_{IN} quiescent current loss dominates the efficiency loss at very light load currents and the I^2R loss dominates the efficiency loss at medium to heavy load currents.

6.1 The V_{IN} quiescent current loss comprises two parts: the DC bias current as given in the electrical characteristics and the internal MOSFET switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each cycle the gate is switched from high to low, then to high again, and the packet of charge, dQ moves from V_{IN} to ground. The resulting dQ/dt is the current out of V_{IN} that is typically larger than the internal DC bias current. In continuous mode,

$$I_{GATE} = f \times (Q_P + Q_N)$$

Where Q_P and Q_N are the gate charge of power PMOSFET and NMOSFET switches. Both the DC bias current and gate charge losses are proportional to the V_{IN} and this effect will be more serious at higher input voltages.

6.2 I^2R losses are calculated from internal switch resistance, R_{SW} and external inductor resistance R_L. In continuous mode, the average output current flowing through the inductor is chopped between power PMOSFET switch and NMOSFET switch. Then, the series resistance looking into the SW pin is a function of both PMOSFET $R_{DS(ON)P}$ and NMOSFET $R_{DS(ON)N}$ resistance and the duty cycle (D):

$$R_{SW} = R_{DS(ON)P} \times D + R_{DS(ON)N} \times (1 - D)$$

Therefore, to obtain the I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% of total additional loss.

7. Thermal Characteristics

In most applications, the part does not dissipate much heat due to its high efficiency. However, in some conditions when the part is operating in high ambient temperature with high $R_{DS(ON)}$ resistance and high duty cycles, such as in LDO mode, the heat dissipated may exceed the maximum junction temperature. To avoid the part from exceeding maximum junction temperature, the user should do some thermal analysis. The maximum power dissipation depends on the layout of PCB, the thermal resistance of IC package, the rate of surrounding airflow and the temperature difference between junction and ambient.

8. Input Over Voltage Protection

When the input voltage of AUR9718B exceeds V_{OVP}, the IC would enter the mode of Input Over Voltage Protection. It will be shutdown and there will be no output voltage. As the input voltage goes down below 5.5V, the IC would leave input OVP mode and the output voltage will be recovered.

9. PC Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to optimize the

Application Information (Continued)

performance of AUR9718B.

1. The power traces, including the GND trace, the SW trace and the VIN trace should be kept direct, short and wide.

2. Put the input capacitor as close as possible to the VIN_SW, VIN_A and GND pins.

3. The FB pin should be connected directly to the feedback resistor divider.

4. Keep the switching node SW away from the sensitive FB pin and the node should be kept small area.

The following is an example of 2-layer PCB layout as shown in Figure 32 and Figure 33 for reference.

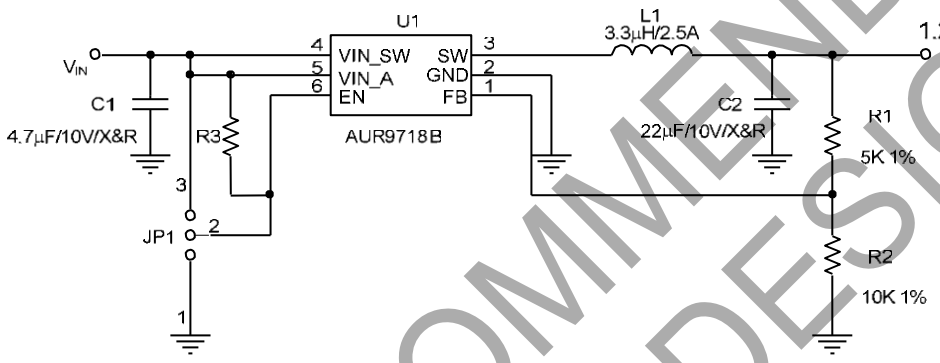


Figure 31. The Evaluation Board Schematic

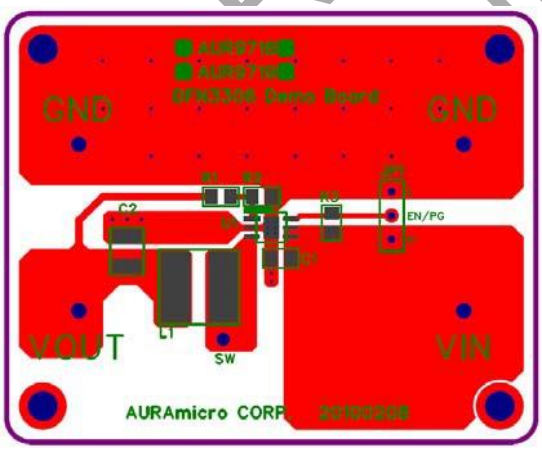


Figure 32. Top Layer for Demo Board

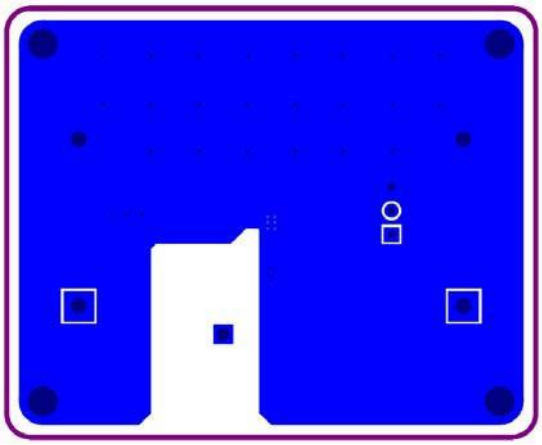
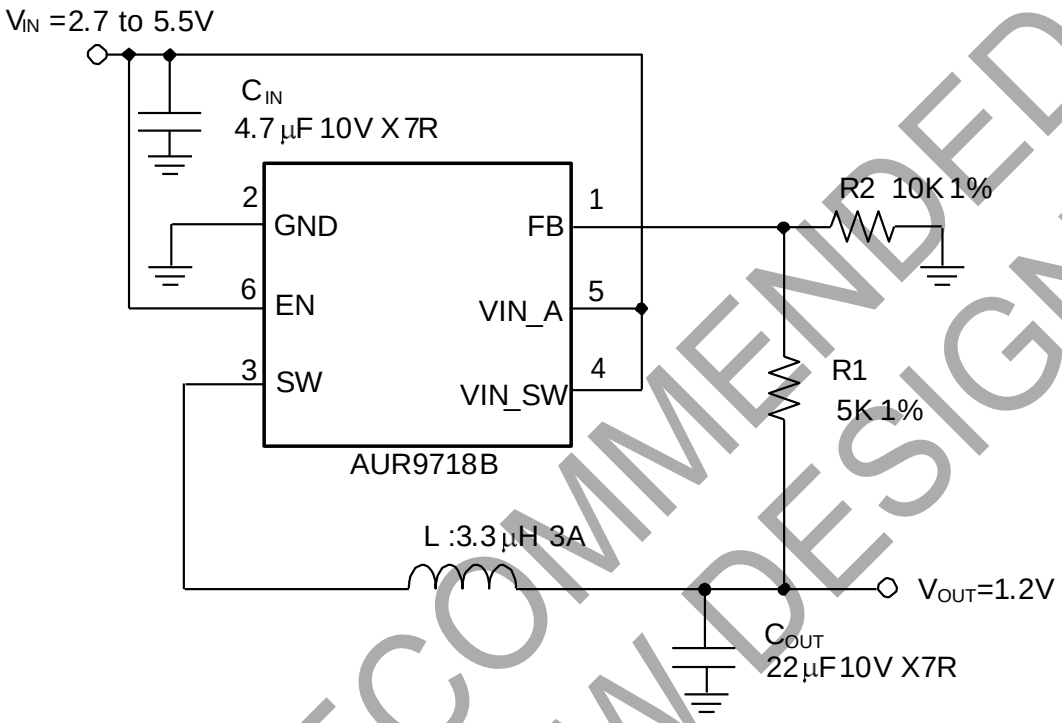


Figure 33. Bottom Layer for Demo Board

Typical Application



Note 2: $V_{OUT} = V_{FB} \times (1 + \frac{R_1}{R_2})$

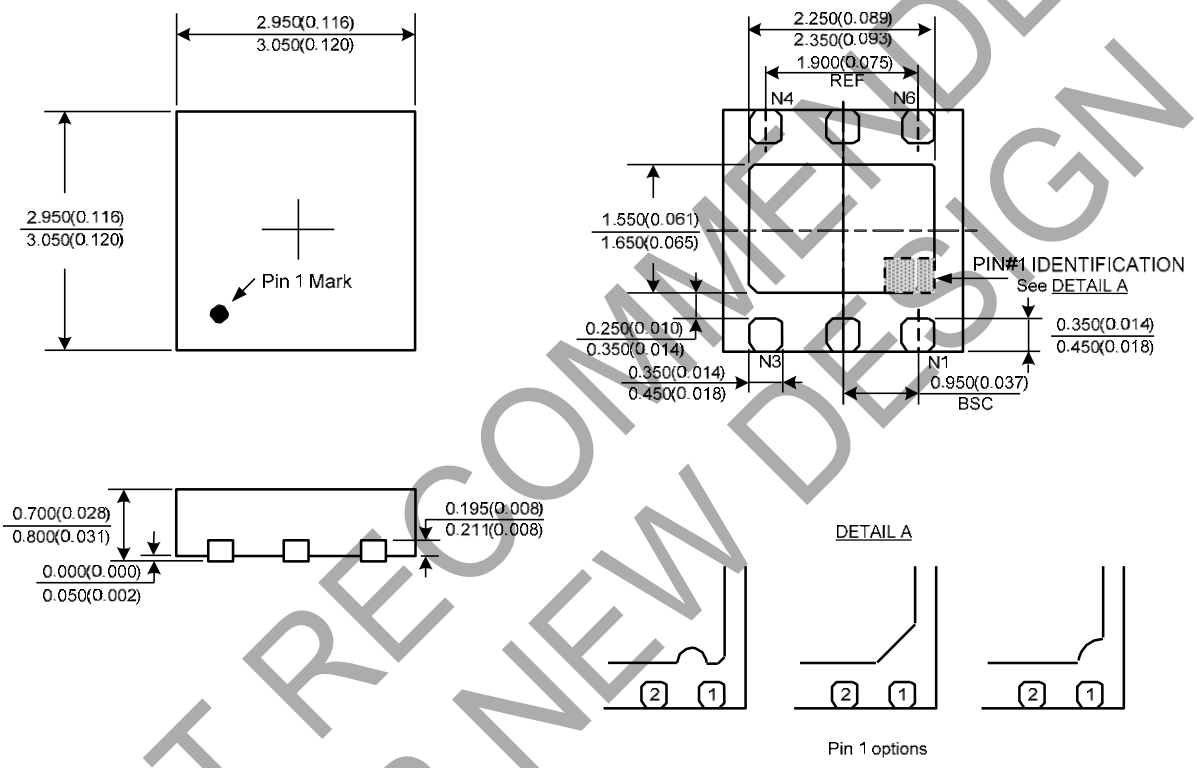
Figure 34. Typical Application Circuit of AUR9718B (Note 2)

Table 1. Component Guide

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)
3.3	31.25	10	3.3
2.5	21.5	10	3.3
1.8	12.5	10	3.3
1.2	5	10	3.3
1.0	3	10	3.3

Mechanical Dimensions

DFN-3×3-6 **Unit: mm(inch)**



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MAIN SITE

- Headquarters
BCD Semiconductor Manufacturing Limited
No. 1600, Zi Xing Road, Shanghai ZiZhu Science-based Industrial Park, 200241, China
Tel: +86-21-24162266, Fax: +86-21-24162277

- Wafer Fab
Shanghai SIM-BCD Semiconductor Manufacturing Co., Ltd.
800 Yi Shan Road, Shanghai 200233, China Tel:
+86-21-6485 1491, Fax: +86-21-5450 0008

REGIONAL SALES OFFICE

Shenzhen Office
Shanghai SIM-BCD Semiconductor Manufacturing Co., Ltd., Shenzhen Office
Unit A Room 1203, Skyworth Bldg., Gaoxin Ave.1.S., Nanshan District, Shenzhen, China
Tel: +86-755-8826 7951
Fax: +86-755-8826 7865

Taiwan Office
BCD Semiconductor (Taiwan) Company Limited
4F, 298-1, Rui Guang Road, Nei-Hu District, Taipei, Taiwan
Tel: +886-2-2656 2808
Fax: +886-2-2656 2806

USA Office
BCD Semiconductor Corp.
30920 Huntwood Ave. Hayward, CA 94544, USA
Tel : +1-510-324-2988
Fax: +1-510-324-2788