International
IOR Rectifier

# IR3081PBF

## DATA SHEET

## *XPHASE*™ VR 10 CONTROL IC

## DESCRIPTION

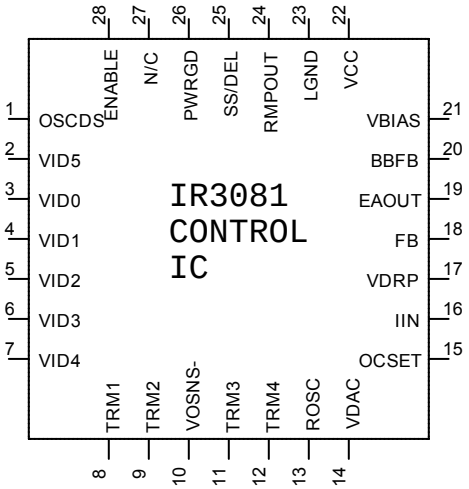
The IR3081PBF Control IC combined with an IR *XPhase*™ Phase IC provides a full featured and flexible way to implement a complete VR 10 power solution. The "Control" IC provides overall system control and interfaces with any number of "Phase ICs" which each drive and monitor a single phase of a multiphase converter. The *XPhase*™ architecture results in a power supply that is smaller, less expensive, and easier to design while providing higher efficiency than conventional approaches.

The IR3081PBF is intended for VRD or VRM/EVRD 10 applications that use external VCCVID/VTT circuits.

## FEATURES

- 6 bit VR 10 compatible VID with 0.5% overall system accuracy
- 1 to X phases operation with matching phase ICs
- Programmable Dynamic VID Slew Rate
- No Discharge of output capacitors during Dynamic VID step-down (can be disabled)
- +/-300mV Differential Remote Sense
- Programmable 150kHz to 1MHz oscillator
- Programmable VID Offset and Load Line output impedance
- Programmable Softstart
- Programmable Hiccup Over-Current Protection with Delay to prevent false triggering
- Simplified Powergood provides indication of proper operation and avoids false triggering
- Operates from 12V input with 9.1V Under-Voltage Lockout
- 6.8V/5mA Bias Regulator provides System Reference Voltage
- Enable Input
- Small thermally enhanced 28L MLPQ package

## PACKAGE PINOUT



## ORDERING INFORAMATION

| Device | Order Quantity |
|---|---|
| IR3081MPBFTR | 3000 per reel |
| IR3081MPBF | 100 piece strips |

## ABSOLUTE MAXIMUM RATINGS

Operating Junction Temperature……..150°C
Storage Temperature Range…….-65°C to 150°C
ESD Rating……HBM Class 1C JEDEC standard

| PIN # | PIN NAME | $V_{MAX}$ | $V_{MIN}$ | $I_{SOURCE}$ | $I_{SINK}$ |
|---|---|---|---|---|---|
| 1 | OSCDS | 20V | -0.3V | 1mA | 1mA |
| 2-7 | VID0-5 | 20V | -0.3V | 10mA | 10mA |
| 8, 9, 11,12 | TRM1-4 | Do Not Connect | Do Not Connect | Do Not Connect | Do Not Connect |
| 10 | VOSNS- | 0.5V | -0.5V | 10mA | 10mA |
| 13 | ROSC | 20V | -0.5V | 1mA | 1mA |
| 14 | VDAC | 20V | -0.3V | 1mA | 1mA |
| 15 | OCSET | 20V | -0.3V | 1mA | 1mA |
| 16 | IIN | 20V | -0.3V | 1mA | 1mA |
| 17 | VDRP | 20V | -0.3V | 5mA | 5mA |
| 18 | FB | 20V | -0.3V | 1mA | 1mA |
| 19 | EAOUT | 10V | -0.3V | 10mA | 20mA |
| 20 | BBFB | 20V | -0.3V | 1mA | 1mA |
| 21 | VBIAS | 20V | -0.3V | 1mA | 1mA |
| 22 | VCC | 20V | -0.3V | 1mA | 50mA |
| 23 | LGND | n/a | n/a | 50mA | 1mA |
| 24 | RMPOUT | 20V | -0.3V | 1mA | 1mA |
| 25 | SS/DEL | 20V | -0.3V | 1mA | 1mA |
| 26 | PWRGD | 20V | -0.3V | 1mA | 20mA |
| 27 | N/C | n/a | n/a | n/a | n/a |
| 28 | ENABLE | 20V | -0.3V | 1mA | 1mA |

## ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over: 9.5V ≤ $V_{CC}$ ≤ 14V, 0 °C ≤ $T_J$ ≤ 100 °C

| PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **VDAC Reference** | | | | | |
| System Set-Point Accuracy | -0.3V ≤ VOSNS- ≤ 0.3V, Connect FB to EAOUT, Measure V(EAOUT) – V(VOSNS-) deviation from Table 1. Applies to all VID codes. | | 0.5 | | % |
| Source Current | $R_{ROSC}$ = 41.9kΩ | 68 | 80 | 92 | μA |
| Sink Current | $R_{ROSC}$ = 41.9kΩ | 47 | 55 | 63 | μA |
| VID Input Threshold | | 500 | 600 | 700 | mV |
| VID Input Bias Current | 0V ≤ VID0-5 ≤ VCC | -5 | 0 | 5 | μA |
| Regulation Detect Comparator Input Offset | | -5 | 0 | 5 | mV |
| Regulation Detect to EAOUT Delay | | | 130 | 200 | ns |
| BBFB to FB Bias Current Ratio | | 0.95 | 1.00 | 1.05 | μA/μA |
| VID 11111x Blanking Delay | Measure Time till PWRGD drives low | | 800 | | ns |
| VID Step Down Detect Blanking Time | Measure from VID inputs to EAOUT | | 1.7 | | μs |
| VID Down BB Clamp Voltage | Percent of VDAC voltage | 70 | 75 | 80 | % |
| VID Down BB Clamp Current | | 3.5 | 6.2 | 12 | mA |
| **Error Amplifier** | | | | | |
| Input Offset Voltage | Connect FB to EAOUT, Measure V(EAOUT) – V(DAC). from Table 1. Applies to all VID codes and -0.3V ≤ VOSNS- ≤ 0.3V. Note 2 | -3 | 4 | 8 | mV |
| FB Bias Current | $R_{ROSC}$ = 41.9kΩ | -31 | -29.5 | -28 | μA |
| DC Gain | Note 1 | 90 | 100 | 105 | dB |
| Gain-Bandwidth Product | Note 1 | 4 | 7 | | MHz |
| Source Current | | 0.4 | 0.6 | 0.8 | mA |
| Sink Current | | 0.7 | 1.2 | 1.7 | mA |
| Max Voltage | VBIAS–VEAOUT (referenced to VBIAS) | 125 | 250 | 375 | mV |
| Min Voltage | Normal operation or Fault mode | 30 | 100 | 150 | mV |
| **VDRP Buffer Amplifier** | | | | | |
| Input Offset Voltage | V(VDRP) – V(IIN), 0.8V ≤ V(IIN) ≤ 5.5V | -8 | 0 | 8 | mV |
| Input Voltage Range | | 0.8 | | 5.5 | V |
| Bandwidth (-3dB) | Note 1 | 1 | 6 | | MHz |
| Slew Rate | | | 10 | | V/μs |
| IIN Bias Current | | -2.0 | -0.75 | 0 | μA |

| PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **Oscillator** | | | | | |
| Switching Frequency | $R_{ROSC}$ = 41.9kΩ | 255 | 300 | 345 | kHz |
| Peak Voltage (5V typical, measured as % of VBIAS) | $R_{ROSC}$ = 41.9kΩ | 70 | 71 | 74 | % |
| Valley Voltage (1V typical, measured as % of VBIAS) | $R_{ROSC}$ = 41.9kΩ | 11 | 14 | 16 | % |
| **VBIAS Regulator** | | | | | |
| Output Voltage | -5mA ≤ I(VBIAS) ≤ 0 | 6.5 | 6.8 | 7.1 | V |
| Current Limit | | -30 | -15 | -6 | mA |
| **Soft Start and Delay** | | | | | |
| SS/DEL to FB Input Offset Voltage | With FB = 0V, adjust V(SS/DEL) until EAOUT drives high | 0.85 | 1.3 | 1.5 | V |
| Charge Current | | 40 | 70 | 100 | μA |
| Discharge Current | | 4 | 6 | 9 | μA |
| Charge/Discharge Current Ratio | | 10 | 11.5 | 13 | μA/μA |
| Charge Voltage | | 3.7 | 4.0 | 4.2 | V |
| Delay Comparator Threshold | Relative to Charge Voltage | 70 | 90 | 110 | mV |
| Discharge Comparator Threshold | | 150 | 200 | 250 | mV |
| **Over-Current Comparator** | | | | | |
| Input Offset Voltage | 1V ≤ V(OCSET) ≤ 5V | -10 | 0 | 10 | mV |
| OCSET Bias Current | $R_{ROSC}$ = 41.9kΩ | -31 | -29.5 | -28 | μA |
| **PWRGD Output** | | | | | |
| Output Voltage | I(PWRGD) = 4mA | | 150 | 400 | mV |
| Leakage Current | V(PWRGD) = 5.5V | | 0 | 10 | μA |
| **Enable Input** | | | | | |
| Threshold voltage | | 500 | 600 | 700 | mV |
| Bias Current | 0V ≤ V(ENABLE) ≤ VCC | -5 | 0 | 5 | μA |
| **VCC Under-Voltage Lockout** | | | | | |
| Start Threshold | | 8.6 | 9.1 | 9.6 | V |
| Stop Threshold | | 8.4 | 8.9 | 9.4 | V |
| Hysteresis | Start – Stop | 150 | 200 | 300 | mV |
| **General** | | | | | |
| VCC Supply Current | | 8 | 11 | 14 | mA |
| VOSNS- Current | -0.3V ≤ VOSNS- ≤ 0.3V, All VID Codes | -5.5 | -4.5 | -3.5 | mA |

**Note 1:** Guaranteed by design, but not tested in production
**Note 2:** VDAC Output is trimmed to compensate for Error Amplifier input offsets errors

## PIN DESCRIPTION

| PIN# | PIN SYMBOL | PIN DESCRIPTION |
|---|---|---|
| 1 | OSCDS | Apply a voltage greater than VBIAS to disable the oscillator. Used during factory testing & trimming. Ground or leave open for normal operation. |
| 2-7 | VID0-5 | Inputs to VID D to A Converter |
| 8, 9, 11,12 | TRM1-4 | Used for precision post-package trimming of the VDAC voltage. Do not make any connection to these pins. |
| 10 | VOSNS- | Remote Sense Input. Connect to ground at the Load. |
| 13 | ROSC | Connect a resistor to VOSNS- to program oscillator frequency and FB, OCSET, BBFB, and VDAC bias currents |
| 14 | VDAC | Regulated voltage programmed by the VID inputs. Current Sensing and PWM operation are referenced to this pin. Connect an external RC network to VOSNS- to program Dynamic VID slew rate. |
| 15 | OCSET | Programs the hiccup over-current threshold through an external resistor tied to VDAC and an internal current source. Over-current protection can be disabled by connecting this pin to a DC voltage no greater than 6.5V (do not float this pin as improper operation will occur). |
| 16 | IIN | Current Sense input from the Phase IC(s). To ensure proper operation bias to at least 250mV (don't float this pin). |
| 17 | VDRP | Buffered IIN signal. Connect an external RC network to FB to program converter output impedance |
| 18 | FB | Inverting input to the Error Amplifier. Converter output voltage is offset from the VDAC voltage through an external resistor connected to the converter output voltage at the load and an internal current source. |
| 19 | EAOUT | Output of the Error Amplifier |
| 20 | BBFB | Input to the Regulation Detect Comparator. Connect to converter output voltage and VDRP pin through resistor network to program recovery from VID step-down. Connect to ground to disable Body Braking™ during transition to a lower VID code. |
| 21 | VBIAS | 6.8V/5mA Regulated output used as a system reference voltage for internal circuitry and the Phase ICs. |
| 22 | VCC | Power for internal circuitry |
| 23 | LGND | Local Ground and IC substrate connection |
| 24 | RMPOUT | Oscillator Output voltage. Used by Phase ICs to program Phase Delay |
| 25 | SS/DEL | Controls Converter Softstart, Power Good, and Over-Current Delay Timing. Connect an external capacitor to LGND to program the timing. An optional resistor can be added in series with the capacitor to reduce the over-current delay time. |
| 26 | PWRGD | Open Collector output that drives low during Softstart and any external fault condition. Connect external pull-up. |
| 27 | N/C | No internal connection |
| 28 | ENABLE | Enable Input. A logic low applied to this pin puts the IC into Fault mode. |

## SYSTEM THEORY OF OPERATION

### *XPhase*™ Architecture

The *XPhase*™ architecture is designed for multiphase interleaved buck converters which are used in applications requiring small size, design flexibility, low voltage, high current and fast transient response. The architecture can control converters of any phase number where flexibility facilitates the design trade-off of multiphase converters. The scalable architecture can be applied to other applications which require high current or multiple output voltages.

As shown in Figure 1, the *XPhase*™ architecture consists of a Control IC and a scalable array of phase converters each using a single Phase IC. The Control IC communicates with the Phase ICs through a 5-wire analog bus, i.e. bias voltage, phase timing, average current, error amplifier output, and VID voltage. The Control IC incorporates all the system functions, i.e. VID, PWM ramp oscillator, error amplifier, bias voltage, and fault protections etc. The Phase IC implements the functions required by the converter of each phase, i.e. the gate drivers, PWM comparator and latch, over-voltage protection, and current sensing and sharing.

There is no unused or redundant silicon with the *XPhase*™ architecture compared to others such as a 4 phase controller that can be configured for 2, 3, or 4 phase operation. PCB Layout is easier since the 5 wire bus eliminates the need for point-to-point wiring between the Control IC and each Phase. The critical gate drive and current sense connections are short and local to the Phase ICs. This improves the PCB layout by lowering the parasitic inductance of the gate drive circuits and reducing the noise of the current sense signal.

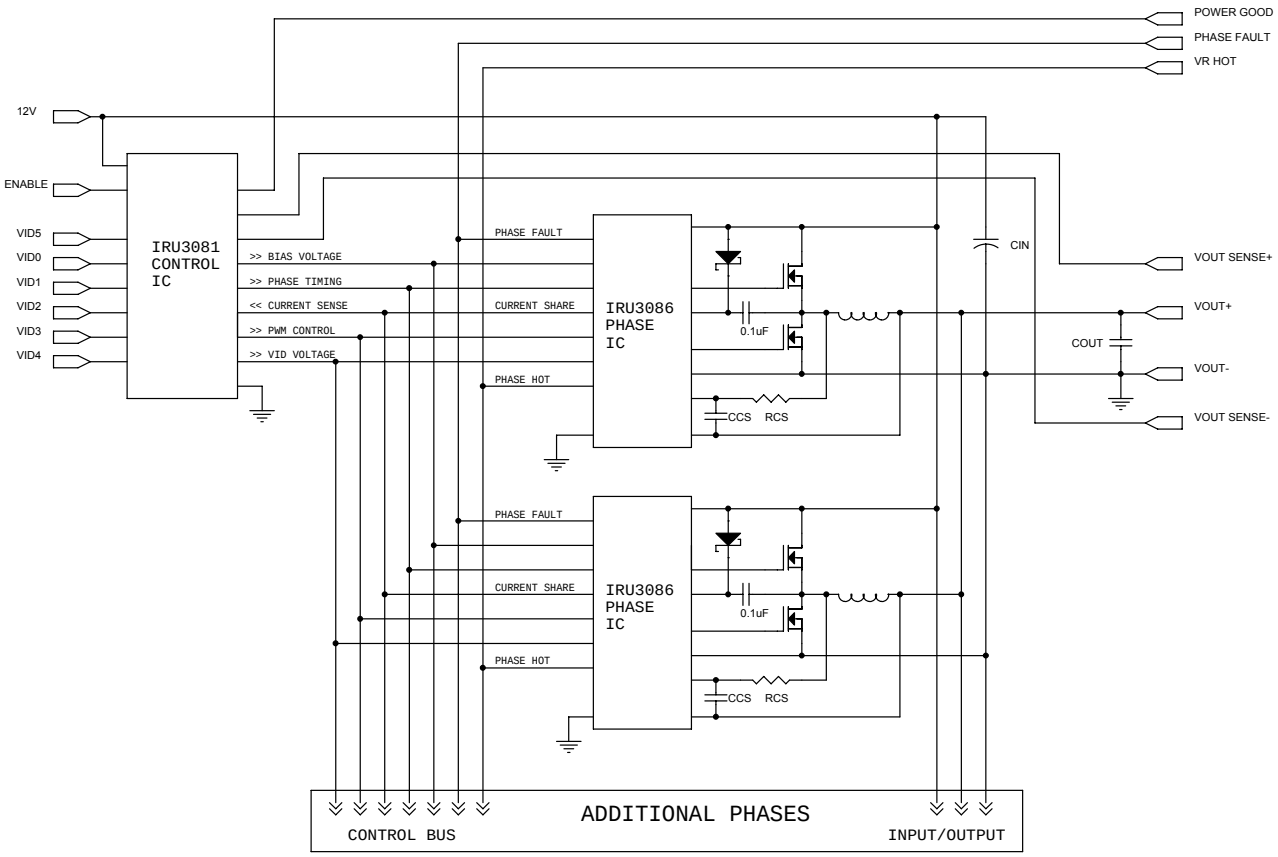



Figure 1. System Block Diagram

**PWM Control Method**

The PWM block diagram of the *XPhase*™ architecture is shown in Figure 2. Feed-forward voltage mode control with trailing edge modulation is used. A high-gain wide-bandwidth voltage type error amplifier in the Control IC is used for the voltage control loop. An external RC circuit connected to the input voltage and ground is used to program the slope of the PWM ramp and to provide the feed-forward control at each phase. The PWM ramp slope will change with the input voltage and automatically compensate for changes in the input voltage. The input voltage can change due to variations in the silver box output voltage or due to the wire and PCB-trace voltage drop related to changes in load current.

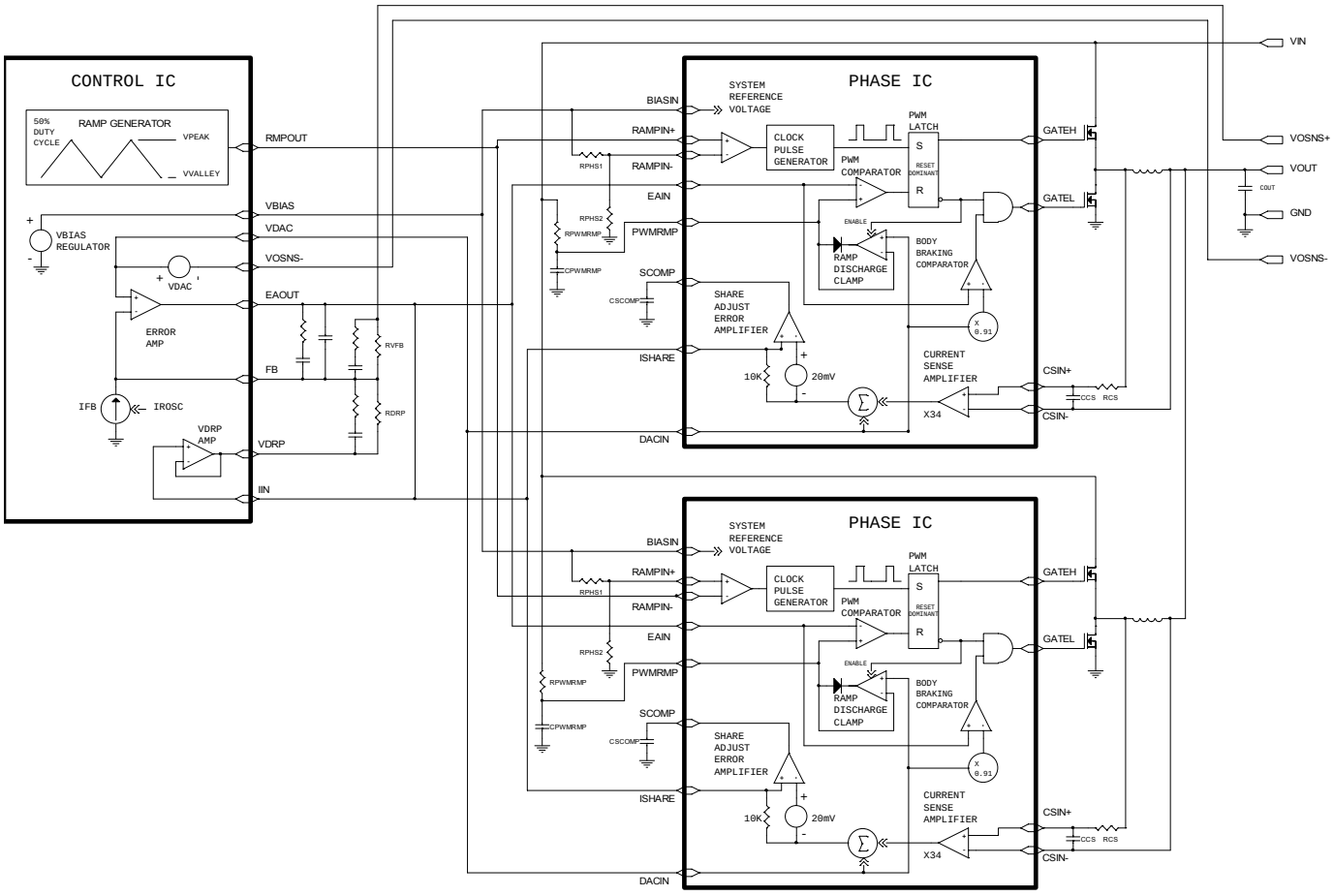



Figure 2. PWM Block Diagram

**Frequency and Phase Timing Control**

The oscillator is located in the Control IC and its frequency is programmable from 150kHz to 1MHZ by an external resistor. The output of the oscillator is a 50% duty cycle triangle waveform with peak and valley voltages of approximately 5V and 1V respectively. This signal is used to program both the switching frequency and phase timing of the Phase ICs. The Phase IC is programmed by resistor divider $R_{PHS1}$ and $R_{PHS2}$ connected between the VBIAS reference voltage and the Phase IC LGND pin. A comparator in the Phase ICs detects the crossing of the oscillator waveform over the voltage generated by the resistor divider and triggers a clock pulse that starts the PWM cycle. The peak and valley voltages track the VBIAS voltage reducing potential Phase IC timing errors. Figure 3 shows the Phase timing for an 8 phase converter. Note that both slopes of the triangle waveform can be used for phase timing by swapping the RMPIN+ and RMPIN– pins, as shown in Figure 2.

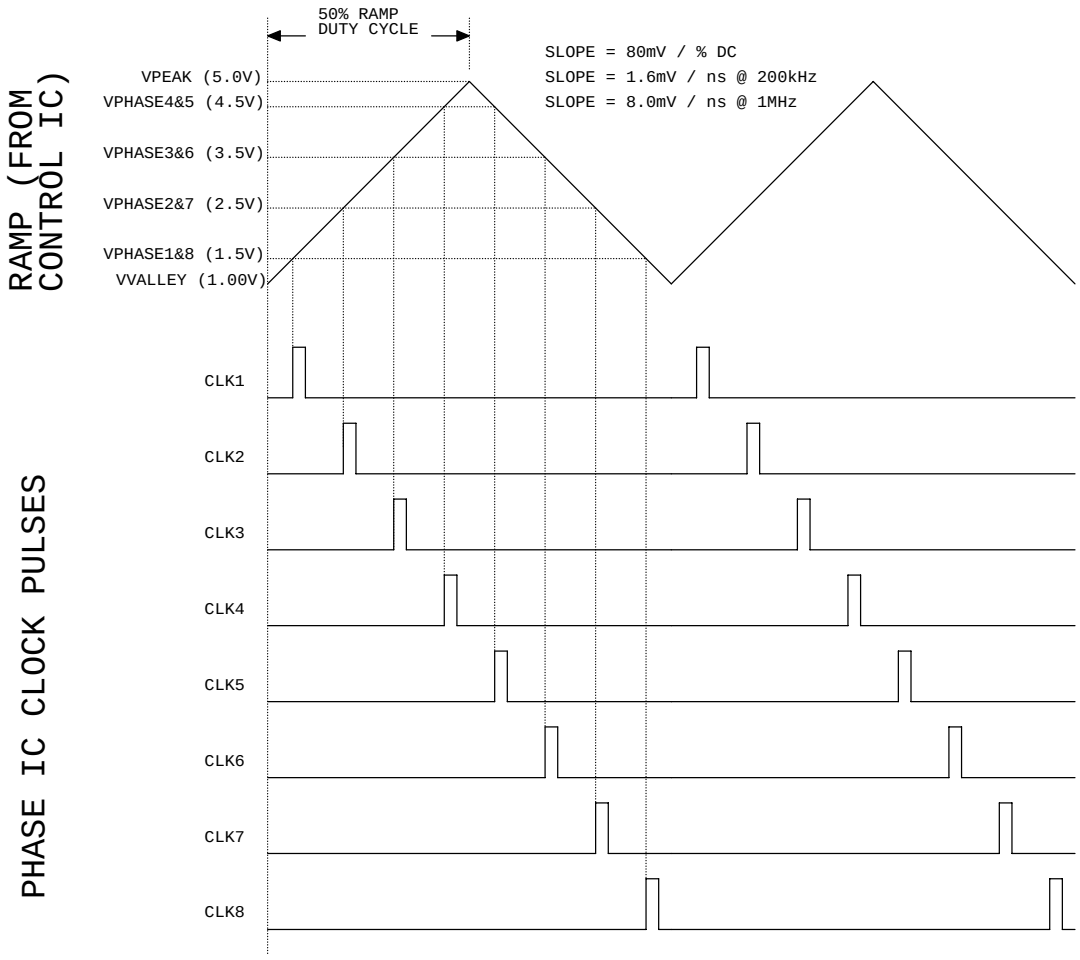



Figure 3. 8 Phase Oscillator Waveforms

**PWM Operation**

The PWM comparator is located in the Phase IC. Upon receiving a clock pulse, the PWM latch is set; the PWMRMP voltage begins to increase; the low side driver is turned off, and the high side driver is then turned on after the non-overlap time. When the PWMRMP voltage exceeds the Error Amplifier's output voltage, the PWM latch is reset. This turns off the high side driver and then turns on the low side driver after the non-overlap time; it activates the Ramp Discharge Clamp, which quickly discharges the PWMRMP capacitor to the VDAC voltage of the Control IC until the next clock pulse.

The PWM latch is reset dominant allowing all phases to go to zero duty cycle within a few tens of nanoseconds in response to a load step decrease. Phases can overlap and go to 100% duty cycle in response to a load step increase with turn-on gated by the clock pulses. An Error Amplifier output voltage greater than the common mode input range of the PWM comparator results in 100% duty cycle regardless of the voltage of the PWM ramp. This arrangement guarantees the Error Amplifier is always in control and can demand 0 to 100% duty cycle as required. It also favors response to a load step decrease which is appropriate given the low output to input voltage ratio of most systems. The inductor current will increase much more rapidly than decrease in response to load transients.

This control method is designed to provide "single cycle transient response" where the inductor current changes in response to load transients within a single switching cycle maximizing the effectiveness of the power train and minimizing the output capacitor requirements. An additional advantage of the architecture is that differences in ground or input voltage at the phases have no effect on operation since the PWM ramps are referenced to VDAC.

Figure 4 depicts PWM operating waveforms under various conditions.

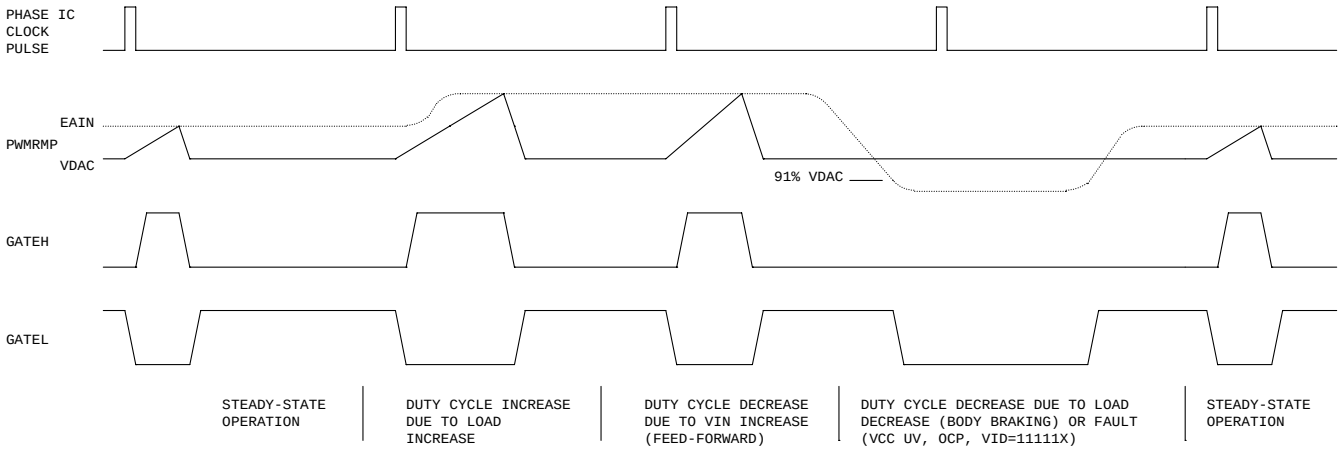



Figure 4. PWM Operating Waveforms

**Body Braking™**

In a conventional synchronous buck converter, the minimum time required to reduce the current in the inductor in response to a load step decrease is;

$$T_{SLEW} = \frac{L*(I_{MAX} - I_{MIN})}{V_O}$$

The slew rate of the inductor current can be significantly increased by turning off the synchronous rectifier in response to a load step decrease. The switch node voltage is then forced to decrease until conduction of the synchronous rectifier's body diode occurs. This increases the voltage across the inductor from Vout to Vout + $V_{BODYDIODE}$. The minimum time required to reduce the current in the inductor in response to a load transient decrease is now;

$$T_{SLEW} = \frac{L*(I_{MAX} - I_{MIN})}{V_O + V_{BODYDIODE}}$$

Since the voltage drop in the body diode is often higher than output voltage, the inductor current slew rate can be increased by 2X or more. This patent pending technique is referred to as "body braking" and is accomplished through the "0% Duty Cycle Comparator" located in the Phase IC. If the Error Amplifier's output voltage drops below 91% of the VDAC voltage this comparator turns off the low side gate driver.

**Lossless Average Inductor Current Sensing**

Inductor current can be sensed by connecting a series resistor and a capacitor network in parallel with the inductor and measuring the voltage across the capacitor, as shown in Figure 5. The equation of the sensing network is,

$$v_C(s) = v_L(s)\frac{1}{1+sR_{CS}C_{CS}} = i_L(s)\frac{R_L + sL}{1+sR_{CS}C_{CS}}$$

Usually the resistor Rcs and capacitor Ccs are chosen so that the time constant of Rcs and Ccs equals the time constant of the inductor which is the inductance L over the inductor DCR ($R_L$). If the two time constants match, the voltage across Ccs is proportional to the current through L, and the sense circuit can be treated as if only a sense resistor with the value of $R_L$ was used. The mismatch of the time constants does not affect the measurement of inductor DC current, but affects the AC component of the inductor current.

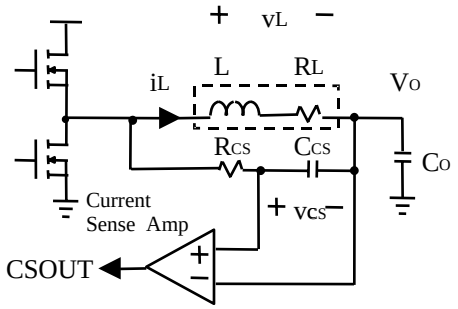



Figure 5. Inductor Current Sensing and Current Sense Amplifier

The advantage of sensing the inductor current versus high side or low side sensing is that actual output current being delivered to the load is obtained rather than peak or sampled information about the switch currents. The output voltage can be positioned to meet a load line based on real time information. Except for a sense resistor in series with the inductor, this is the only sense method that can support a single cycle transient response. Other methods provide no information during either load increase (low side sensing) or load decrease (high side sensing).

An additional problem associated with peak or valley current mode control for voltage positioning is that they suffer from peak-to-average errors. These errors will show in many ways but one example is the effect of frequency variation. If the frequency of a particular unit is 10% low, the peak to peak inductor current will be 10% larger and the output impedance of the converter will drop by about 10%. Variations in inductance, current sense amplifier bandwidth, PWM prop delay, any added slope compensation, input voltage, and output voltage are all additional sources of peak-to-average errors.

**Current Sense Amplifier**

A high speed differential current sense amplifier is located in the Phase IC, as shown in Figure 5. Its gain decreases with increasing temperature and is nominally 34 at 25ºC and 29 at 125ºC (-1470 ppm/ºC). This reduction of gain tends to compensate the 3850 ppm/ºC increase in inductor DCR. Since in most designs the Phase IC junction is hotter than the inductor these two effects tend to cancel such that no additional temperature compensation of the load line is required.

The current sense amplifier can accept positive differential input up to 100mV and negative up to -20mV before clipping. The output of the current sense amplifier is summed with the DAC voltage and sent to the Control IC and other Phases through an on-chip 10KΩ resistor connected to the ISHARE pin. The ISHARE pins of all the phases are tied together and the voltage on the share bus represents the average current through all the inductors and is used by the Control IC for voltage positioning and current limit protection.

**Average Current Share Loop**

Current sharing between phases of the converter is achieved by the average current share loop in each Phase IC. The output of the current sense amplifier is compared with the share bus less a 20mV offset. If current in a phase is smaller than the average current, the share adjust amplifier of the phase will activate a current source that reduces the slope of its PWM ramp thereby increasing its duty cycle and output current. The crossover frequency of the current share loop can be programmed with a capacitor at the SCOMP pin so that the share loop does not interact with the output voltage loop.

## IR3081PBF THEORY OF OPERATION

### Block Diagram

The Block diagram of the IR3081PBF is shown in Figure 6, and specific features are discussed in the following sections.

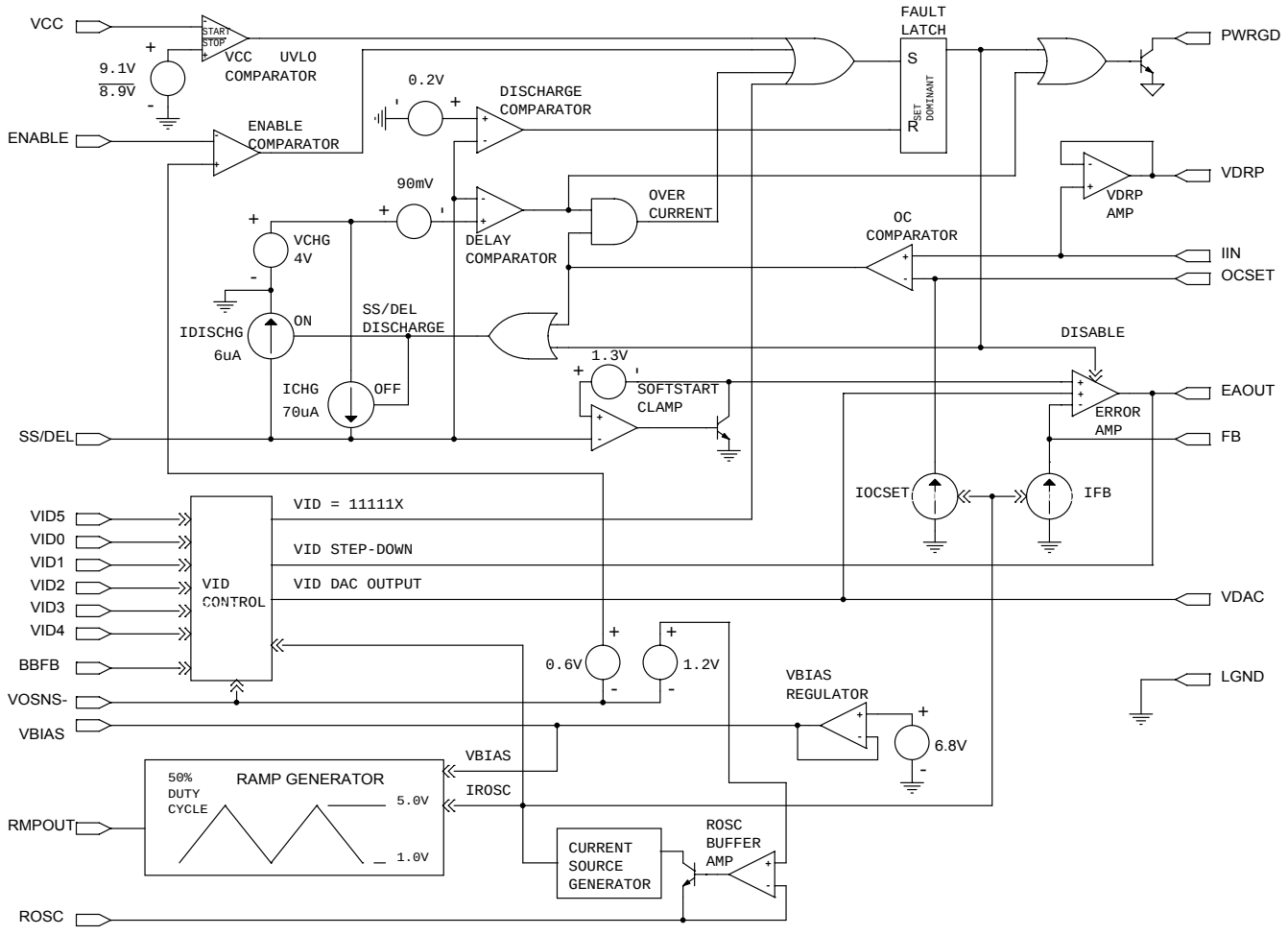



Figure 6. IR3081PBF Block Diagram

### VID Control

A 6-bit VID voltage compatible with VR 10, as shown in Table 1, is available at the VDAC pin. A detailed block diagram of the VID control circuitry can be found in Figure 7. The VID pins require an external bias voltage and should not be floated. The VID input comparators, with 0.6V reference, monitor the VID pins and control the 6 bit Digital-to-Analog Converter (DAC) whose output is sent to the VDAC buffer amplifier. The output of the buffer amplifier is the VDAC pin. The VDAC voltage is post-package trimmed to compensate for the input offsets of the Error Amplifier to provide a 0.5% **system set-point** accuracy. The actual VDAC voltage does not determine the system accuracy and has a wider tolerance.

The IR3081PBF can accept changes in the VID code while operating and vary the DAC voltage accordingly. The sink/source capability of the VDAC buffer amplifier is programmed by the same external resistor that sets the oscillator frequency. The slew rate of the voltage at the VDAC pin can be adjusted by an external capacitor between VDAC pin and the VOSNS- pin. A resistor connected in series with this capacitor is required to compensate the VDAC buffer amplifier. Digital VID transitions result in a smooth analog transition of the VDAC voltage and converter output voltage minimizing inrush currents in the input and output capacitors and overshoot of the output voltage.

It is desirable to prevent negative inductor currents in response to a request for a lower VID code. Negative current transforms the buck converter into a boost converter and transfers energy from the output capacitors back into the input voltage. This energy can cause voltage spikes and damage the silver box or other components unless they are specifically designed to handle it. Furthermore, power is wasted during the transfer of energy from the output back to the input.

The IR3081PBF includes circuitry that turns off both control and synchronous MOSFETs in response to a lower VID code so that the load current instead of the inductor discharges the output capacitors. A lower VID code is detected by the VID step-down detect comparator which monitors the “fast” output of the DAC (plus 7mV for noise immunity) compared to the “slow” output of the VDAC pin. If a dynamic VID step down is detected, the body brake latch is set and the output of the error amplifier is pulled down to 75% of the DAC voltage by the VID body brake clamp. This triggers the Body Braking™ function which turns off both high side and low side drivers in the phase ICs.

The converter’s output voltage needs to be monitored and compared to the VDAC voltage to determine when to resume normal operation. Unfortunately, the voltage on the FB pin can be pulled down by its compensation network during the sudden decrease in the Error Amplifier’s output voltage so an additional pin BBFB is provided. The BBFB pin is connected to the converter output voltage and VDRP pin with resistors of the same value as on the FB pin and therefore provides an un-corrupted representation of converter output voltage. The regulation detect comparator compares the BBFB to the VDAC voltage and resets the body brake latch releasing the error amplifier’s output and allowing normal operation to resume. Body Braking™ during a transition to a lower VID code can be disabled by connecting the BBFB pin to ground.

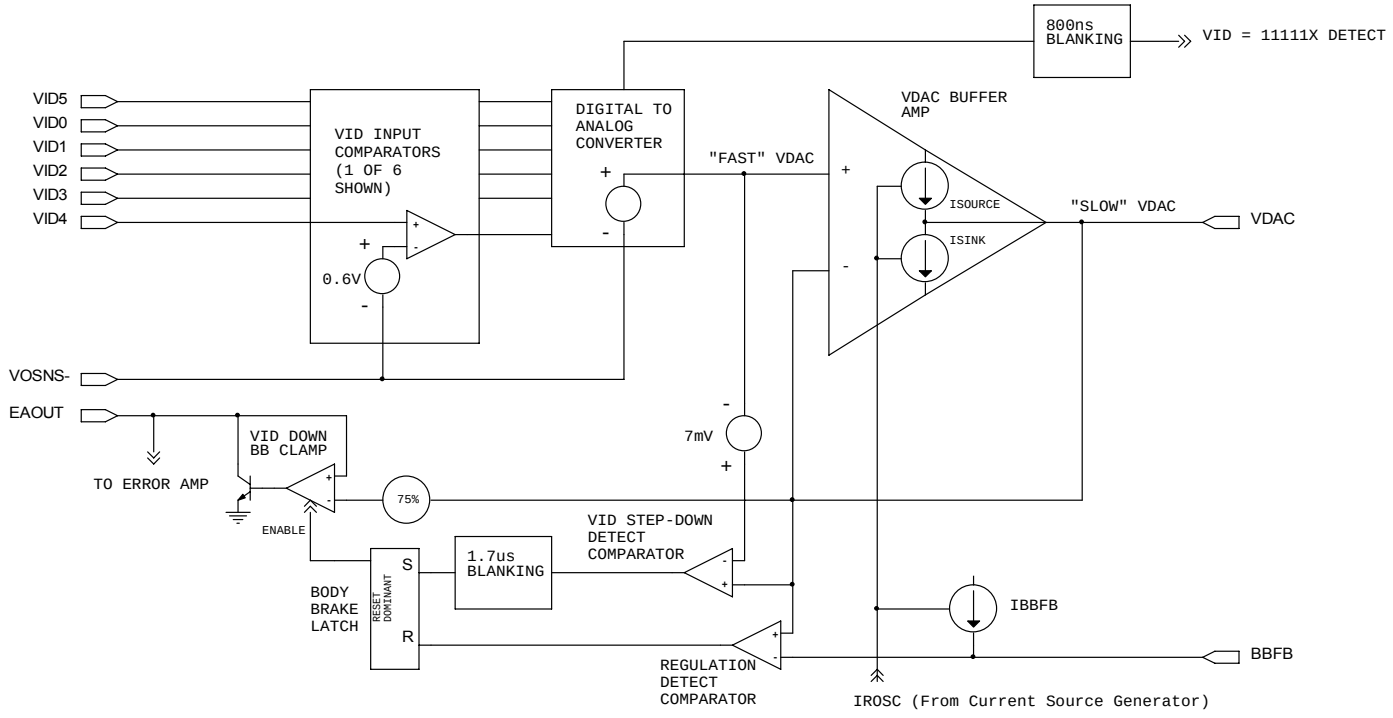



Figure 7. VID Control Block Diagram

| Processor Pins (0 = low, 1 = high) | | | | | | Vout (V) | | Processor Pins (0 = low, 1 = high) | | | | | | Vout (V) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VID4 | VID3 | VID2 | VID1 | VID0 | VID5 | | | VID4 | VID3 | VID2 | VID1 | VID0 | VID5 | |
| 0 | 1 | 0 | 1 | 0 | 0 | 0.8375 | | 1 | 1 | 0 | 1 | 0 | 0 | 1.2125 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0.8500 | | 1 | 1 | 0 | 0 | 1 | 1 | 1.2250 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0.8625 | | 1 | 1 | 0 | 0 | 1 | 0 | 1.2375 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0.8750 | | 1 | 1 | 0 | 0 | 0 | 1 | 1.2500 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0.8875 | | 1 | 1 | 0 | 0 | 0 | 0 | 1.2625 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0.9000 | | 1 | 0 | 1 | 1 | 1 | 1 | 1.2750 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0.9125 | | 1 | 0 | 1 | 1 | 1 | 0 | 1.2875 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0.9250 | | 1 | 0 | 1 | 1 | 0 | 1 | 1.3000 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0.9375 | | 1 | 0 | 1 | 1 | 0 | 0 | 1.3125 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0.9500 | | 1 | 0 | 1 | 0 | 1 | 1 | 1.3250 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0.9625 | | 1 | 0 | 1 | 0 | 1 | 0 | 1.3375 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0.9750 | | 1 | 0 | 1 | 0 | 0 | 1 | 1.3500 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0.9875 | | 1 | 0 | 1 | 0 | 0 | 0 | 1.3625 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1.0000 | | 1 | 0 | 0 | 1 | 1 | 1 | 1.3750 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1.0125 | | 1 | 0 | 0 | 1 | 1 | 0 | 1.3875 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1.0250 | | 1 | 0 | 0 | 1 | 0 | 1 | 1.4000 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1.0375 | | 1 | 0 | 0 | 1 | 0 | 0 | 1.4125 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1.0500 | | 1 | 0 | 0 | 0 | 1 | 1 | 1.4250 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1.0625 | | 1 | 0 | 0 | 0 | 1 | 0 | 1.4375 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1.0750 | | 1 | 0 | 0 | 0 | 0 | 1 | 1.4500 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1.0875 | | 1 | 0 | 0 | 0 | 0 | 0 | 1.4625 |
| 1 | 1 | 1 | 1 | 1 | 1 | OFF[4] | | 0 | 1 | 1 | 1 | 1 | 1 | 1.4750 |
| 1 | 1 | 1 | 1 | 1 | 0 | OFF[4] | | 0 | 1 | 1 | 1 | 1 | 0 | 1.4875 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1.1000 | | 0 | 1 | 1 | 1 | 0 | 1 | 1.5000 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1.1125 | | 0 | 1 | 1 | 1 | 0 | 0 | 1.5125 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1.1250 | | 0 | 1 | 1 | 0 | 1 | 1 | 1.5250 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1.1375 | | 0 | 1 | 1 | 0 | 1 | 0 | 1.5375 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1.1500 | | 0 | 1 | 1 | 0 | 0 | 1 | 1.5500 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1.1625 | | 0 | 1 | 1 | 0 | 0 | 0 | 1.5625 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1.1750 | | 0 | 1 | 0 | 1 | 1 | 1 | 1.5750 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1.1875 | | 0 | 1 | 0 | 1 | 1 | 0 | 1.5875 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1.2000 | | 0 | 1 | 0 | 1 | 0 | 1 | 1.6000 |

Note: 3. Output disabled (Fault mode)

Table 1. Voltage Identification (VID)

**Adaptive Voltage Positioning**

Adaptive voltage positioning is needed to reduce the output voltage deviations during load transients and the power dissipation of the load when it is drawing maximum current. The circuitry related to voltage positioning is shown in Figure 8. Resistor $R_{FB}$ is connected between the Error Amplifier's inverting input pin FB and the converter's output voltage. An internal current source whose value is programmed by the same external resistor that programs the oscillator frequency pumps current into the FB pin. The error amplifier forces the converter's output voltage lower to maintain a balance at its inputs. $R_{FB}$ is selected to program the desired amount of fixed offset voltage below the DAC voltage.

The voltage at the VDRP pin is a buffered version of the share bus and represents the sum of the DAC voltage and the average inductor current of all the phases. The VDRP pin is connected to the FB pin through the resistor $R_{DRP}$. Since the Error Amplifier will force the loop to maintain FB to be equal to the VDAC reference voltage, an additional current will flow into the FB pin equal to (VDRP-VDAC) / $R_{DRP}$. When the load current increases, the adaptive positioning voltage increases accordingly. More current flows through the feedback resistor $R_{FB}$, and makes the output voltage lower proportional to the load current. The positioning voltage can be programmed by the resistor $R_{DRP}$ so that the droop impedance produces the desired converter output impedance. The offset and slope of the converter output impedance are referenced to and therefore independent of the VDAC voltage.

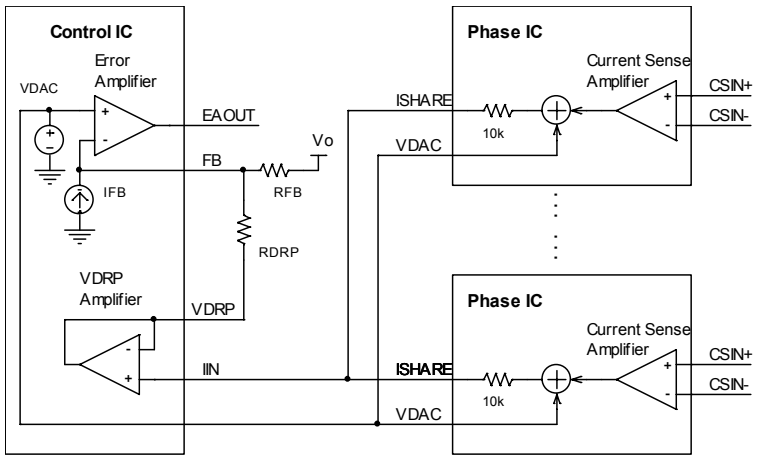



Figure 8. Adaptive voltage positioning

**Inductor DCR Temperature Correction**

If the thermal compensation of the inductor DCR provided by the temperature dependent gain of the current sense amplifier is not adequate, a negative temperature coefficient (NTC) thermistor can be used for additional correction. The thermistor should be placed close to the inductor and connected in parallel with the feedback resistor, as shown in Figure 9. The resistor in series with the thermistor is used to reduce the nonlinearity of the thermistor. A similar network must be placed on the BBFB to ensure proper operation during a transition to a lower VID code with Body Braking™.

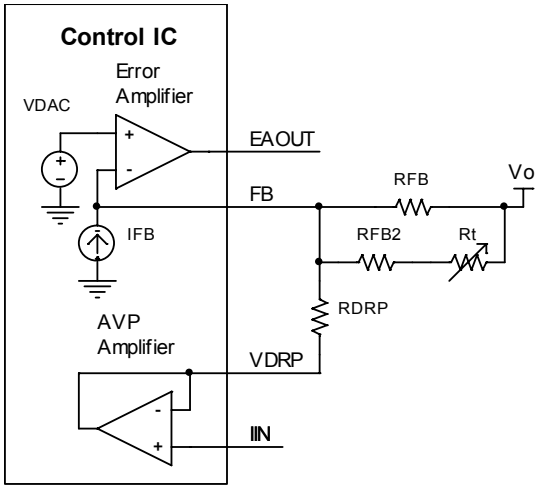



Figure 9. Temperature compensation of inductor DCR

**Remote Voltage Sensing**

To reduce the effect of impedance in the ground plane, the VOSNS- pin is used for remote sensing and connected directly to the load. The VDAC voltage is referenced to VOSNS- to avoid additional error terms or delay related to a separate differential amplifier. The capacitor connecting the VDAC and VOSNS- pins ensure that high speed transients are fed directly into the error amplifier without delay.

**Soft Start, Over-Current Fault Delay, and Hiccup Mode**

The IR3081PBF has a programmable soft-start function to limit the surge current during the converter start-up. A capacitor connected between the SS/DEL and LGND pins controls soft start as well as over-current protection delay and hiccup mode timing. A charge current of 70uA and discharge current of 6uA control the up slope and down slope of the voltage at the SS/DEL pin respectively.

Figure 10 depicts the various operating modes as controlled by the SS/DEL function. If there is no fault, the SS/DEL pin will begin to be charged. The error amplifier output is clamped low until SS/DEL reaches 1.3V. The error amplifier will then regulate the converter's output voltage to match the SS/DEL voltage less the 1.3V offset until it reaches the level determined by the VID inputs. The SS/DEL voltage continues to increase until it rises above 3.91V and allows the PWRGD signal to be asserted. SS/DEL finally settles at 4V, indicating the end of the soft start.

Under Voltage Lock Out and VID=11111x faults as well as a low signal on the ENABLE input immediately sets the fault latch causing SS/DEL to begin to discharge. The SS/DEL capacitor will continue to discharge down to 0.2V. If the fault has cleared the fault latch will be reset by the discharge comparator allowing a normal soft start to occur.

A delay is included if an over-current condition occurs after a successful soft start sequence. This is required since over-current conditions can occur as part of normal operation due to load transients or VID transitions. If an over-current fault occurs during normal operation it will initiate the discharge of the capacitor at SS/DEL but will not set the fault latch immediately. If the over-current condition persists long enough for the SS/DEL capacitor to discharge below the 90mV offset of the delay comparator, the Fault latch will be set pulling the error amplifier's output low inhibiting switching in the phase ICs and de-asserting the PWRGD signal. The SS/DEL capacitor will continue to discharge until it reaches 0.2V and the fault latch is reset allowing a normal soft start to occur. If an over-current condition is again encountered during the soft start cycle the fault latch will be set without any delay and hiccup mode will begin. During hiccup mode the charge to discharge current ratio results in a fixed 7.9% hiccup mode duty cycle regardless of at what point the over-current condition occurs. However, the hiccup frequency is determined by the load current and over-current set value.

The over-current delay can be reduced by adding a resistor in series with the SS/DEL capacitor. The delay comparator's offset voltage is reduced by the drop in the resistor caused by the discharge current. The value of the series resistor should be 10KΩ or less to avoid interference with the soft start function.

If SS/DEL pin is pulled below 0.9V, the converter can be disabled.

**Under Voltage Lockout (UVLO)**

The UVLO function monitors the IR3081PBF's VCC supply pin and ensures that IR3081PBF has a high enough voltage to power the internal circuit. The IR3081PBF's UVLO is set higher than the minimum operating voltage of compatible Phase ICs thus providing UVLO protection for them as well. During power-up the fault latch is reset when VCC exceeds 9.1V and there is no other fault. If the VCC voltage drops below 8.9V the fault latch will be set. For converters using a separate 5V supply for gate driver bias an external UVLO circuit can be added to prevent any operation until adequate voltage is present. A diode connected between the 5V supply and the SS/DEL pin provides a simple 5V UVLO function.

**Over Current Protection (OCP)**

The current limit threshold is set by a resistor connected between the OCSET and VDAC pins. If the IIN pin voltage, which is proportional to the average current plus DAC voltage, exceeds the OCSET voltage, the over-current protection is triggered.

**VID = 11111X Fault**

VID codes of 111111 and 111110 will set the fault latch and disable the error amplifier. An 800ns delay is provided to prevent a fault condition from occurring during Dynamic VID changes.

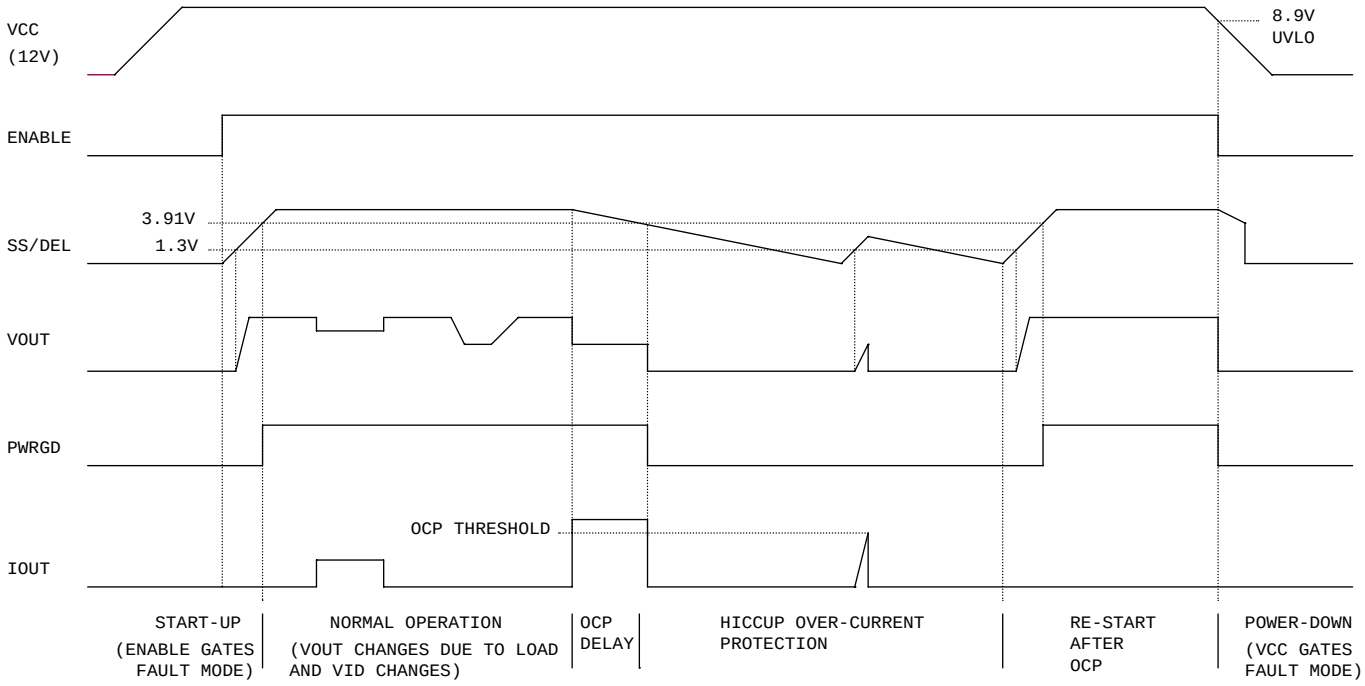



Figure 10. Operating Waveforms

**Power Good Output**

The PWRGD pin is an open-collector output and should be pulled up to a voltage source through a resistor. During soft start, the PWRGD remains low until the output voltage is in regulation and SS/DEL is above 3.91V. The PWRGD pin becomes low if the fault latch is set. A high level at the PWRGD pin indicates that the converter is in operation and has no fault, but does not ensure the output voltage is within the specification. Output voltage regulation within the design limits can logically be assured however, assuming no component failure in the system.

**Load Current Indicator Output**

The VDRP pin voltage represents the average current of the converter plus the DAC voltage. The load current information can be retrieved by a differential amplifier which subtracts the VDAC voltage from the VDRP voltage.

**System Reference Voltage (VBIAS)**

The IR3081PBF supplies a 6.8V/5mA precision reference voltage from the VBIAS pin. The oscillator ramp amplitude tracks the VBIAS voltage, which should be used to program the Phase IC trip points to minimize phase delay errors.

**Enable Input**

Pulling the ENABLE pin below 0.6V sets the Fault Latch.

## APPLICATION INFORMATION

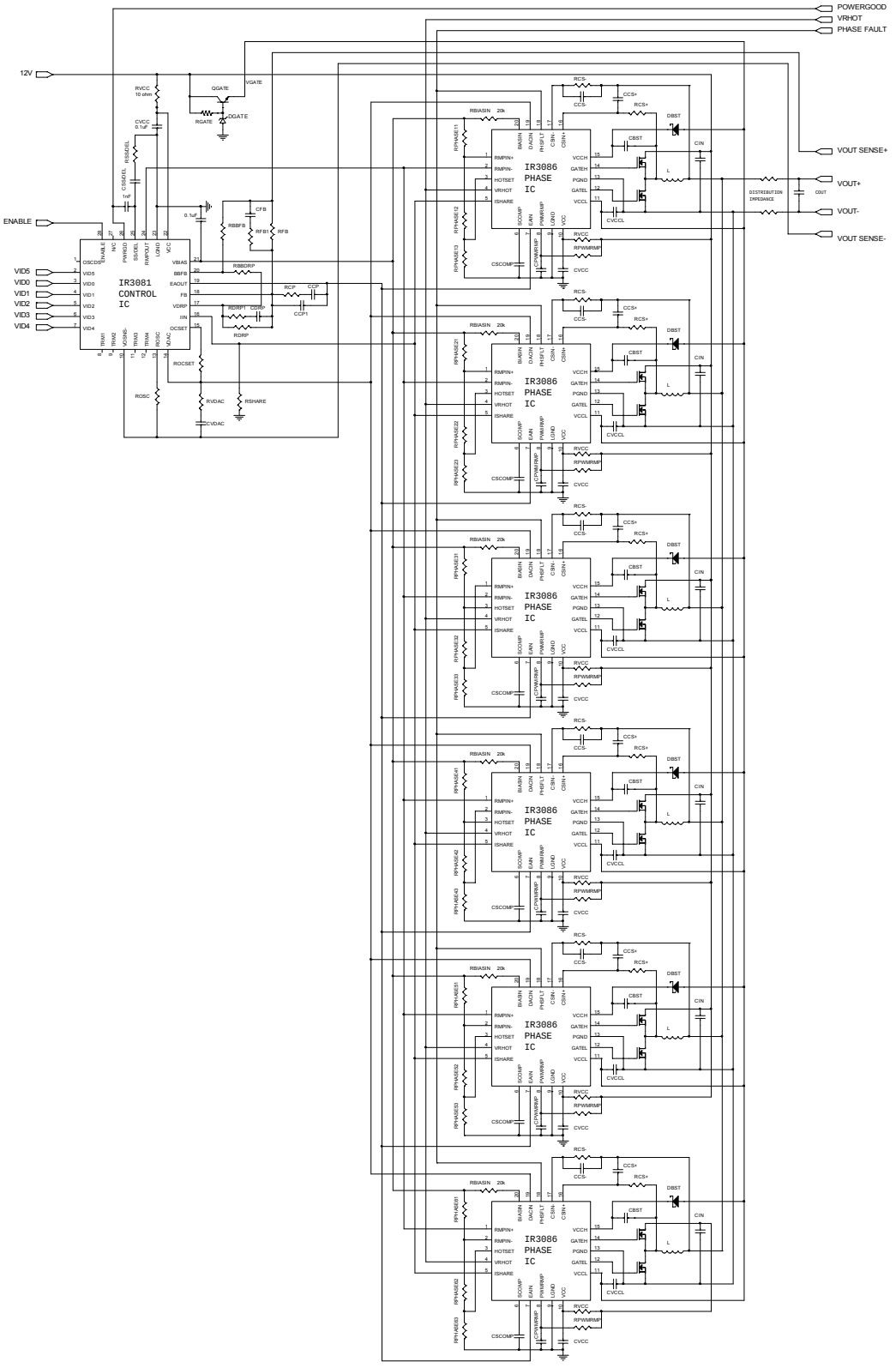



Figure 11. IR3081PBF/IR3086 Six-Phase VRM/EVRD 10 Converter

## DESIGN PROCEDURES - IR3081PBF AND IR3086 CHIPSET

### IR3081PBF EXTERNAL COMPONENTS

#### Oscillator Resistor *Rosc*

The oscillator of IR3081PBF generates a triangle waveform to synchronize the phase ICs, and the switching frequency of the each phase converter equals the oscillator frequency, which is set by the external resistor $R_{OSC}$ according to the curve in Figure 13.

#### Soft Start Capacitor *CSS/DEL* and Resistor *RSS/DEL*

Because the capacitor $C_{SS/DEL}$ programs four different time parameters, i.e. soft start delay time, soft start time, over-current latch delay time, and power good delay time, they should be considered together while choosing $C_{SS/DEL}$.

The SS/DEL pin voltage controls the slew rate of the converter output voltage, as shown in Figure 10. After the ENABLE pin voltage rises above 0.6V, there is a soft-start delay time $t_{SSDEL}$, after which the error amplifier output is released to allow the soft start. The soft start time $t_{SS}$ represents the time during which converter voltage rises from zero to $V_O$. $t_{SS}$ can be programmed by an external capacitor, which is determined by Equation (1).

$$C_{SS/DEL} = \frac{I_{CHG} * t_{SS}}{V_O} = \frac{70*10^{-6} * t_{SS}}{V_O} \quad (1)$$

Once $C_{SS/DEL}$ is chosen, the soft start delay time $t_{SSDEL}$, the over-current fault latch delay time $t_{OCDEL}$, and the delay time $t_{VccPG}$ from output voltage ($V_O$) in regulation to Power Good are fixed and shown in Equations (2), (3) and (4) respectively.

$$t_{SSDEL} = \frac{C_{SS/DEL} * 1.3}{I_{CHG}} = \frac{C_{SS/DEL} * 1.3}{70*10^{-6}} \quad (2)$$

$$t_{OCDEL} = \frac{C_{SS/DEL} * 0.09}{I_{DISCHG}} = \frac{C_{SS/DEL} * 0.09}{6*10^{-6}} \quad (3)$$

$$t_{VccPG} = \frac{C_{SS/DEL} * (3.91 - V_O - 1.3)}{I_{CHG}} = \frac{C_{SS/DEL} * (3.91 - V_O - 1.3)}{70*10^{-6}} \quad (4)$$

If faster over-current protection is required, a resistor in series with the soft start capacitor $C_{SS/DEL}$ can be used to reduce the over-current fault latch delay time $t_{OCDEL}$, and the resistor $R_{SS/DEL}$ is determined by Equation (5). Equation (1) for soft start capacitor $C_{SS/DEL}$ and Equation (4) for power good delay time $t_{VccPG}$ are unchanged, while the equation for soft start delay time $t_{SS/DEL}$ (Equation 2) is changed to Equation (6). Considering the worst case values of charge and discharge current, $R_{SS/DEL}$ should be no grater than 10kΩ.

$$R_{SS/DEL} = \frac{0.09 - \frac{t_{OCDEL} * I_{DISCHG}}{C_{SS/DEL}}}{I_{DISCHG}} = \frac{0.09 - \frac{t_{OCDEL} * 6*10^{-6}}{C_{SS/DEL}}}{6*10^{-6}} \quad (5)$$

$$t_{SSDEL} = \frac{C_{SS/DEL} * (1.3 - R_{SS/DEL} * I_{CHG})}{I_{CHG}} = \frac{C_{SS/DEL} * (1.3 - R_{SS/DEL} * 70*10^{-6})}{70*10^{-6}} \quad (6)$$

#### VDAC Slew Rate Programming Capacitor *CVDAC* and Resistor *RVDAC*

The slew rate of VDAC down-slope $SR_{DOWN}$ can be programmed by the external capacitor $C_{VDAC}$ as defined in Equation (7), where $I_{SINK}$ is the sink current of VDAC pin as shown in Figure 15. The resistor $R_{VDAC}$ is used to compensate VDAC circuit and is determined by Equation (8). The slew rate of VDAC up-slope $SR_{UP}$ is proportional

to that of VDAC down-slope and is given by Equation (9), where ISOURCE is the source current of VDAC pin as shown in Figure15.

$$C_{VDAC} = \frac{I_{SINK}}{SR_{DOWN}} \quad (7)$$

$$R_{VDAC} = 0.5 + \frac{3.2 * 10^{-15}}{C_{VDAC}{}^2} \quad (8)$$

$$SR_{UP} = \frac{I_{SOURCE}}{C_{VDAC}} \quad (9)$$

**Over Current Setting Resistor *ROCSET***

The inductor DC resistance is utilized to sense the inductor current. The copper wire of inductor has a constant temperature coefficient of 3850 ppm/°C, and therefore the maximum inductor DCR can be calculated from Equation (10), where RL_MAX and RL_ROOM are the inductor DCR at maximum temperature TL_MAX and room temperature T_ROOM respectively.

$$R_{L\_MAX} = R_{L\_ROOM} * [1 + 3850 * 10^{-6} * (T_{L\_MAX} - T_{ROOM})] \quad (10)$$

The current sense amplifier gain of IR3086 decreases with temperature at the rate of 1470 ppm/°C, which compensates part of the inductor DCR increase. The phase IC die temperature is only a couple of degrees Celsius higher than the PCB temperature due to the low thermal impedance of MLPQ package. The minimum current sense amplifier gain at the maximum phase IC temperature TIC_MAX is calculated from Equation (11).

$$G_{CS\_MIN} = G_{CS\_ROOM} * [1 - 1470 * 10^{-6} * (T_{IC\_MAX} - T_{ROOM})] \quad (11)$$

The total input offset voltage (VCS_TOFST) of current sense amplifier in phase ICs is the sum of input offset (VCS_OFST) of the amplifier itself and that created by the amplifier input bias currents flowing through the current sense resistors RCS+ and RCS-.

$$V_{CS\_TOFST} = V_{CS\_OFST} + I_{CSIN+} * R_{CS+} - I_{CSIN-} * R_{CS-} \quad (12)$$

The over current limit is set by the external resistor ROCSET as defined in Equation (13), where ILIMIT is the required over current limit. IOCSET, the bias current of OCSET pin, changes with switching frequency setting resistor ROSC and is determined by the curve in Figure 14. KP is the ratio of inductor peak current over average current in each phase and is calculated from Equation (14).

$$R_{OCSET} = [\frac{I_{LIMIT}}{n} * R_{L\_MAX} * (1 + K_P) + V_{CS\_TOFST}] * G_{CS\_MIN} / I_{OCSET} \quad (13)$$

$$K_P = \frac{(V_I - V_O) * V_O / (L * V_I * f_{SW} * 2)}{I_O / n} \quad (14)$$

**No Load Output Voltage Setting Resistor *RFB* and Adaptive Voltage Positioning Resistor *RDRP***

A resistor between FB pin and the converter output is used to create output voltage offset VO_NLOFST, which is the difference between VDAC voltage and output voltage at no load condition. Adaptive voltage positioning further lowers the converter voltage by RO*IO, where RO is the required output impedance of the converter.

RFB is not only determined by IFB, the current flowing out of FB pin as shown in Figure 14, but also affected by the adaptive voltage positioning resistor RDRP and total input offset voltage of current sense amplifiers. RFB and RDRP are determined by (15) and (16) respectively.

$$R_{FB} = \frac{R_{L\_MAX} * V_{O\_NLOFST} - V_{CS\_TOFST} * n * R_O}{I_{FB} * R_{L\_MAX}} \quad (15)$$

$$R_{DRP} = \frac{R_{FB} * R_{L\_MAX} * G_{CS\_MIN}}{n * R_O} \quad (16)$$

### Body Braking™ Related Resistors *RBBFB* and *RBBDRP*

The body braking™ during Dynamic VID can be disabled by connecting BBFB pin to ground. If the feature is enabled, resistors RBBFB and RBBDRP are needed to restore the feedback voltage of the error amplifier after Dynamic VID step down. Usually RBBFB and RBBDRP are chosen to match RFB and RDRP respectively.

## IR3086 EXTERNAL COMPONENTS

### PWM Ramp Resistor *RPWMRMP* and Capacitor C*PWMRMP*

PWM ramp is generated by connecting the resistor RPWMRMP between a voltage source and PWMRMP pin as well as the capacitor CPWMRMP between PWMRMP and LGND. Choose the desired PWM ramp magnitude VRAMP and the capacitor CPWMRMP in the range of 100pF and 470pF, and then calculate the resistor RPWMRMP from Equation (17). To achieve feed-forward voltage mode control, the resistor RRAMP should be connected to the input of the converter.

$$R_{PWMRMP} = \frac{V_O}{V_{IN} * f_{SW} * C_{PWMRMP} * [\ln(V_{IN} - V_{DAC}) - \ln(V_{IN} - V_{DAC} - V_{PWMRMP})]} \quad (17)$$

### Inductor Current Sensing Capacitor *CCS+* and Resistors *RCS+* and *RCS-*

The DC resistance of the inductor is utilized to sense the inductor current. Usually the resistor RCS+ and capacitor CCS+ in parallel with the inductor are chosen to match the time constant of the inductor, and therefore the voltage across the capacitor CCS+ represents the inductor current. If the two time constants are not the same, the AC component of the capacitor voltage is different from that of the real inductor current. The time constant mismatch does not affect the average current sharing among the multiple phases, but affect the current signal ISHARE as well as the output voltage during the load current transient if adaptive voltage positioning is adopted.

Measure the inductance L and the inductor DC resistance RL. Pre-select the capacitor CCS+ and calculate RCS+ as follows.

$$R_{CS+} = \frac{L/R_L}{C_{CS+}} \quad (18)$$

The bias current flowing out of the non-inverting input of the current sense amplifier creates a voltage drop across RCS+, which is equivalent to an input offset voltage of the current sense amplifier. The offset affects the accuracy of converter current signal ISHARE as well as the accuracy of the converter output voltage if adaptive voltage positioning is adopted. To reduce the offset voltage, a resistor RCS- should be added between the amplifier inverting input and the converter output. The resistor RCS- is determined by the ratio of the bias current from the non-inverting input and the bias current from the inverting input.

$$R_{CS-} = \frac{I_{CSIN+}}{I_{CSIN-}} * R_{CS+} \quad (19)$$

If RCS- is not used, RCS+ should be chosen so that the offset voltage is small enough. Usually RCS+ should be less than 2 kΩ and therefore a larger CCS+ value is needed.

**Over Temperature Setting Resistors *RHOTSET1* and *RHOTSET2***

The threshold voltage of VRHOT comparator is proportional to the die temperature $T_J$ (ºC) of phase IC. Determine the relationship between the die temperature of phase IC and the temperature of the power converter according to the power loss, PCB layout and airflow etc, and then calculate HOTSET threshold voltage corresponding to the allowed maximum temperature from Equation (20).

$$V_{HOTSET} = 4.73 * 10^{-3} * T_J + 1.241 \quad (20)$$

There are two ways to set the over temperature threshold, central setting and local setting. In the central setting, only one resistor divider is used, and the setting voltage is connected to HOTSET pins of all the phase ICs. To reduce the influence of noise on the accuracy of over temperature setting, a 0.1uF capacitor should be placed next to HOTSET pin of each phase IC. In the local setting, a resistor divider per phase is needed, and the setting voltage is connected to HOTSET pin of each phase. The 0.1uF decoupling capacitor is not necessary. Use VBIAS as the reference voltage. If $R_{HOTSET1}$ is pre-selected, $R_{HOTSET2}$ can be calculated as follows.

$$R_{HOTSET2} = \frac{R_{HOTSET1} * V_{HOTSET}}{V_{BIAS} - V_{HOTSET}} \quad (21)$$

**Phase Delay Timing Resistors *RPHASE1* and *RPHASE2***

The phase delay of the interleaved multiphase converter is programmed by the resistor divider connected at RMPIN+ or RMPIN- depending on which slope of the oscillator ramp is used for the phase delay programming of phase IC, as shown in Figure 3.

If the upslope is used, RMPIN+ pin of the phase IC should be connected to RMPOUT pin of the control IC and RMPIN- pin should be connected to the resistor divider. When RMPOUT voltage is above the trip voltage at RMPIN- pin, the PWM latch is set. GATEL becomes low, and GATEH becomes high after the non-overlap time.

If down slope is used, RMPIN- pin of the phase IC should be connected to RMPOUT pin of the control IC and RMPIN+ pin should be connected to the resistor divider. When RMPOUT voltage is below the trip voltage at RMPIN- pin, the PWM latch is set. GATEL becomes low, and GATEH becomes high after the non-overlap time.

Use VBIAS voltage as the reference for the resistor divider since the oscillator ramp magnitude from control IC tracks VBIAS voltage. Try to avoid both edges of the oscillator ramp for better noise immunity. Determine the ratio of the programming resistors corresponding to the desired switching frequencies and phase numbers. If the resistor $R_{PHASEx1}$ is pre-selected, the resistor $R_{PHASEx2}$ is determined as:

$$R_{PHASEx2} = \frac{RA_{PHASEx} * R_{PHASEx1}}{1 - RA_{PHASEx}} \quad (22)$$

**Combined Over Temperature and Phase Delay Setting Resistors *RPHASE1*, *RPHASE2* and *RPHASE3***

The over temperature setting resistor divider can be combined with the phase delay resistor divider to save one resistor per phase.

Calculate the HOTSET threshold voltage $V_{HOTSET}$ corresponding to the allowed maximum temperature from Equation (20). If the over temperature setting voltage is lower than the phase delay setting voltage, VBIAS*$RA_{PHASEx}$, connect RMPIN+ or RMPIN- pin between $R_{PHASEx1}$ and $R_{PHASEx2}$, and connect HOTSET pin between $R_{PHASEx2}$ and $R_{PHASEx3}$. Pre-select $R_{PHASEx1}$,

$$R_{PHASEx2} = \frac{(RA_{PHASEx} * V_{BIAS} - V_{HOTSET}) * R_{PHASEx1}}{V_{BIAS} * (1 - RA_{PHASEx})} \quad (23)$$

$$R_{PHASEx3} = \frac{V_{HOTSET} * R_{PHASEx1}}{V_{BIAS} * (1 - RA_{PHASEx})} \quad (24)$$

If the over temperature setting voltage is higher than the phase delay setting voltage, VBIAS*RAPHASEx, connect HOTSET pin between RPHASEx1 and RPHASEx2 and connect RMPIN+ or RMPIN- between RPHASEx2 and RPHASEx3 respectively. Pre-select RPHASEx1,

$$R_{PHASEx2} = \frac{(V_{HOTSET} - RA_{PHASEx} * V_{BIAS}) * R_{PHASEx1}}{V_{BIAS} - V_{HOTSET}} \quad (25)$$

$$R_{PHASEx3} = \frac{RA_{PHASEx} * V_{BIAS} * R_{PHASEx1}}{V_{BIAS} - V_{HOTSET}} \quad (26)$$

**Bootstrap Capacitor *CBST***

Depending on the duty cycle and gate drive current of the phase IC, a 0.1uF to 1uF capacitor is needed for the bootstrap circuit.

**Decoupling Capacitors for Phase IC**

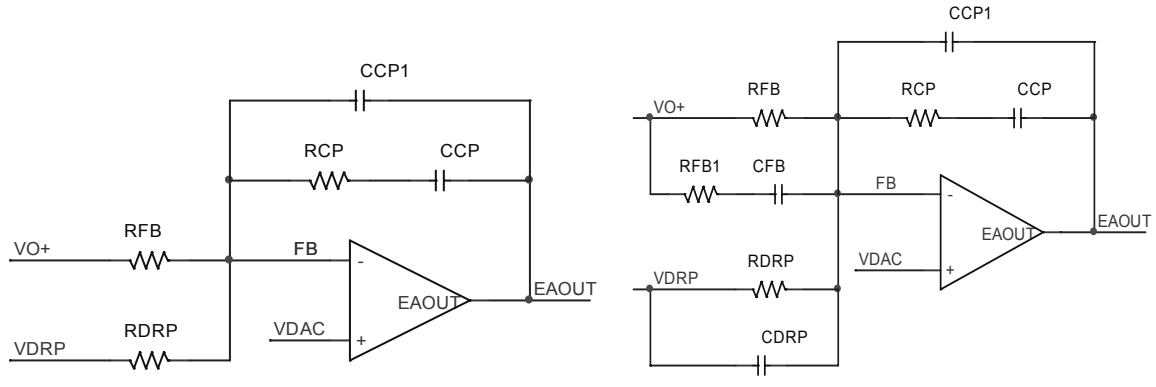
0.1uF-1uF decoupling capacitors are required at VCC and VCCL pins of phase ICs.

**VOLTAGE LOOP COMPENSATION**

The adaptive voltage positioning (AVP) is usually adopted in the computer applications to improve the transient response and reduce the power loss at heavy load. Like current mode control, the adaptive voltage positioning loop introduces extra zero to the voltage loop and splits the double poles of the power stage, which make the voltage loop compensation much easier.

Resistors RFB and RDRP are chosen according to Equations (15) and (16), and the selection of compensation types depends on the output capacitors used in the converter. For the applications using Electrolytic, Polymer or AL-Polymer capacitors and running at lower frequency, type II compensation shown in Figure 12(a) is usually enough. While for the applications using only ceramic capacitors and running at higher frequency, type III compensation shown in Figure 12(b) is preferred.

For applications where AVP is not required, the compensation is the same as for the regular voltage mode control. For converter using Polymer, AL-Polymer, and ceramic capacitors, which have much higher ESR zero frequency, type III compensation is required as shown in Figure 12(b) with RDRP and CDRP removed.




(a) Type II compensation (b) Type III compensation

Figure 12. Voltage loop compensation network

**Type II Compensation for AVP Applications**

Determine the compensation at no load, the worst case condition. Choose the crossover frequency fc between 1/10 and 1/5 of the switching frequency per phase. Assume the time constant of the resistor and capacitor across the output inductors matches that of the inductor, and determine RCP and CCP from Equations (27) and (28), where LE and CE are the equivalent inductance of output inductors and the equivalent capacitance of output capacitors respectively.

$$R_{CP} = \frac{(2\pi * f_C)^2 * L_E * C_E * R_{FB} * V_{PWMRMP}}{V_O * \sqrt{1 + (2\pi * f_C * C * R_C)^2}} \quad (27)$$

$$C_{CP} = \frac{10 * \sqrt{L_E * C_E}}{R_{CP}} \quad (28)$$

$C_{CP1}$ is optional and may be needed in some applications to reduce the jitter caused by the high frequency noise. A ceramic capacitor between 10pF and 220pF is usually enough.

**Type III Compensation for AVP Applications**

Determine the compensation at no load, the worst case condition. Assume the time constant of the resistor and capacitor across the output inductors matches that of the inductor, the crossover frequency and phase margin of the voltage loop can be estimated by Equations (29) and (30), where $R_{LE}$ is the equivalent resistance of inductor DCR.

$$f_{C1} = \frac{R_{DRP}}{2\pi * C_E * G_{CS} * R_{FB} * R_{LE}} \quad (29)$$

$$\theta_{C1} = 90 - A\tan(0.5) * \frac{180}{\pi} \quad (30)$$

Choose the desired crossover frequency fc around fc1 estimated by Equation (29) or choose fc between 1/10 and 1/5 of the switching frequency per phase, and select the components to ensure the slope of close loop gain is -20dB /Dec around the crossover frequency. Choose resistor $R_{FB1}$ according to Equation (31), and determine $C_{FB}$ and $R_{DRP}$ from Equations (32) and (33).

$$R_{FB1} = \frac{1}{2} R_{FB} \quad \text{to} \quad R_{FB1} = \frac{2}{3} R_{FB} \quad (31)$$

$$C_{FB} = \frac{1}{4\pi * f_C * R_{FB1}} \quad (32)$$

$$C_{DRP} = \frac{(R_{FB} + R_{FB1}) * C_{FB}}{R_{DRP}} \quad (33)$$

$R_{CP}$ and $C_{CP}$ have limited effect on the crossover frequency, and are used only to fine tune the crossover frequency and transient load response. Determine $R_{CP}$ and $C_{CP}$ from Equations (34) and (35).

$$R_{CP} = \frac{(2\pi * f_C)^2 * L_E * C_E * R_{FB} * V_{PWMRMP}}{V_O} \quad (34)$$

$$C_{CP} = \frac{10 * \sqrt{L_E * C_E}}{R_{CP}} \quad (35)$$

$C_{CP1}$ is optional and may be needed in some applications to reduce the jitter caused by the high frequency noise. A ceramic capacitor between 10pF and 220pF is usually enough.

**Type III Compensation for Non-AVP Applications**

Resistor $R_{FB}$ is chosen according to Equations (15), and resistor $R_{DRP}$ and capacitor $C_{DRP}$ are not needed. Choose the crossover frequency fc between 1/10 and 1/5 of the switching frequency per phase and select the desired phase margin θc. Calculate K factor from Equation (36), and determine the component values based on Equations (37) to (41),

$$K = \tan[\frac{\pi}{4} * (\frac{\theta_C}{180} + 1.5)] \quad (36)$$

$$R_{CP} = R_{FB} * \frac{(2\pi * \sqrt{L_E * C_E} * f_C)^2 * V_{PWMRMP}}{V_O * K} \quad (37)$$

$$C_{CP} = \frac{K}{2\pi * f_C * R_{CP}} \quad (38)$$

$$C_{CP1} = \frac{1}{2\pi * f_C * K * R_{CP}} \quad (39)$$

$$C_{FB} = \frac{K}{2\pi * f_C * R_{FB}} \quad (40)$$

$$R_{FB1} = \frac{1}{2\pi * f_C * K * C_{FB}} \quad (41)$$

**CURRENT SHARE LOOP COMPENSATION**

The crossover frequency of the current share loop should be at least one decade lower than that of the voltage loop in order to eliminate the interaction between the two loops. A capacitor from SCOMP to ground is usually enough for the share loop compensation. Choose the crossover frequency of current share loop ($f_{CI}$) based on the crossover frequency of voltage loop ($f_C$), and determine the $C_{SCOMP}$,

$$C_{SCOMP} = \frac{0.65 * R_{PWMRMP} * V_I * I_O * G_{CS\_ROOM} * R_{LE} * [1 + 2\pi * f_{CI} * C_E * (V_O / I_O)] * F_{MI}}{V_O * 2\pi * f_{CI} * 1.05 * 10^6} \quad (42)$$

Where $F_{MI}$ is the PWM gain in the current share loop,

$$F_{MI} = \frac{R_{PWMRMP} * C_{PWMRMP} * f_{SW} * V_{PWMRMP}}{(V_I - V_{PWMRMP} - V_{DAC}) * (V_I - V_{DAC})} \quad (43)$$

## DESIGN EXAMPLE 1 - VRM 10 2U CONVERTER

### SPECIFICATIONS

Input Voltage: $V_I$=12 V
DAC Voltage: $V_{DAC}$=1.35 V
No Load Output Voltage Offset: $V_{O\_NLOFST}$=20 mV
Output Current: $I_O$=105 ADC
Maximum Output Current: $I_{OMAX}$=120 ADC
Output Impedance: $R_O$=0.91 mΩ
VCC Ready to VCC Power Good Delay: $t_{VccPG}$=0-10mS
Soft Start Time: $t_{SS}$=2 mS
Over Current Delay: $t_{OCDEL}$=0.5mS
Dynamic VID Down-Slope Slew Rate: $SR_{DOWN}$=2.5mV/uS
Over Temperature Threshold: $T_{PCB}$=115 ºC

### POWER STAGE

Phase Number: n=6
Switching Frequency: $f_{SW}$=400 kHz
Output Inductors: L=220 nH, $R_L$=0.47 mΩ
Output Capacitors: AL-Polymer, C=560uF, $R_C$= 7mΩ, Number Cn=10

### IR3081PBF EXTERNAL COMPONENTS

#### Oscillator Resistor *Rosc*

Once the switching frequency is chosen, $R_{OSC}$ can be determined from the curve in Figure 13. For switching frequency of 400kHz per phase, choose $R_{OSC}$=30.1kΩ

#### Soft Start Capacitor *$C_{SS/DEL}$* and Resistor *$R_{SS/DEL}$*

Because faster over-current protection is required, the soft start capacitor $C_{SS/DEL}$ in series with the resistor $R_{SS/DEL}$ is used. Calculate the soft start capacitor from the required soft start time.

$$C_{SS/DEL} = \frac{I_{CHG} * t_{SS}}{V_O} = \frac{70*10^{-6} * 2*10^{-3}}{1.35 - 20*10^{-3}} = 0.1uF$$

Calculate the soft start resistor from the required over current delay time $t_{OCDEL}$,

$$R_{SS/DEL} = \frac{0.09 - \frac{t_{OCDEL} * I_{DISCHG}}{C_{SS/DEL}}}{I_{DISCHG}} = \frac{0.09 - \frac{0.5*10^{-3} * 6*10^{-6}}{0.1*10^{-6}}}{6*10^{-6}} = 10k\Omega$$

The soft start delay time is

$$t_{SSDEL} = \frac{C_{SS/DEL} * (1.3 - R_{SS/DEL} * I_{CHG})}{I_{CHG}} = \frac{0.1*10^{-6} * (1.3 - 10*10^{3} * 70*10^{-6})}{70*10^{-6}} = 0.86mS$$

The power good delay time is

$$t_{VccPG} = \frac{C_{SS/DEL} * (3.91 - V_O - 1.3)}{I_{CHG}} = \frac{0.1*10^{-6} * (3.91 - 1.33 - 1.3)}{70*10^{-6}} = 1.8ms$$

**VDAC Slew Rate Programming Capacitor *CVDAC* and Resistor *RVDAC***

From Figure 15, the sink current of VDAC pin corresponding to 400kHz (ROSC=30.1kΩ) is 76uA. Calculate the VDAC down-slope slew-rate programming capacitor from the required down-slope slew rate.

$$C_{VDAC} = \frac{I_{SINK}}{SR_{DOWN}} = \frac{76*10^{-6}}{2.5*10^{-3}/10^{-6}} = 30.4nF$$ , Choose CVDAC=33nF

Calculate the programming resistor.

$$R_{VDAC} = 0.5 + \frac{3.2*10^{-15}}{C_{VDAC}{}^2} = 0.5 + \frac{3.2*10^{-15}}{(33*10^{-9})^2} = 3.5\Omega$$

From Figure 15, the source current of VDAC pin is 110uA. The VDAC up-slope slew rate is

$$SR_{UP} = \frac{I_{SOURCE}}{C_{VDAC}} = \frac{110*10^{-6}}{33*10^{-9}} = 3.3mV/uS$$

**Over Current Setting Resistor *ROCSET***

The room temperature is 25ºC and the target PCB temperature is 100 ºC. The phase IC die temperature is about 1 ºC higher than that of phase IC, and the inductor temperature is close to PCB temperature.

Calculate Inductor DC resistance at 100 ºC,

$$R_{L\_MAX} = R_{L\_ROOM} * [1 + 3850*10^{-6} * (T_{L\_MAX} - T_{ROOM})] = 0.47*10^{-3} * [1 + 3850*10^{-6} * (100 - 25)] = 0.61m\Omega$$

The current sense amplifier gain is 34 at 25ºC, and its gain at 101ºC is calculated as,

$$G_{CS\_MIN} = G_{CS\_ROOM} * [1 - 1470*10^{-6} * (T_{IC\_MAX} - T_{ROOM})] = 34 * [1 - 1470*10^{-6} * (101 - 25)] = 30.2$$

Set the over current limit at 135A. From Figure 14, the bias current of OCSET pin (IOCSET) is 41uA with ROSC=30.1kΩ. The total current sense amplifier input offset voltage is 0.55mV, which includes the offset created by the current sense amplifier input resistor mismatch.

Calculate constant KP, the ratio of inductor peak current over average current in each phase,

$$K_P = \frac{(V_I - V_O) * V_O / (L * V_I * f_{SW} * 2)}{I_{LIMIT} / n} = \frac{(12 - 1.33) * 1.33 / (220*10^{-9} * 12 * 400*10^3 * 2)}{135/6} = 0.3$$

$$R_{OCSET} = [\frac{R_{LIMIT}}{n} * R_{L\_MAX} * (1 + K_P) + V_{CS\_TOFST}] * G_{CS\_MIN} / I_{OCSET}$$

$$= (\frac{135}{6} * 0.61*10^{-3} * 1.3 + 0.55*10^{-3}) * 30.2 / (41*10^{-6}) = 13.3k\Omega$$

**No Load Output Voltage Setting Resistor *RFB* and Adaptive Voltage Positioning Resistor *RDRP***

From Figure 14, the bias current of FB pin is 41uA with ROSC=30.1kΩ.

$$R_{FB} = \frac{R_{L\_MAX} * V_{O\_NLOFST} - V_{CS\_TOFST} * n * R_O}{I_{FB} * R_{L\_MAX}} = \frac{0.61*10^{-3} * 20*10^{-3} - 0.55*10^{-3} * 6 * 0.91*10^{-3}}{41*10^{-6} * 0.61*10^{-3}} = 365\Omega$$

$$R_{DRP} = \frac{R_{FB} * R_{L\_MAX} * G_{CS\_MIN}}{n * R_O} = \frac{365 * 0.61*10^{-3} * 30.2}{6 * 0.91*10^{-3}} = 1.21k\Omega$$

**Body Braking Related Resistors *RBBFB* and *RBBDRP***

N/A. The body braking during Dynamic VID is disabled.

**IR3086 EXTERNAL COMPONENTS**

**PWM Ramp Resistor *RPWMRMP* and Capacitor C*PWMRMP***

Set PWM ramp magnitude VPWMRMP=0.8V. Choose 220pF for PWM ramp capacitor CPWMRMP, and calculate the resistor RPWMRMP,

$$R_{PWMRMP} = \frac{V_O}{V_{IN} * f_{SW} * C_{PWMRMP} * [\ln(V_{IN} - V_{DAC}) - \ln(V_{IN} - V_{DAC} - V_{PWMRMP})]}$$

$$= \frac{1.33}{12 * 400 * 10^3 * 220 * 10^{-12} * [\ln(12 - 1.35) - \ln(12 - 1.35 - 0.8)]} = 16.1k\Omega$$ , choose RPWMRMP=16.2kΩ

**Inductor Current Sensing Capacitor *CCS+* and Resistors *RCS+* and *RCS-***

Choose CCS+=47nF, and calculate RCS+,

$$R_{CS+} = \frac{L/R_L}{C_{CS+}} = \frac{220 * 10^{-9} / (0.47 * 10^{-3})}{47 * 10^{-9}} = 10.0k\Omega$$

The bias currents of CSIN+ and CSIN- are 0.25uA and 0.4uA respectively. Calculate resistor RCS-,

$$R_{CS-} = \frac{0.25}{0.4} * R_{CS+} = \frac{0.25}{0.4} * 10.0 * 10^3 = 6.2k\Omega$$ , choose RCS-=6.19kΩ

**Over Temperature Setting Resistors *RHOTSET1* and *RHOTSET2***

Use central over-temperature setting and set the temperature threshold at 115 ºC, which corresponds to the IC die temperature of 116 ºC. Calculate the HOTSET threshold voltage corresponding to the temperature thresholds.

$$V_{HOTSET} = 4.73 * 10^{-3} * T_J + 1.241 = 4.73 * 10^{-3} * 116 + 1.241 = 1.79V$$

Pre-select RHOTSET1=10.0kΩ,

$$R_{HOTSET2} = \frac{R_{HOTSET1} * V_{HOTSET}}{V_{BIAS} - V_{HOTSET}} = \frac{10 * 10^3 * 1.79}{6.8 - 1.79} = 3.57k\Omega$$

**Phase Delay Timing Resistors *RPHASE1* and *RPHASE2***

Use central over-temperature setting and set the temperature threshold at 115 ºC, which corresponds to the IC die temperature of 116 ºC. Calculate the HOTSET threshold voltage corresponding to the temperature thresholds.

The phase delay resistor ratios for phases 1 to 6 at 400kHz of switching frequencies are RAPHASE1=0.628, RAPHASE2=0.415, RAPHASE3=0.202, RAPHASE4=0.246, RAPHASE5=0.441 and RAPHASE6=0.637 starting from down-slope. Pre-select RPHASE11=RPHASE21=RPHASE31=RPHASE41=RPHASE51= RPHASE61=10kΩ,

$$R_{PHASE12} = \frac{RA_{PHASE1}}{1 - RA_{PHASE1}} * R_{PHASE11} = \frac{0.628}{1 - 0.628} * 10 * 10^3 = 16.9k\Omega$$

RPHASE22=7.15kΩ, RPHASE32=2.55kΩ, RPHASE42=3.24kΩ, PPHASE52=7.87kΩ, RPHASE62=17.4kΩ

**Bootstrap Capacitor CBST**

Choose CBST=0.1uF

**Decoupling Capacitors for Phase IC and Power Stage**

Choose CVCC=0.1uF, CVCCL=0.1uF

**VOLTAGE LOOP COMPENSATION**

Type II compensation is used for the converter with AL-Polymer output capacitors. Choose the crossover frequency fc=40kHz, which is 1/10 of the switching frequency per phase, and determine Rcp and CCP.

$$R_{CP} = \frac{(2\pi * f_C)^2 * L_E * C_E * R_{FB} * V_{RAMP}}{V_O * \sqrt{1+(2\pi * f_C * C * R_C)^2}} = \frac{(2\pi * 40 * 10^3)^2 * (220 * 10^{-9}/6) * (560 * 10^{-6} * 10) * 365 * 0.8}{(1.35 - 20 * 10^{-3}) * \sqrt{1+(2\pi * 40 * 10^3 * 560 * 10^{-6} * 7 * 10^{-3})^2}} = 2.0k\Omega$$

$$C_{CP} = \frac{10 * \sqrt{L_E * C_E}}{R_{CP}} = \frac{10 * \sqrt{(220 * 10^{-9}/6) * (560 * 10^{-6} * 10)}}{2.0 * 10^3} = 71nF$$ , Choose CCP=68nF

Choose CCP1=47pF to reduce high frequency noise.

**CURRENT SHARE LOOP COMPENSATION**

The crossover frequency of the current share loop fCI should be at least one decade lower than that of the voltage loop fC. Choose the crossover frequency of current share loop fCI=4kHz, and calculate CSCOMP,

$$F_{MI} = \frac{R_{PWMRMP} * C_{PWMRMP} * f_{SW} * V_{PWMRMP}}{(V_I - V_{PWMRMP} - V_{DAC}) * (V_I - V_{DAC})} = \frac{16.2 * 10^3 * 220 * 10^{-12} * 400 * 10^3 * 0.8}{(12 - 0.8 - 1.35) * (12 - 1.35)} = 0.011$$

$$C_{SCOMP} = \frac{0.65 * R_{PWMRMP} * V_I * I_O * G_{CS\_ROOM} * R_{LE} * [1 + 2\pi * f_{CI} * C_E * (V_O / I_O)] * F_{MI}}{V_O * 2\pi * f_{CI} * 1.05 * 10^6}$$

$$= \frac{0.65 * 16.2 * 10^3 * 12 * 105 * 34 * (0.47 * 10^{-3}/6) * [1 + 2\pi * 4 * 10^3 * 560 * 10^{-6} * 10 * (1.33 - 105 * 9.1 * 10^{-4})/105] * 0.011}{(1.33 - 105 * 9.1 * 10^{-4}) * 2\pi * 4 * 10^3 * 1.05 * 10^6}$$

$$= 31.4nF$$

Choose CSCOMP=33nF.

## DESIGN EXAMPLE 2 - EVRD 10 HIGH FREQUENCY ALL-CERAMIC CONVERTER

### SPECIFICATIONS

Input Voltage: $V_I$=12 V
DAC Voltage: $V_{DAC}$=1.3 V
No Load Output Voltage Offset: $V_{O\_NLOFST}$=20 mV
Output Current: $I_O$=105 ADC
Maximum Output Current: $I_{OMAX}$=120 ADC
Output Impedance: $R_O$=0.91 mΩ
VCC Ready to VCC Power Good Delay: $t_{VccPG}$=0-10mS
Soft Start Time: $t_{SS}$=2.9mS
Over Current Delay: $t_{OCDEL}$=2.1mS
Dynamic VID Down-Slope Slew Rate: $SR_{DOWN}$=2.5mV/uS
Over Temperature Threshold: $T_{PCB}$=115 ºC

### POWER STAGE

Phase Number: n=6
Switching Frequency: $f_{SW}$=800 kHz
Output Inductors: L=100 nH, $R_L$=0.5 mΩ
Output Capacitors: Ceramic, C=22uF, $R_C$= 2mΩ, Number Cn=62

### IR3081PBF EXTERNAL COMPONENTS

#### Oscillator Resistor *Rosc*

Once the switching frequency is chosen, $R_{OSC}$ can be determined from the curve in Figure 13 data sheet. For switching frequency of 800kHz per phase, choose $R_{OSC}$=13.3kΩ

#### Soft Start Capacitor $C_{SS/DEL}$ and Resistor $R_{SS/DEL}$

Because faster over-current protection is required, the soft start capacitor $C_{SS/DEL}$ in series with the resistor $R_{SS/DEL}$ is used. Calculate the soft start capacitor from the required soft start time.

$$C_{SS/DEL} = \frac{I_{CHG} * t_{SS}}{V_O} = \frac{70*10^{-6} * 2.9*10^{-3}}{1.3 - 20*10^{-3}} = 0.16uF$$ , choose $C_{SS/DEL}$=0.15uF

Calculate the soft start resistor from the required over current delay time $t_{OCDEL}$,

$$R_{SS/DEL} = \frac{0.09 - \frac{t_{OCDEL} * I_{DISCHG}}{C_{SS/DEL}}}{I_{DISCHG}} = \frac{0.09 - \frac{2.1*10^{-3} * 6*10^{-6}}{0.15*10^{-6}}}{6*10^{-6}} = 1k\Omega$$

The soft start delay time is

$$t_{SSDEL} = \frac{C_{SS/DEL} * (1.3 - R_{SS/DEL} * I_{CHG})}{I_{CHG}} = \frac{0.15*10^{-6} * (1.3 - 1*10^{3} * 70*10^{-6})}{70*10^{-6}} = 2.6mS$$

The power good delay time is

$$t_{VccPG} = \frac{C_{SS/DEL} * (3.91 - V_O - 1.3)}{I_{CHG}} = \frac{0.15*10^{-6} * (3.91 - 1.28 - 1.3)}{70*10^{-6}} = 2.85ms$$

**VDAC Slew Rate Programming Capacitor *CVDAC* and Resistor *RVDAC***

From Figure 15, the sink current of VDAC pin corresponding to 800kHz ($R_{OSC}$=13.3kΩ) is 170uA. Calculate the VDAC down-slope slew-rate programming capacitor from the required down-slope slew rate.

$$C_{VDAC} = \frac{I_{SINK}}{SR_{DOWN}} = \frac{170*10^{-6}}{2.5*10^{-3}/10^{-6}} = 68nF$$

Calculate the programming resistor.

$$R_{VDAC} = 0.5 + \frac{3.2*10^{-15}}{C_{VDAC}{}^2} = 0.5 + \frac{3.2*10^{-15}}{(68*10^{-9})^2} = 1.2\Omega$$

From Figure 15, the source current of VDAC pin is 250uA. The VDAC up-slope slew rate is

$$SR_{UP} = \frac{I_{SOURCE}}{C_{VDAC}} = \frac{250*10^{-6}}{68*10^{-9}} = 3.7mV/uS$$

**Over Current Setting Resistor *ROCSET***

The room temperature is 25ºC and the target PCB temperature is 100 ºC. The phase IC die temperature is about 1 ºC higher than that of phase IC, and the inductor temperature is close to PCB temperature.

Calculate Inductor DC resistance at 100 ºC,

$$R_{L\_MAX} = R_{L\_ROOM} * [1 + 3850*10^{-6} * (T_{L\_MAX} - T_{ROOM})] = 0.5*10^{-3} * [1 + 3850*10^{-6} * (100 - 25)] = 0.64m\Omega$$

The current sense amplifier gain is 34 at 25ºC, and its gain at 101ºC is calculated as,

$$G_{CS\_MIN} = G_{CS\_ROOM} * [1 - 1470*10^{-6} * (T_{IC\_MAX} - T_{ROOM})] = 34 * [1 - 1470*10^{-6} * (101 - 25)] = 30.2$$

Set the over current limit at 135A. From Figure 14, the bias current of OCSET pin ($I_{OCSET}$) is 90uA with $R_{OSC}$=13.3kΩ. The total current sense amplifier input offset voltage is 0.55mV, which includes the offset created by the current sense amplifier input resistor mismatch.

Calculate constant $K_P$, the ratio of inductor peak current over average current in each phase,

$$K_P = \frac{(V_I - V_O) * V_O / (L * V_I * f_{SW} * 2)}{I_{LIMIT}/n} = \frac{(12 - 1.28) * 1.28 / (100*10^{-9} * 12 * 800 * 10^3 * 2)}{135/6} = 0.32$$

$$R_{OCSET} = [\frac{R_{LIMIT}}{n} * R_{L\_MAX} * (1 + K_P) + V_{CS\_TOFST}] * G_{CS\_MIN} / I_{OCSET}$$

$$= (\frac{135}{6} * 0.64*10^{-3} * 1.32 + 0.55*10^{-3}) * 30.2 / (90*10^{-6}) = 6.34k\Omega$$

**No Load Output Voltage Setting Resistor *RFB* and Adaptive Voltage Positioning Resistor *RDRP***

From Figure 14, the bias current of FB pin is 90uA with $R_{OSC}$=13.3kΩ.

$$R_{FB} = \frac{R_{L\_MAX} * V_{O\_NLOFST} - V_{CS\_TOFST} * n * R_O}{I_{FB} * R_{L\_MAX}} = \frac{0.64*10^{-3} * 20*10^{-3} - 0.55*10^{-3} * 6 * 0.91*10^{-3}}{90*10^{-6} * 0.64*10^{-3}} = 162\Omega$$

$$R_{DRP} = \frac{R_{FB} * R_{L\_MAX} * G_{CS\_MIN}}{n * R_O} = \frac{162 * 0.64*10^{-3} * 30.2}{6 * 0.91*10^{-3}} = 576\Omega$$

**Body Braking Related Resistors *RBBFB* and *RBBDRP***

N/A. The body braking during Dynamic VID is disabled.

**IR3086 EXTERNAL COMPONENTS**

**PWM Ramp Resistor *RPWMRMP* and Capacitor C*PWMRMP***

Set PWM ramp magnitude VPWMRMP=0.75V. Choose 100pF for PWM ramp capacitor CPWMRMP, and calculate the resistor RPWMRMP,

$$R_{PWMRMP} = \frac{V_O}{V_{IN} * f_{SW} * C_{PWMRMP} * [\ln(V_{IN} - V_{DAC}) - \ln(V_{IN} - V_{DAC} - V_{PWMRMP})]}$$

$$= \frac{1.28}{12 * 800 * 10^3 * 100 * 10^{-12} * [\ln(12 - 1.3) - \ln(12 - 1.3 - 0.75)]} = 18.2k\Omega$$

**Inductor Current Sensing Capacitor *CCS+* and Resistors *RCS+* and *RCS-***

Choose 47nF for capacitor CCS+, and calculate RCS+,

$$R_{CS+} = \frac{L/R_L}{C_{CS+}} = \frac{100 * 10^{-9} / (0.5 * 10^{-3})}{47 * 10^{-9}} = 4.22k\Omega$$

The bias currents of CSIN+ and CSIN- are 0.25uA and 0.4uA respectively. Calculate resistor RCS-,

$$R_{CS-} = \frac{0.25}{0.4} * R_{CS+} = \frac{0.25}{0.4} * 4.22 * 10^3 = 2.61k\Omega$$

**Combined Over Temperature and Phase Delay Setting Resistors *RPHASEx1*, *RPHASEx2* and *RPHASEx3***

The over temperature setting resistor divider is combined with the phase delay resistor divider. Set the temperature threshold at 115 ºC, which corresponds to the IC die temperature of 116 ºC, and calculate the HOTSET threshold voltage corresponding to the temperature thresholds.

$$V_{HOTSET} = 4.73 * 10^{-3} * T_J + 1.241 = 4.73 * 10^{-3} * 116 + 1.241 = 1.79V$$

The phase delay resistor ratios for phases 1 to 6 at 800kHz of switching frequencies are RAPHASE1=0.665, RAPHASE2=0.432, RAPHASE3=0.198, RAPHASE4=0.206, RAPHASE5=0.401 and RAPHASE6=0.597 starting from down-slope.

The over temperature setting voltage of phases 1, 2, 5, and 6 is lower than the phase delay setting voltage, VBIAS*RAPHASEx. Pre-select RPHASE11=10kΩ,

$$R_{PHASEx2} = \frac{(RA_{PHASEx} * V_{BIAS} - V_{HOTSET}) * R_{PHASEx1}}{V_{BIAS} * (1 - RA_{PHASEx})} = \frac{(0.665 * 6.8 - 1.79) * 10 * 10^3}{6.8 * (1 - 0.665)} = 12.1k\Omega$$

$$R_{PHASEx3} = \frac{V_{HOTSET} * R_{PHASEx1}}{V_{BIAS} * (1 - RA_{PHASEx})} = \frac{1.79 * 12.1 * 10^3}{6.8 * (1 - 0.665)} = 7.87k\Omega$$

RPHASE21=10kΩ, RPHASE22=2.94kΩ, RPHASE23=4.64kΩ

RPHASE51=10kΩ, RPHASE52=2.32kΩ, RPHASE53=4.42kΩ

RPHASE61=10kΩ, RPHASE62=8.25kΩ, RPHASE63=6.49kΩ

The over temperature setting voltage of Phases 3 and 4 is higher than the phase delay setting voltage, VBIAS*RAPHASEx. Pre-select RPHASEX1=10kΩ,

$$R_{PHASE32} = \frac{(V_{HOTSET} - RA_{PHASE3} * V_{BIAS}) * R_{PHASE31}}{V_{BIAS} - V_{HOTSET}} = \frac{(1.79 - 0.198 * 6.8) * 10 * 10^3}{6.8 - 1.79} = 887\Omega$$

$$R_{PHASE33} = \frac{RA_{PHASE3} * V_{BIAS} * R_{PHASE31}}{V_{BIAS} - V_{HOTSET}} = \frac{0.198 * 6.8 * 10 * 10^3}{6.8 - 1.79} = 2.67k\Omega$$

RPHASE41=10kΩ, RPHASE42=768Ω, RPHASE43=2.80kΩ

**Bootstrap Capacitor *CBST***

Choose CBST=0.1uF

**Decoupling Capacitors for Phase IC and Power Stage**
Choose CVCC=0.1uF, CVCCL=0.1uF

**VOLTAGE LOOP COMPENSATION**

Type III compensation is used for the converter with only ceramic output capacitors. The crossover frequency and phase margin of the voltage loop can be estimated as follows.

$$f_{C1} = \frac{R_{DRP}}{2\pi * C_E * G_{CS} * R_{FB} * R_{LE}} = \frac{576}{2\pi * (62 * 22 * 10^{-6}) * 34 * 162 * (0.5 * 10^{-3} / 6)} = 146kHz$$

$$\theta_{C1} = 90 - A\tan(0.5) * \frac{180}{\pi} = 63°$$

Choose $R_{FB1} = \frac{2}{3} * R_{FB} = \frac{2}{3} * 162 = 110\Omega$

Choose the desired crossover frequency fc (=140kHz) around fc1 estimated above, and calculate

$$C_{FB} = \frac{1}{4\pi * f_C * R_{FB1}} = \frac{1}{4\pi * 140 * 10^3 * 110} = 5.2nF$$ , choose CFB=5.6nF

$$C_{DRP} = \frac{(R_{FB} + R_{FB1}) * C_{FB}}{R_{DRP}} = \frac{(162 + 110) * 5.6 * 10^{-9}}{576} = 2.7nF$$

$$R_{CP} = \frac{(2\pi * f_C)^2 * L_E * C_E * R_{FB} * V_{RAMP}}{V_O} = \frac{(2\pi * 140 * 10^3)^2 * (100 * 10^{-9} / 6) * (22 * 10^{-6} * 62) * 162 * 0.75}{1.3 - 20 * 10^{-3}} = 1.65k\Omega$$

$$C_{CP} = \frac{10 * \sqrt{L_E * C_E}}{R_{CP}} = \frac{10 * \sqrt{(100 * 10^{-9} / 6) * (22 * 10^{-6} * 62)}}{1.65 * 10^3} = 27nF$$

Choose CCP1=47pF to reduce high frequency noise.

**CURRENT SHARE LOOP COMPENSATION**

The crossover frequency of the current share loop fCI should be at least one decade lower than that of the voltage loop fC. Choose the crossover frequency of current share loop fCI=3.5kHz, and calculate CSCOMP,

$$F_{MI} = \frac{R_{PWMRMP} * C_{PWMRMP} * f_{SW} * V_{PWMRMP}}{(V_I - V_{PWMRMP} - V_{DAC}) * (V_I - V_{DAC})} = \frac{18.2 * 10^3 * 100 * 10^{-12} * 800 * 10^3 * 0.75}{(12 - 0.75 - 1.3) * (12 - 1.3)} = 0.011$$

$$C_{SCOMP} = \frac{0.65 * R_{PWMRMP} * V_I * I_O * G_{CS\_ROOM} * R_{LE} * [1 + 2\pi * f_{CI} * C_E * (V_O / I_O)] * F_{MI}}{V_O * 2\pi * f_{CI} * 1.05 * 10^6}$$

$$= \frac{0.65 * 18.2 * 10^3 * 12 * 105 * 34 * (0.5 * 10^{-3} / 6) * [1 + 2\pi * 3500 * 22 * 10^{-6} * 62 * (1.33 - 105 * 9.1 * 10^{-4}) / 105] * 0.011}{(1.33 - 105 * 9.1 * 10^{-4}) * 2\pi * 3500 * 1.05 * 10^6}$$

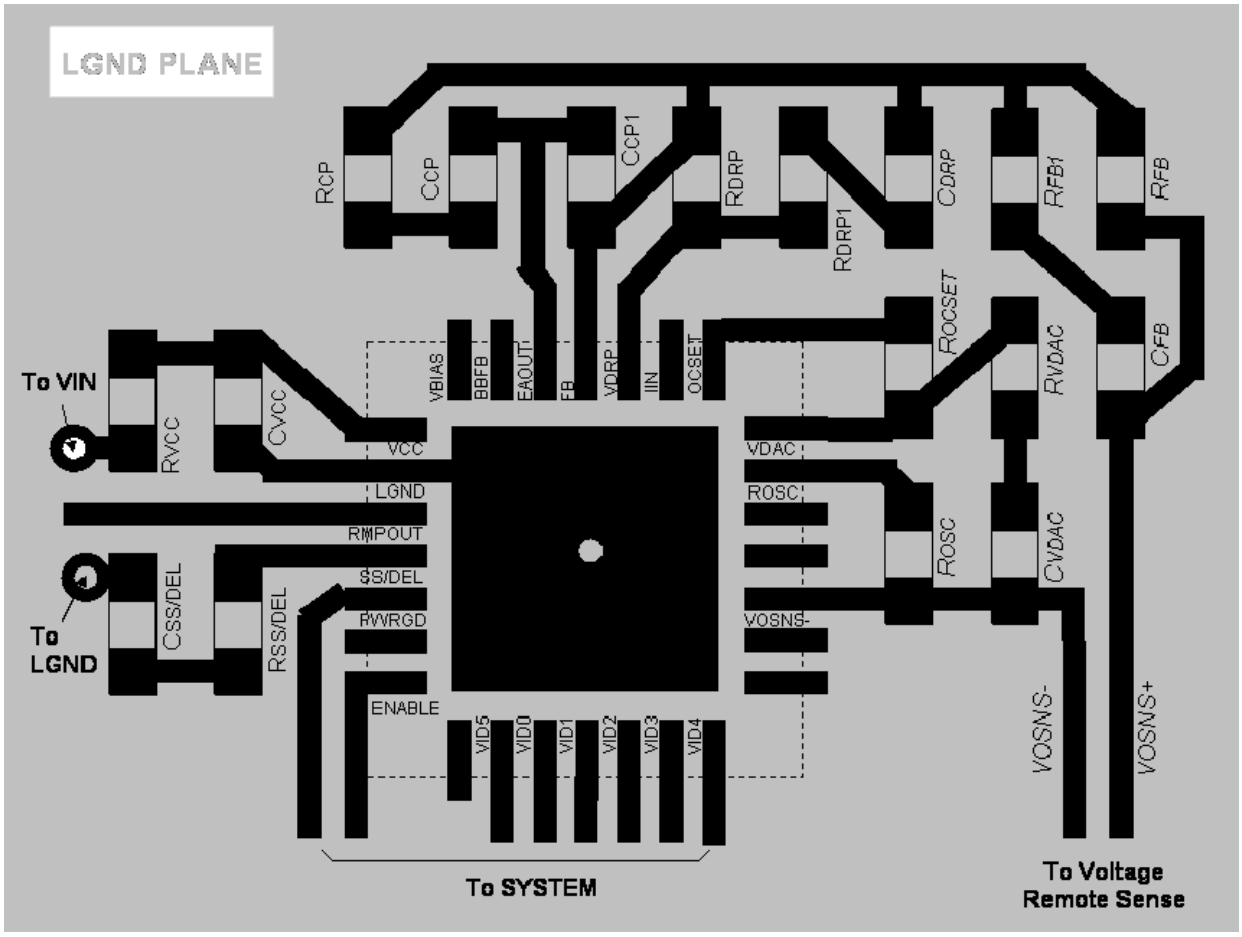
$$= 20.6nF$$

Choose CSCOMP=22nF

## LAYOUT GUIDELINES

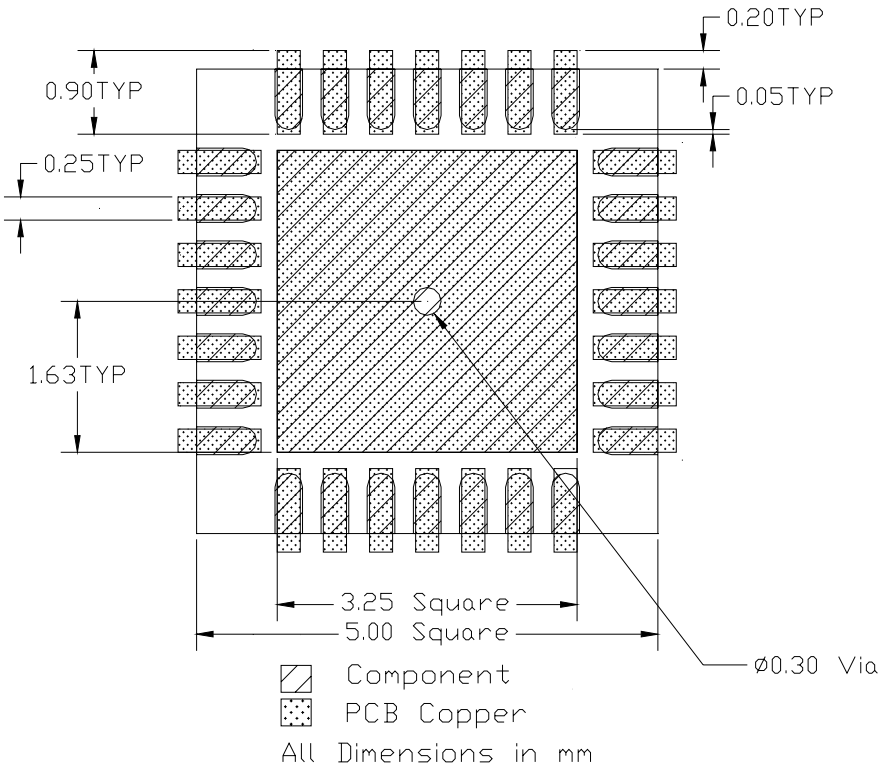
The following layout guidelines are recommended to reduce the parasitic inductance and resistance of the PCB layout, therefore minimizing the noise coupled to the IC.

- Dedicate at least one middle layer for a ground plane LGND.
- Connect the ground tab under the control IC to LGND plane through a via.
- Place the following critical components on the same layer as control IC and position them as close as possible to the respective pins, ROSC, ROCSET, RVDAC, CVDAC, CVCC, CSS/DEL and RCC/DEL. Avoid using any via for the connection.
- Place the compensation components on the same layer as control IC and position them as close as possible to EAOUT, FB and VDRP pins. Avoid using any via for the connection.
- Use Kelvin connections for the remote voltage sense signals, VOSNS+ and VOSNS-, and avoid crossing over the fast transition nodes, i.e. switching nodes, gate drive signals and bootstrap nodes.
- Control bus signals, VDAC, RMPOUT, IIN, VBIAS, and especially EAOUT, should not cross over the fast transition nodes.



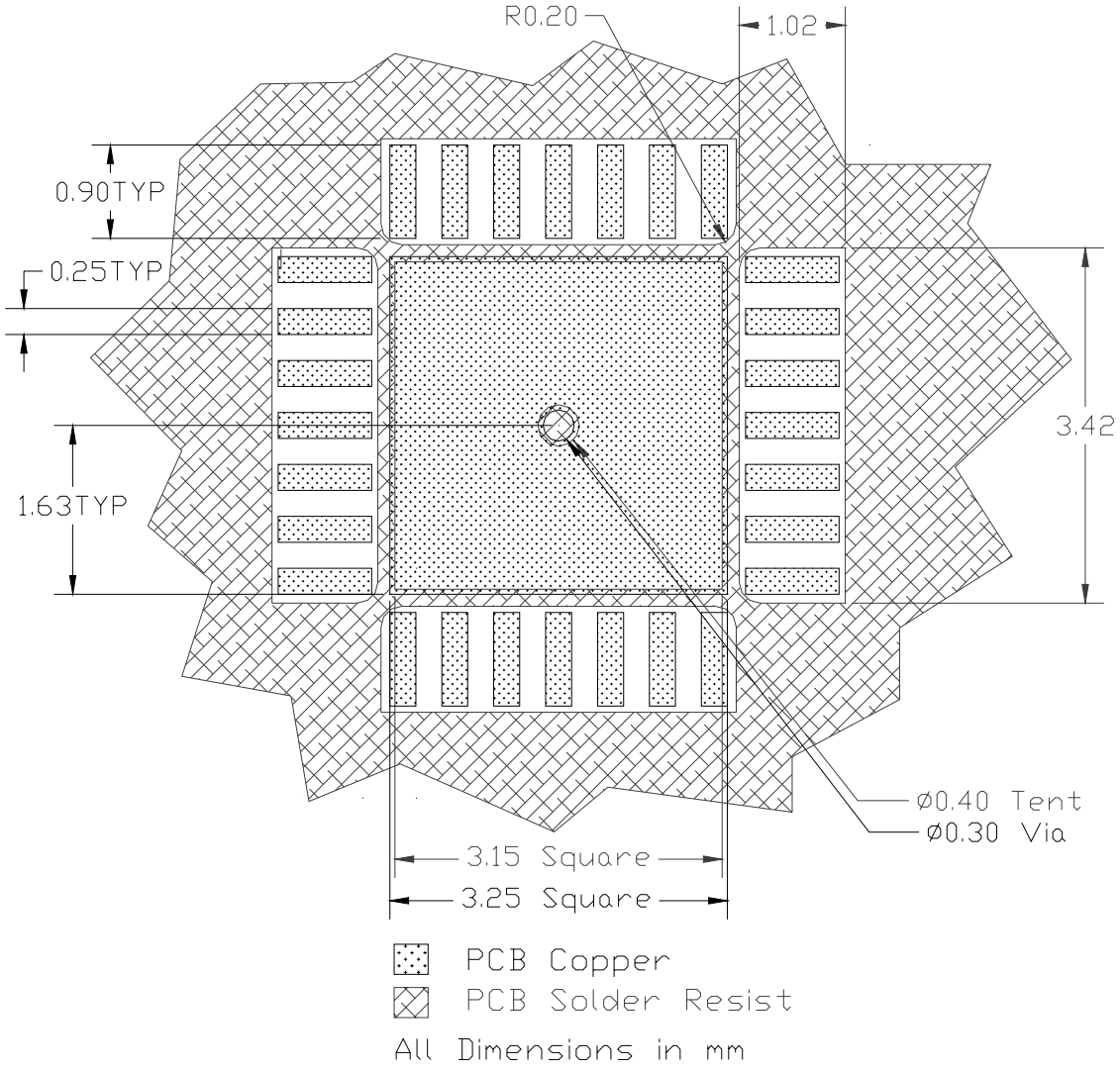
**PCB Metal and Component Placement**

- Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to minimize shorting.
- Lead land length should be equal to maximum part lead length + 0.2 mm outboard extension + 0.05mm inboard extension. The outboard extension ensures a large and inspectable toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
- Center pad land length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be ≥ 0.17mm for 2 oz. Copper (≥ 0.1mm for 1 oz. Copper and ≥ 0.23mm for 3 oz. Copper)
- A single 0.30mm diameter via shall be placed in the center of the pad land and connected to ground to minimize the noise effect on the IC.



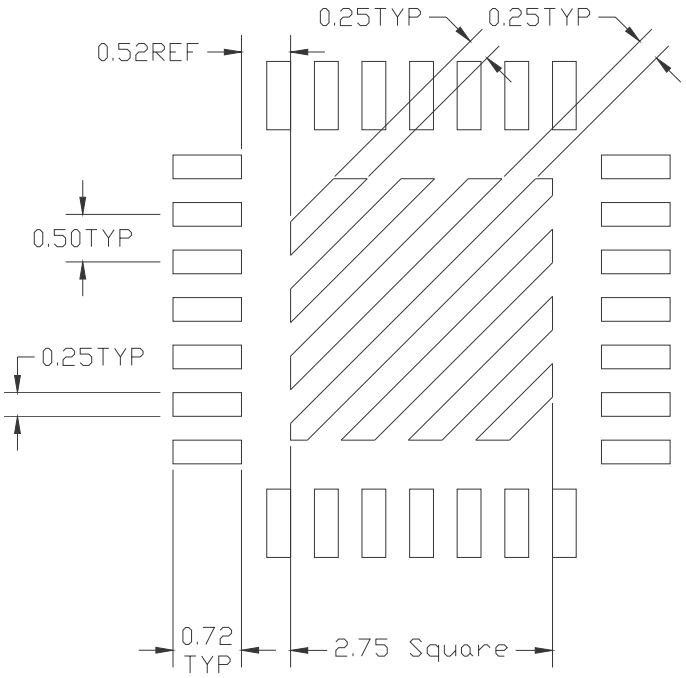
**Solder Resist**

- The solder resist should be pulled away from the metal lead lands by a minimum of 0.06mm. The solder resist mis-alignment is a maximum of 0.05mm and it is recommended that the lead lands are all Non Solder Mask Defined (NSMD). Therefore pulling the S/R 0.06mm will always ensure NSMD pads.
- The minimum solder resist width is 0.13mm, therefore it is recommended that the solder resist is completely removed from between the lead lands forming a single opening for each “group” of lead lands.
- At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of ≥ 0.17mm remains.
- The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.06mm to accommodate solder resist mis-alignment. In 0.5mm pitch cases it is allowable to have the solder resist opening for the land pad to be smaller than the part pad.
- Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.
- The single via in the land pad should be tented with solder resist 0.4mm diameter, or 0.1mm larger than the diameter of the via.



**Stencil Design**

- The stencil apertures for the lead lands should be approximately 80% of the area of the lead lands. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The stencil lead land apertures should therefore be shortened in length by 80% and centered on the lead land.
- The land pad aperture should be striped with 0.25mm wide openings and spaces to deposit approximately 50% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.




Stencil Aperture

All Dimensions in mm

## PERFORMANCE CHARACTERISTICS

Figure 13 - Oscillator Frequency versus ROSC

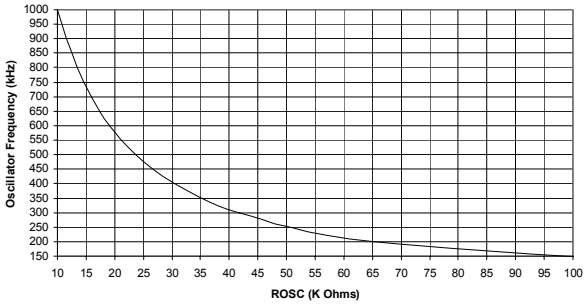



Figure 14 - IFB, BBFB, & OCSET Bias Currents vs ROSC

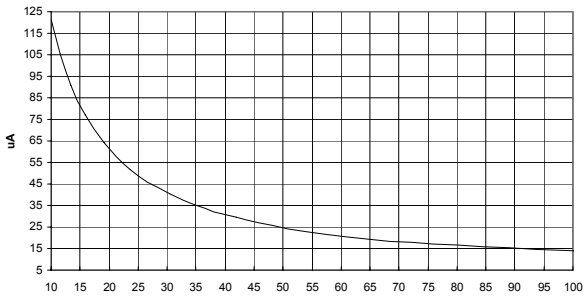



Figure 15 - VDAC Source & Sink Currents vc ROSC (includes OCSET Bias Current)

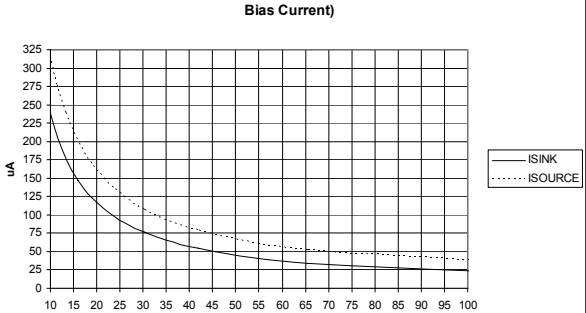
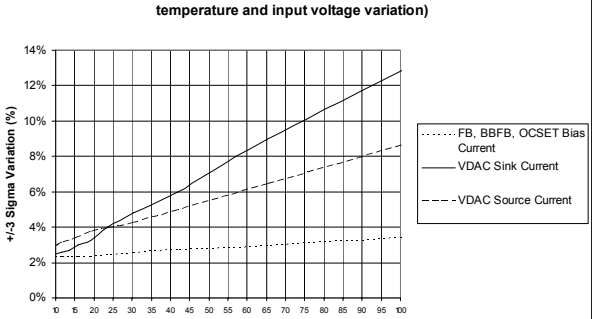
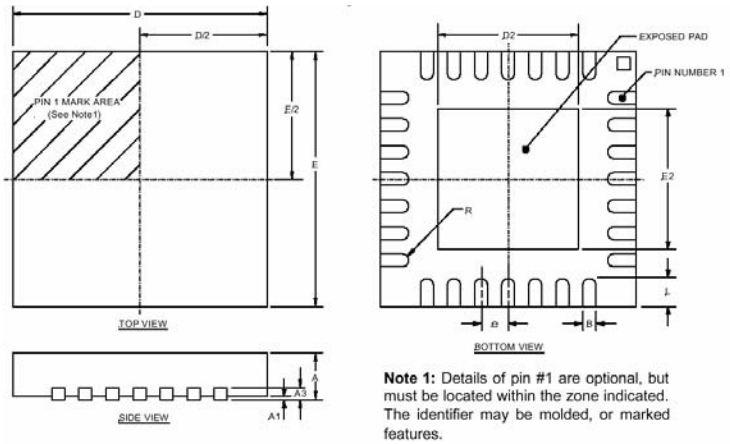



Figure 16 - Bias Current Accuracy versus ROsC (includes temperature and input voltage variation)



## PACKAGE INFORMATION

**28L MLPQ (5 x 5 mm Body) – $\theta_{JA}$ = 30°C/W, $\theta_{JC}$ = 3°C/W**




**Note 1:** Details of pin #1 are optional, but must be located within the zone indicated. The identifier may be molded, or marked features.

| SYMBOL | 28-PIN 5x5 | | |
|---|---|---|---|
| DESIG | MIN | NOM | MAX |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20 REF | |
| B | 0.18 | 0.23 | 0.30 |
| D | | 5.00 BSC | |
| D2 | 3.00 | 3.15 | 3.25 |
| E | | 5.00 BSC | |
| E2 | 3.00 | 3.15 | 3.25 |
| e | | 0.50 BSC | |
| L | 0.45 | 0.55 | 0.65 |
| R | 0.09 | --- | --- |

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.



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