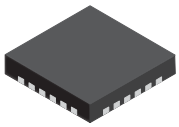
Multiple-Output Regulator for Automotive LCD Displays

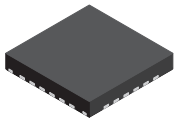
FEATURES AND BENEFITS

- Automotive-grade AEC-Q100 qualified
- Input voltage from 3 to 10 V
- Four individual output supplies
- Independent control of each output voltage
- Boost switching frequency: 350 kHz to 2.25 MHz
- External synchronization capability is available
- Frequency dithering to reduce EMI
- Less than 10 µA shutdown current
- Protection features: overcurrent, overvoltage, short circuit, and thermal overload protection
- Fully programmable outputs through I²C
  - □ Regulator voltage
  - □ Startup/shutdown sequences
  - □ Fault retry counter

PACKAGES:



24-Pin 4 mm × 4 mm QFN with Sidewall Plating



24-Pin 4 mm × 4 mm QFN with Wettable Flank

Not to scale

DESCRIPTION

The A8603 is a fixed-frequency, multiple-output supply for LCD bias. Its switching frequency can be either programmed or synchronized with an external clock signal between 350 kHz and 2.25 MHz. This will minimize interference with AM and FM radio bands.

An I²C-compliant serial interface allows a system microcontroller to configure the A8603 by writing into its internal registers. A system controller can also access the A8603 status registers in case of fault conditions.

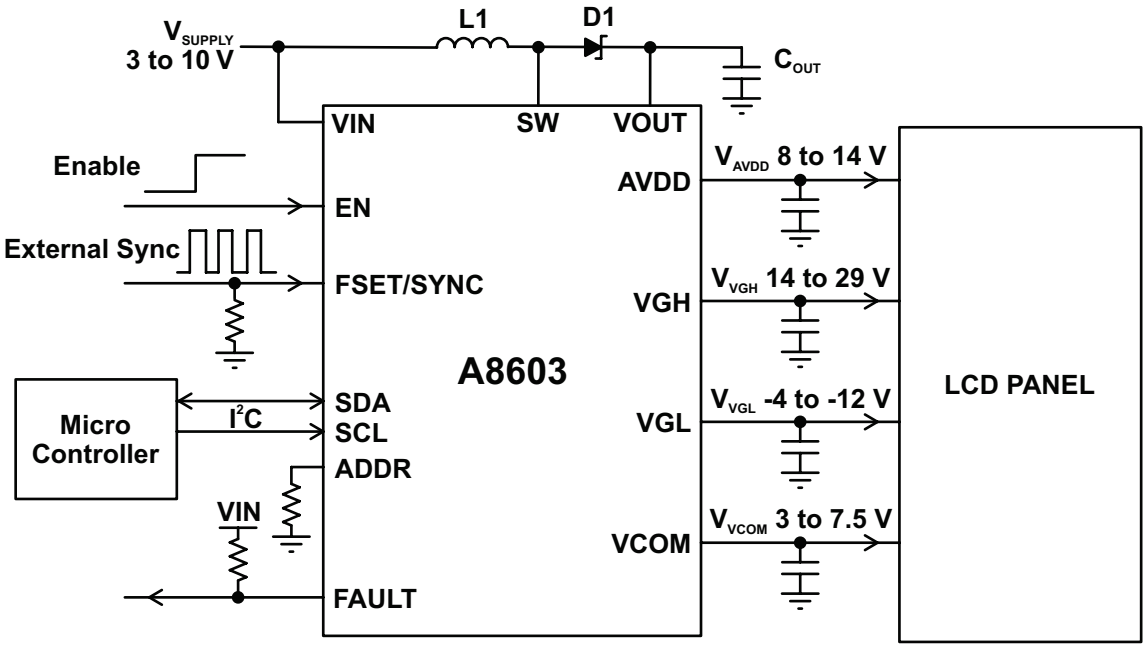
The A8603 incorporates a boost stage followed by two linear regulators and two charge-pump regulators. Each output voltage can be programmed independently through serial interface. During power-up and shutdown, the outputs are turned on and off in preprogrammed sequences with adjustable delay. This will meet the sequencing requirements for specific LCD panels.

Short-circuit protection is provided for all outputs. The boost switch is protected against overcurrent and overvoltage.

The A8603 is provided in a 24-pin 4 mm × 4 mm QFN package, with exposed thermal pad to allow operation at high ambient temperatures. It is lead (Pb) free with 100% matte-tin leadframe plating.

APPLICATIONS

- GPS
- Infotainment
- Medium LCDs



System Block Diagram Showing Typical Regulator Voltages

Table 1: Selection Guide

Part Number	Package	Packing*	Pin Soldering
A8603KESTR-R	24-pin 4×4 QFN with exposed thermal pad	1500 pieces per 13-in. reel	Sidewall Plating
A8603KESTR-J	24-pin 4×4 QFN with exposed thermal pad	Contact Factory	Wettable Flank

*Contact Allegro™ for additional packing options.

Table of Contents

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS [1][2][5]

Characteristic	Symbol	Notes	Rating	Unit
VIN Pin Voltage	V_{IN}	All voltages measured with respect to GND	–0.3 to 11	V
SW Pin Voltage [3][4]	V_{SW}	Continuous	–0.6 to 22	V
		Voltage spikes (pulse width < 100 ns)	–1 to 40	V
OUT Pin Voltage	V_{OUT}		–0.3 to 22	V
AVDD Pin Voltage	V_{AVDD}		–0.3 to lower of 16 or V_{OUT} + 0.3	V
CP11 Pin Voltage	V_{CP11}	Positive charge pump	–0.3 to 31	V
CP12 Pin Voltage	V_{CP12}	Positive charge pump	–0.3 to V_{CP11} + 0.3	V
VGH and VGH3 Pin Voltage	V_{VGH}, V_{VGH3}	Positive charge pump	–0.3 to 31	V
CP21 Pin Voltage	V_{CP21}	Negative charge pump	–0.3 to 14	V
CP22 and VGL Pin Voltage	V_{CP22}, V_{VGL}	Negative charge pump	–14 to 0.3	V
FAULT Pin Voltage	V_{FAULT}		–0.3 to lower of 10 or V_{VIN} + 0.3	V
BIAS, COMP, FSET Pin Voltage	V_{BIAS}, V_{COMP}, V_{FSET}		–0.3 to 3.3	V
VCOM Pin Voltage	V_{VCOM}		–0.3 to lower of 8.5 or V_{AVDD} + 0.3	V
AGND, PGND and GNDVCOM Pin Voltage	V_{AGND}, V_{PGND}, $V_{GNDVCOM}$		–0.3 to 0.3	V
Logic Pins (EN, SCL, SDA, ADDR, NC)	–		–0.3 to 5.5	V
Operating Ambient Temperature	T_A	K temperature range	–40 to 125	°C
Maximum Junction Temperature	$T_{J(max)}$		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

[1] Stresses beyond those listed in this table may cause permanent damage to the device. The Absolute Maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to Absolute Maximum-rated conditions for extended periods may affect device reliability.
[2] All voltages referenced to AGND.
[3] The SW pin has internal clamp diodes to GND. Applications that forward bias this diode should take care not to exceed the IC package power dissipation limits. Note: Exact energy specification to be determined.
[4] The switch DMOS is self-protected. If voltage spikes exceeding 40 V are applied, the device would conduct and absorb the energy safely.
[5] When V_{IN} = 0 (no power), all inputs are limited by –0.3 to 5.5 V.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [6]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Package ES on 4-layer PCB based on JEDEC standard	37	°C/W

[6] Additional thermal information available on the Allegro website.

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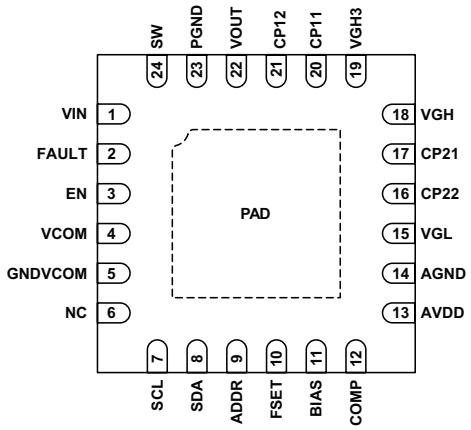
PINOUT DIAGRAMS AND TERMINAL LIST TABLE



Package ES, 24-Pin QFN Pinouts

Terminal List Table

Number	Name	Function
1	VIN	Input supply voltage (3 to 10 V) for the IC
2	FAULT	Open-drain output, pulls low in case of error condition
3	EN	Enable pin for enabling the IC; system can only be enabled after V_{IN} is above UVLO level (refer to Startup Timing Diagram)
4	VCOM	Output from internal low-dropout (LDO) regulator (item 2 in Functional Block Diagram) powered by AVDD
5	GNDVCOM	Ground reference for VCOM; connect to ground plane
6	NC	No Connect (reserved for Test Mode); connect to GND in actual PCB
7	SCL	I²C clock signal
8	SDA	I²C data signal
9	ADDR	I²C address selection (up to 4 physical IC addresses based on voltage level)
10	FSET	Input for synchronizing boost and charge pump signals switching frequency to external clock signal; alternatively, it can be connected to an external resistor to set the switching frequency
11	BIAS	Output from internal 2.8 V bias regulator; connect to GND via 1 µF ceramic capacitor for decoupling
12	COMP	Compensation pin, connect to external COMP components (R_Z and C_Z)
13	AVDD	Output from internal LDO (item 1 in Functional Block Diagram) powered by V_{OUT}
14	AGND	Analog GND reference for signals; connect to ground plane
15	VGL	Inverted charge pump output (item 3 in Functional Block Diagram)
16	CP22	Capacitor terminals for inverted charge pump (item 3 in Functional Block Diagram)
17	CP21	
18	VGH	2× charge pump output (item 4 in Functional Block Diagram)
19	VGH3	3× charge pump output (item 4 in Functional Block Diagram)
20	CP11	Capacitor terminals for charge pump (item 4 in Functional Block Diagram)
21	CP12	
22	VOUT	Connect to boost output for internal LDO and charge pump regulators
23	PGND	Power ground for internal boost switch; connect this pin to ground terminal of output ceramic capacitor(s)
24	SW	Internal boost converter switch node
–	PAD	

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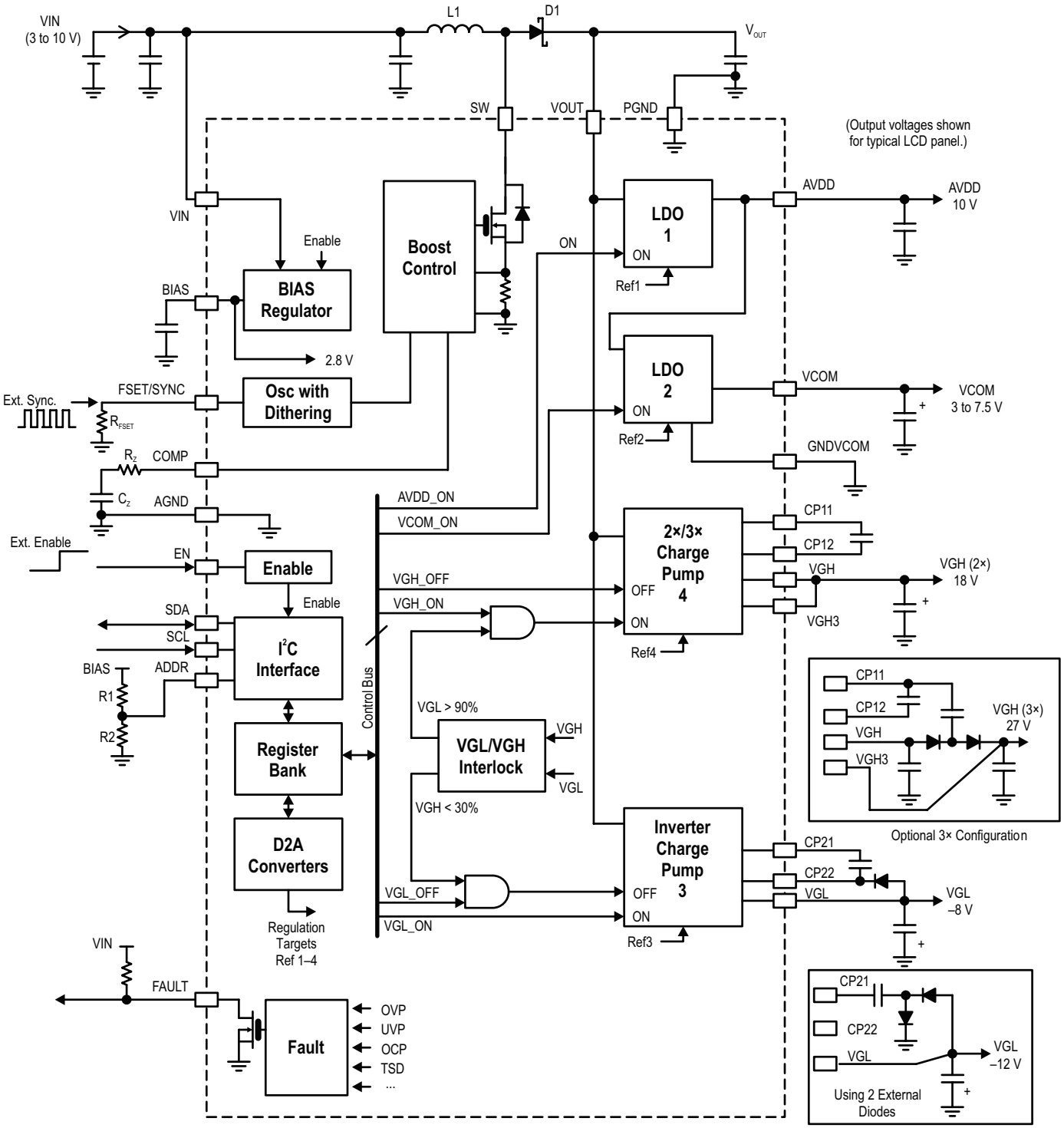

Functional Block Diagram

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ELECTRICAL CHARACTERISTICS [1]: Valid at V_{IN} = 5 V, EN = high, f_{SW} = 2 MHz, V_{AVDD} = 10 V, V_{VGH1} = 20 V, V_{VGL} = –8 V, T_J = T_A = 25°C, except • indicates specifications guaranteed for T_J = T_A = −40°C to 125°C, unless otherwise specified

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
INPUT VOLTAGE AND CURRENT							
Input Voltage	V_{IN}		•	3	–	10	V
VIN Pin Undervoltage Lockout (UVLO) Threshold	V_{UVLO}	V_{IN} rising	•	–	2.8	2.9	V
VIN Pin UVLO Hysteresis	$V_{UVLO(HYS)}$			–	0.15	0.25	V
BIAS Voltage	V_{BIAS}	Internal BIAS regulator, EN = high		–	2.8	–	V
Shutdown BIAS Current [1]	$I_{VINBIAS(SD)}$	Current into VIN pin, EN = low	•	–	1	10	µA
Standby BIAS Current	$I_{VINBIAS(STB)}$	EN = high, output disabled		–	3	–	mA
Operating BIAS Current	$I_{VINBIAS(OP)}$	EN = high, output enabled		–	6	–	mA
BOOST SWITCH							
Switch Peak Current Limit	I_{SWILIM}	Cycle-by-cycle current limit	•	2.2	2.6	3	A
Switch Secondary Current Limit	$I_{SWILIM2}$	Trips SW_OCP fault if exceeded		–	3.7	–	A
Switch On-Resistance	$R_{DS(on)}$	I_{SW} = 0.4 A		–	0.4	0.7	Ω
Switch Minimum On-Time	$t_{ON(MIN)}$		•	–	65	120	ns
Switch Minimum Off-Time	$t_{OFF(MIN)}$		•	–	60	100	ns
SW Pin Leakage Current	$I_{SW(LKG)}$	V_{SW} = 5 V, EN = low		–	0.1	–	µA
VOUT Pin Leakage Current	$I_{OUT(LKG)}$	V_{OUT} = 5 V, EN = low		–	0.1	–	µA
		V_{OUT} = 10 V, EN = low		–	25	37	µA
SW Pin Overvoltage Protection Threshold	$V_{SW(OVP)}$	Measured from SW to GND	•	18.6	21	23	V
SW OVP Detection Time [2]	$t_{SW(OVP)}$	Minimum pulse width required for $V_{SW} \geq V_{SW(OVP)}$ to be detected as SW OVP		–	40	–	ns
SW OVP to Shutdown Delay [2]	$t_{FAULT(OVP)}$	Delay from SW OVP to FAULT = L		–	1	2.5	µs
SWITCHING FREQUENCY/SYNCHRONIZATION							
FSET_SYNC Pin Voltage	$V_{FSETSYNC}$	Without using external synchronization signal		–	0.64	–	V
FSET_SYNC Pin Current	$I_{FSETSYNC}$			22	–	140	µA
Switching Frequency	f_{SW}	R_{FSET_SYNC} = 5.1 kΩ	•	1.8	2	2.2	MHz
Synchronization Frequency	f_{SYNC}	External logic sugnal connected to FSET_SYNC pin	•	0.35	–	2.25	MHz
Synchronization Minimum On-Time	$t_{SYNC(ON)}$		•	150	–	–	ns
Synchronization Minimum Off-Time	$t_{SYNC(OFF)}$		•	150	–	–	ns
Switching Frequency Dithering Range	Δf_{SW0}	No external synch, REG0x10 = ‘00b’		–	0	–	%
		No external synch, REG0x10 = ‘01b’		–	5	–	%
		No external synch, REG0x10 = ‘10b’		–	10	–	%
		No external synch, REG0x10 = ‘11b’		–	15	–	%

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ELECTRICAL CHARACTERISTICS [1] (continued): Valid at V_{IN} = 5 V, EN = high, f_{SW} = 2 MHz, V_{AVDD} = 10 V, V_{VGH1} = 20 V, V_{VGL} = –8 V, $T_J = T_A$ = 25°C, except • indicates specifications guaranteed for $T_J = T_A$ = −40°C to 125°C, unless otherwise specified

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
ERROR AMPLIFIER							
Open-Loop Voltage Gain [2]	A_{VOL}			–	43	–	dB
Transconductance [2]	g_m	I_{COMP} = between –100 µA and 100 µA		–	550	–	µA/V
EA Source Current	I_{EA_SRC}	V_{COMP} = 0.7 V, V_{OUT} below regulation target		–	200	–	µA
EA Sink Current	I_{EA_SINK}	V_{COMP} = 0.7 V, V_{OUT} over regulation target		–	200	–	µA
COMP Pull-Down Resistor	R_{COMP1}	Active pull-down when EN = H, Boost disabled		–	2.5	–	kΩ
	R_{COMP2}	Passive pull-down when EN = L		–	450	–	kΩ
LOGIC INPUTS							
EN Pin Logic High	V_{IH_EN}		•	1.8	–	–	V
EN Pin Logic Low	V_{IL_EN}		•	–	–	0.8	V
Internal Pull-Down Resistance to AGND	$R_{EN(PD)}$			–	100	–	kΩ
Hard-Reset Duration [2]	t_{RESET}	EN = L duration in order to initiate a hardware reset during normal operation		2	–	–	µs
FSET Pin Input Logic High	V_{IH_FSE}	When used in external sync mode	•	1.5	–	–	V
FSET Pin Input Logic Low	V_{IL_FSE}	When used in external sync mode	•	–	–	0.4	V
OVER- AND UNDERVOLTAGE PROTECTION FOR OUTPUT REGULATORS							
Output Overvoltage Fault Threshold	$V_{OUTx(OV)}$	Output rising; measured as % of target voltage		–	120	–	%
Output Undervoltage Fault Threshold	$V_{OUTx(UV)}$	Output falling; measured as % of target voltage		–	80	–	%
OUTPUT REGULATORS							
AVDD Output Voltage	V_{AVDD}		•	5	–	15	V
VCOM Output Voltage	V_{VCOM}	$V_{AVDD} > V_{VCOM}$ + 1.5 V	•	2.5	–	7.5	V
VGH Output Voltage	V_{VGH}	VGH & VGH3 shorted	•	10	–	30	V
VGL Output Voltage	V_{VGL}		•	–12	–	–4	V
Boost Minimum Headroom for AVDD Regulator	$V_{AVDD(DO)}$	Defined as $V_{OUT} – V_{AVDD}$; when AVDD = 15 V, I_{OUT} = 100 mA		–	2.1	–	V
Boost Minimum Headroom for VGH Regulator	$V_{VGH(DO)}$	Defined as $V_{OUT} – V_{VGH} / 2$; when V_{VGH} = 24 V, I_{OUT} = 8 mA		–	2.9	–	V
Boost Minimum Headroom for VGL Regulator	$V_{VGL(DO)}$	Defined as $V_{OUT} – (–V_{VGL})$; when V_{VGL} = –12 V, I_{OUT} = –8 mA		–	3.5	–	V
Ouptut Pull-Down Resistor During Shutdown (AVDD, VCOM)	R_{OUTPD1}	EN = high, output disabled		–	250	–	Ω
Ouptut Pull-Down Resistor During Shutdown (VGH, VGL)	R_{OUTPD2}	EN = high, output disabled		–	500	–	Ω
Ouptut Pull-Down Resistor in Sleep Mode (AVDD, VCOM, VGH)	R_{OUTPD3}	EN = low, $V_{IN} > V_{UVLO}$		–	1	–	kΩ
Ouptut Pull-Down Resistor in Sleep Mode (VGL only)	R_{OUTPD4}	EN = low		–	10	–	kΩ

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Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
OUTPUT CURRENT CAPACITY							
AVDD OCP Trip Level	$I_{AVDD(OCP)}$	Includes I_{VCOM}		200	275	350	mA
VCOM OCP Trip Level	$I_{VCOM(OCP)}$			36	45	54	mA
VGH OCP Trip Level	$I_{VGH(OCP)}$			11	20	26	mA
VGL OCP Trip Level	$I_{VGL(OCP)}$	Current into VGL pin		11	20	26	mA
OUTPUT VOLTAGE ACCURACY							
AVDD, VGH, and VGL Load Regulation	$V_{AVDDreg}$ V_{VGHreg} V_{VGLreg}	V_{AVDD} =10 V, I_{AVDD} = 10 to 100 mA V_{VGH} = 20 V, I_{VGH} = 0.4 to 4 mA V_{VGL} = –8 V, I_{VGL} = –0.8 to –8 mA	•	–0.1	–	0.1	V
AVDD Accuracy	Err_{AVDD}	Reg00 = 0x40 (V_{AVDD} = 10.04 V), I_{AVDD} = 50 mA	•	–2.1	–	2.1	%
VCOM Accuracy	Err_{VCOM}	Reg01,02 = 0x100 (V_{VCOM} = 5.005 V), I_{VCOM} = 10 mA	•	–2.1	–	2.1	%
VGH Accuracy	err_{VGH}	Reg04 = 0x40 (V_{VGH} = 20.65 V), I_{VGH} = 2 mA	•	–2.5	–	2.5	%
VGL Accuracy	err_{VGL}	Reg03 = 0x20 (V_{VGL} = –8.39 V), I_{VGL} = –4 mA	•	–2.5	–	2.5	%
VCOM Step Size					10		mV
VCOM Load Regulation [2]	$V_{VCOMreg}$	I_{LOAD} = 2 to 20 mA, V_{VCOM} = 5.0 V	•	–5	–	5	mV
VCOM Temperature Coefficient [2]	TC_{VCOM}	V_{VCOM} = 5 V, –30°C < T_A < 85°C, I_{LOAD} = 10 mA	•	–100	–	150	µV/°C
Minimum Dropout for VCOM from AVDD	$V_{VCOM(DO)}$	V_{AVDD} = 7 V, I_{VCOM} = 20 mA		–	–	1.5	V
FAULT PIN							
FAULT Pull-Down Voltage	$V_{FAULT(PD)}$	Fault condition asserted, pull-up current = 1 mA		–	–	0.4	V
FAULT Pin Leakage Current	$V_{FAULT(LKG)}$	Fault condition cleared, pull-up to 5 V		–	–	1	µA
PROGRAMMABLE DELAYS AND TIMERS							
Startup Timeout/Watchdog Timer (Time limit for all outputs to reach 90% target, starting from internal EN=H)	$t_{SU\_TO\_min}$	Minimum timeout when Reg0x9 = 0x03 or lower		–	9.6	–	ms
	$t_{SU\_TO\_max}$	Maximum timeout when Reg0x9 = 0x1F		–	99.2	–	ms
Startup Delay Timer#1-4 (One each for AVDD/VCOM/VGL/VGH)	$t_{SU\_DLY\_min}$	Minimum delay when Reg_X = 0x00, X = 5..8 [3]		–	0	–	ms
	$t_{SU\_DLY\_max}$	Maximum delay when Reg_X = 0xFF, X = 5..8 [3]		–	25.5	–	ms
Shutdown Timeout (starting from internal EN = L)	t_{SD_TO}	All outputs discharged to below 10% target (30% for VGL and VGH)		40	50	65	ms
Shutdown Delay Timer#5-8 (One each for AVDD/VCOM/VGL/VGH)	$t_{SD\_DLY\_min}$	Minimum delay when Reg_X = 0x00, X = C,D,E,F [3]		–	0		ms
	$t_{SD\_DLY\_max}$	Maximum delay when Reg_X = 0xFF, X = C,D,E,F [3]		–	25.5	–	ms
Overcurrent Protection (OCP) Timeout	t_{OCP_TO}	Maximum time for any output to stay in OCP fault condition before shutdown.		40	50	60	ms
Fault Retry Counter	$N_{RESTART}$	Maximum number of fault retries. Programmable through Reg0x0A		0	–	15	
Fault Cool-Down Timer	$t_{RESTART\_min}$	Cooldown time between fault shutdown and next retry. Reg0x0B = 0x03 or lower		–	9.6	–	ms
	$t_{RESTART\_max}$	Cooldown time between fault shutdown and next retry. Reg0x0B = 0x3F		–	201.6	–	ms

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ELECTRICAL CHARACTERISTICS [1] (continued): Valid at V_{IN} = 5 V, EN = high, f_{SW} = 2 MHz, V_{AVDD} = 10 V, V_{VGH1} = 20 V, V_{VGL} = –8 V, $T_J = T_A$ = 25°C, except • indicates specifications guaranteed for $T_J = T_A$ = −40°C to 125°C, unless otherwise specified

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
THERMAL SHUTDOWN (TSD) PROTECTION							
TSD Threshold [2]	T_{TSD}	Temperature rising		155	165	–	°C
TSD Hysteresis [2]	$T_{TSD(HYS)}$			–	20	–	°C
I²C INTERFACE							
Logic Input Low (SDA, SCL)	$V_{SCL(L)}$			–	–	0.8	V
Logic Input High (SDA, SCL)	$V_{SCL(H)}$			2.3	–	–	V
Logic Input Hysteresis [2]	$V_{I2CIHYS}$			–	150	–	mV
Logic Input Current	I_{I2CI}			–1	–	1	µA
SDA Output Voltage Low	$V_{I2COut(L)}$	SDA = Low, pull-up current = 2.5 mA		–	–	0.4	V
SDA Output Leakage	I_{I2CLKG}	EN = Low, pull-up to 5.5 V		–	–	1	µA
SCL Clock Frequency	f_{CLK}			–	–	400	KHz
ADDR PIN COMPARATOR THRESHOLD							
Voltage Level for Address 101,0000	$V_{ADDLEVEL1}$	ADDR connected to GND		0	–	0.3	V
Voltage Level for Address 101,0001	$V_{ADDLEVEL2}$			0.6	–	0.9	V
Voltage Level for Address 101,0010	$V_{ADDLEVEL3}$			1.5	–	1.8	V
Voltage Level for Address 101,0011	$V_{ADDLEVEL4}$	ADDR connected to BIAS pin		2.4	–	3	V

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization, not production tested.
[3] Refer to Table 5 for Register Map.

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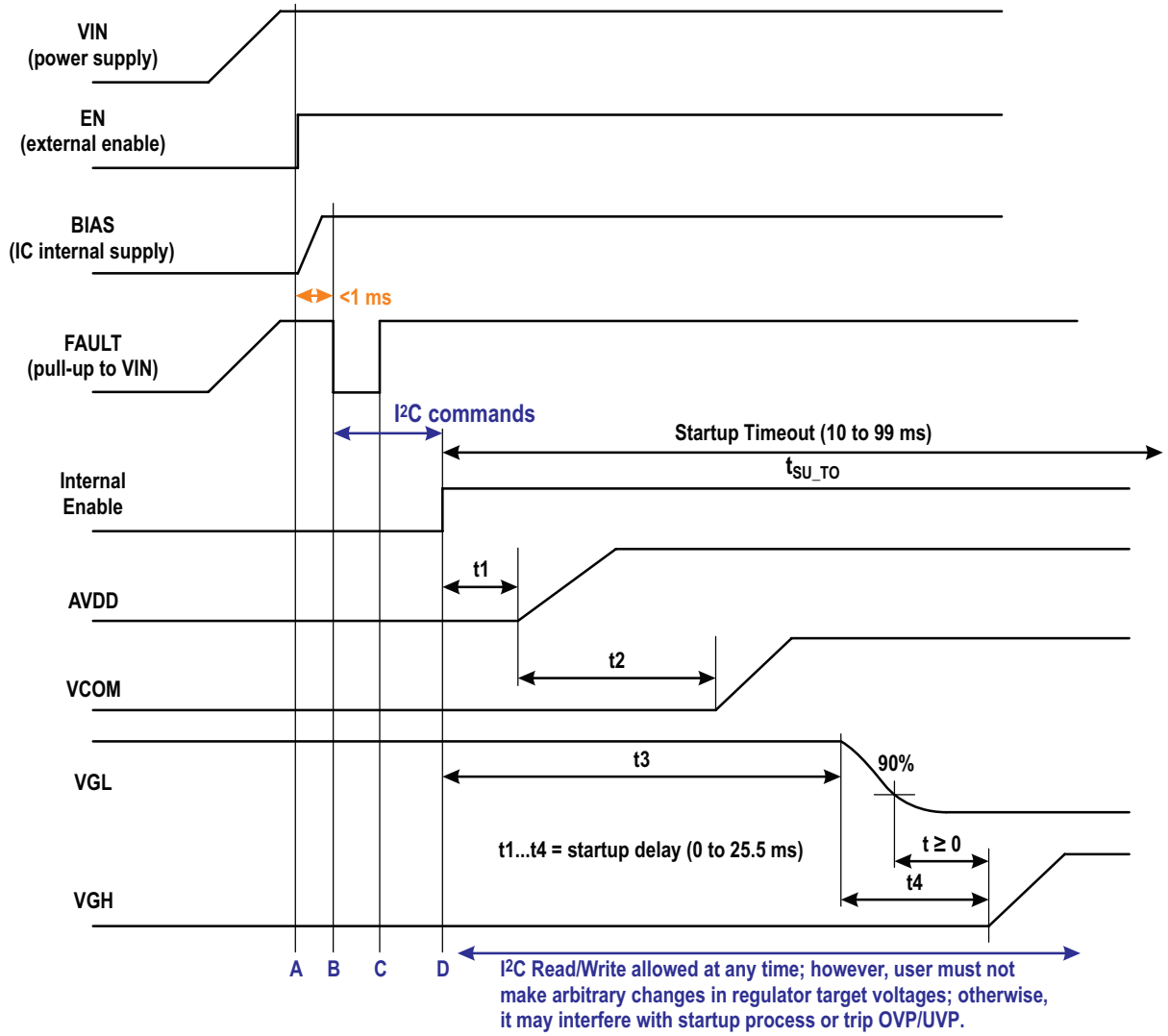
CHARACTERISTIC PERFORMANCE

Startup Timing Diagram



Sequence of events:

A: System controller brings EN = H to enable the A8603, provided that V_{IN} is above UVLO level.

B: After A8603 performs a Power-On Reset (POR), it pulls down FAULT flag to signal that it is ready for I²C commands. (*)

C: System controller detected FAULT = L and sends in I²C command to clear POR status bit. This resets FAULT to H (unless there were other faults detected).

D: After Programming the A8603 registers, system controller sets the *regulator_internal_enable* bit to 1 to turn on all output regulators.

Notes on Startup Timing Diagram

- Each regulator has a programmable Startup Delay timer. Each timer has a resolution of 0.1 ms and a maximum duration of 25.5 ms.
- VCOM cannot start before AVDD (because internally the VCOM regulator takes its power from AVDD output)
- VGH cannot start before VGL has reached 90% of its target voltage
- There is no dependency between {t1, t2} and {t3, t4}. That means VGL/VGH can start before or after AVDD/VCOM
- If any regulator output failed to reach 90% target after the Startup Timeout period (default 50 ms, starting from Internal Enable = H), the FAULT pin will be pulled low and all outputs are shut down in an orderly manner. The IC will then retry after a Cool Down period.

(*) The delay time between EN = H and FAULT = L depends mainly on how fast the external BIAS capacitor can be charged up. For example, charging 1 µF at 5 mA from 0 to 2.8 V takes ~0.6 ms. Therefore, a 1 ms delay time is sufficient.

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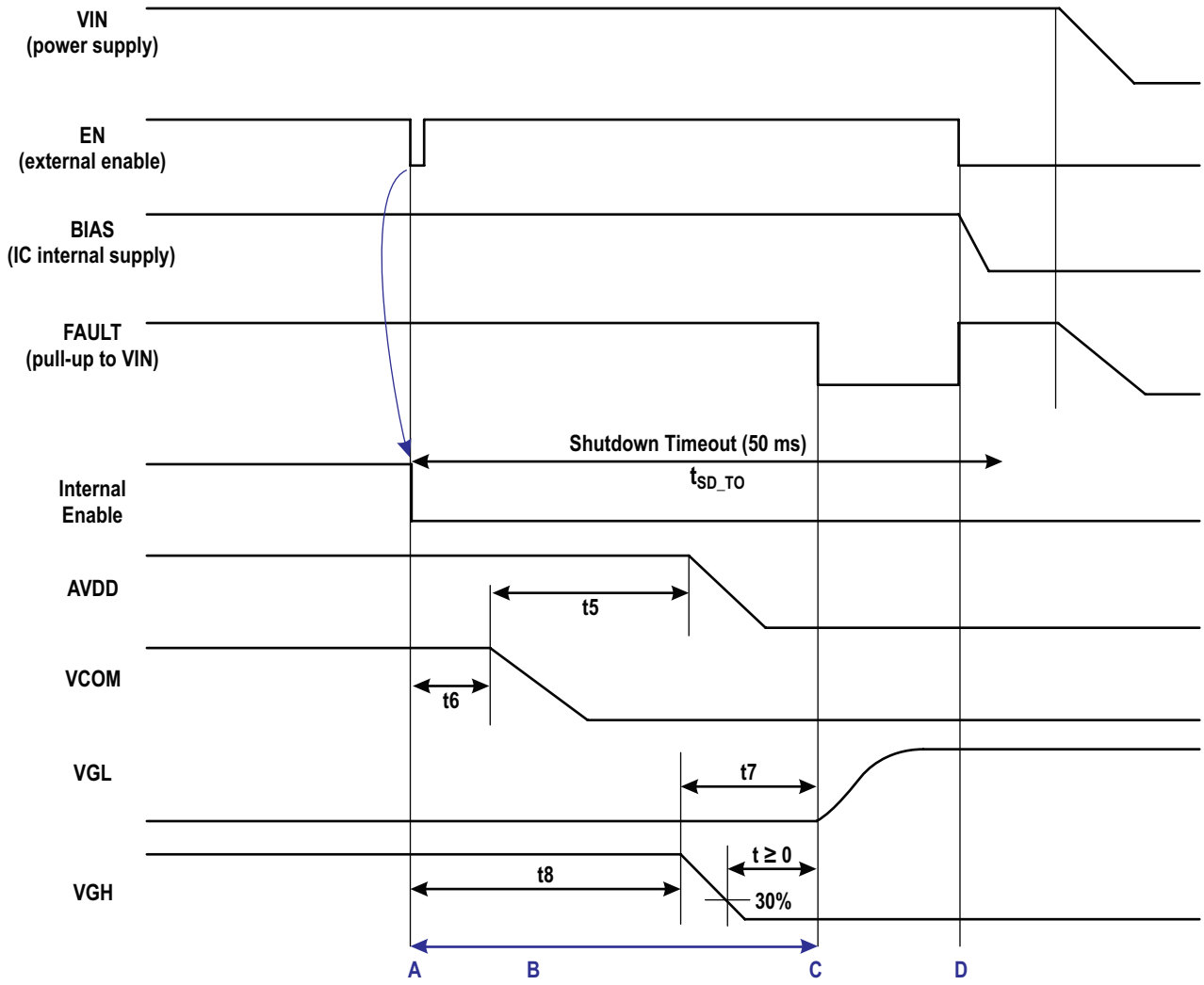
Shutdown Timing Diagram



Sequence of events:

A: System controller brings EN pin to Low for >2 µs to initiate a "Hardware Shutdown." The IC responds by pulling Internal Enable to Low.

B: The A8603 shuts down all output regulators in sequence, according to their shutdown delay times. All registers will be restored to power-up defaults at the end of a Hardware Shutdown. This does not apply to a Software Shutdown when user programs INT_EN = L.

C: After the last regulator has shut down, the A8603 resets all internal registers to their power-on defaults, sets the HARD_RESET status bit to 1, and pulls FAULT pin to Low. The A8603 is now ready to accept new I²C commands.

D: The A8603 is powered down only if EN = L after shutdown has completed.

Notes on Shutdown Timing Diagram

- Each regulator has a programmable Shutdown Delay timer. Each timer has a resolution of 0.1 ms and a maximum duration of 25.5 ms.
- AVDD can only be turned off after VCOM is turned off (t5 = 0 is allowed)
- VGL can only be turned off after VGH drops below 30%, even through t7 = 0 is allowed.
- There is no dependency between {t5, t6} and {t7, t8}
- Once a shutdown is in progress, both external Enable and Internal EN are ignored until shutdown is completed.
- All output discharge times are based on external capacitance and internal pull-down resistance (250 Ω for AVDD and VCOM, 500 Ω for VGH and VGL). The external DC load is assumed to be negligible.
- If any of the regulator output does not decay to below 10% (30% for VGL and VGH) of target voltage after 50 ms time-out period, starting from beginning of shutdown, it is ignored and then the IC is allowed to power down.

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FUNCTIONAL DESCRIPTION

The A8603 is a flexible multivoltage regulator designed for LCD panel bias applications. It utilizes a high-efficiency boost converter, together with space-saving low-dropout (LDO) regulator and charge pump circuits to provide four independently adjustable voltage outputs:

- AVDD: Typically between 5 and 15 V. Nominal output current 100 mA. This output is from a LDO powered by VOUT.
- VCOM: Typically between 3 and 7.5 V at 20 mA. The power supply of this regulator is internally connected to AVDD. Therefore AVDD must be at least 1.5 V higher than the upper limit of VCOM.
- VGL: Typically between –12 and –4 V at 4 mA. This voltage is generated by an inverted charge pump, which is powered by VOUT.
- VGH: Typically between 10 and 24 V at 4 mA. This voltage is generated by a 2× charge pump, which is powered by VOUT.

If necessary, an external 3× charge pump can generate a higher VGH between 20 and 30 V at 4 mA.

Program Diagnostics

A8603 features the I²C (Inter-Integrated Circuit, alternatively spelled as I2C) serial interface and programmable memory array.

The I²C serial interface allows external microcontroller or some type of master device to communicate with A8603 as its slave device. Two bus lines, SCL and SDA, provide access to the internal control registers. The clock input on the SCL pin is generated by the master, while the SDA line functions as either an input or an open-drain output for the A8603, depending on the direction of the data flow.

In case there are two or more slave devices in an I²C network, each device must present a unique physical address for the master to select. To avoid conflict, the A8603 uses a 4-level ADDR pin to set its physical address. Depending on the voltage level at ADDR, the physical address is set as ‘101,00xx’, where xx = {00 | 01 | 10 | 11}. This is illustrated by the figure below.

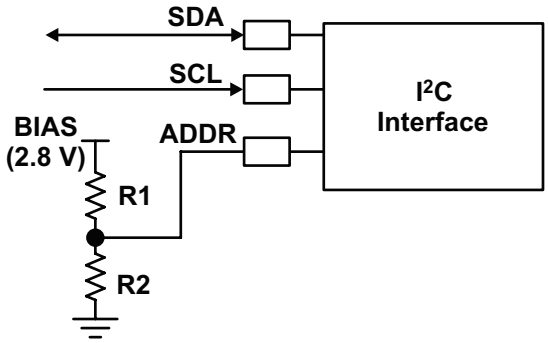

Figure 2: Select I²C Address by Using Resistor Divider at ADDR Pin

Table 1: I²C Address Selection Using Resistor Divider

R1 (k)	R2 (k)	V_{ADDR} (V)	I²C Address
open	0	0	101,0000
27.4	10	0.75	101,0001
6.98	10	1.65	101,0010
0	open	2.8	101,0011

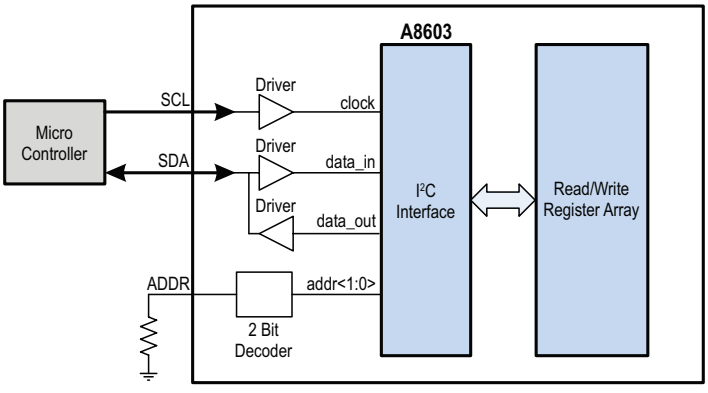

Figure 1: I²C Serial Interface and Programmable Memory Array

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Programmable Regulators

The A8603 has four voltage regulators: AVDD, VCOM, VGL, and VGH.

Target voltages of all four regulators are programmable by internal registers. In addition, other features (such as startup and shutdown sequences, Fault retry counter, etc.) can also be programmed.

The target voltage for each output regulator is programmed by writing to a register, according to the following equation:

$$Target\_Voltage = Min\_voltage + \#steps \times step\_size$$

For example, to set AVDD to 12 V, the user should write '0x59' to Reg0x00. This is because:

$$\#steps = (Target\_Voltage - Min\_Voltage) / step\_size$$

$$= (12 - 5) / 0.07874 = 88.9$$

So the content of Reg0x00 is 89 in decimal, or '0x59' in hexadecimal.

Table 2: Target Voltages

Output Regulator	Register	Min. Voltage (V)	Max. Voltage (V)	DAC # of Bits	DAC # of Steps	Step Size (mV)
AVDD	00	5 (Reg=0x00)	15 (0x7F)	7	127	78.74
VCOM	01, 02	2.5 (0x0000)	7.5 (0x01FF)	9	511	9.785
VGL	03	–3.6 (0x00)	–13.03 (0x3F)	6	63	–149.7
VGH	04	9.9 (0x00)	31.236 (0x7F)	7	127	168

*Note: AVDD must be at least 1.5V higher than VCOM, so not all combinations of VCOM and AVDD are possible.

Table 3: Startup Time Delay

Refer to Startup Timing Diagram on how those time delays are defined.

Timer	Min. Delay (ms)	Max. Delay (ms)	Step Size (ms)	Number of Bits
t1 = AVDD	0 (0x00)	25.5 (0xFF)	0.1	8
t2 = VCOM	0	25.5	0.1	8
t3 = VGL	0	25.5	0.1	8
t4 = VGH	0	25.5	0.1	8

Table 4: Shutdown Time Delay

Refer to Shutdown Timing Diagram on how those time delays are defined.

Timer	Min. Delay (ms)	Max. Delay (ms)	Step Size (ms)	Number of Bits
t5 = AVDD	0 (0x00)	25.5 (0xFF)	0.1	8
t6 = VCOM	0	25.5	0.1	8
t7 = VGL	0	25.5	0.1	8
t8 = VGH	0	25.5	0.1	8

Name	Register	Default	Min.	Max.	Step Size	Number of Bits
Watchdog Timer	0x09	51.2 (0x10) ms	9.6 (0x03) ms	99.2 (0x1F) ms	3.2 ms	5
Cooldown Timer	0x0B	102.4 (0x20) ms	9.6 (0x03) ms	201.6 (0x3F) ms	3.2 ms	6
Fault Retry Counter	0x0A	8 (0x08)	0 (0x00)	15 (0x0F)	1	4

Dithering:

Reg0x10 bit[0,1]: controls Dithering off, ±5%, 10% or 15%.

Power Sequence:

Reg0x10 bit4: By default VGL is enabled before VGH during power-up. But if this bit is set to '1', then VGH is enabled first.

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Table 5: I²C Register Map

Registers	Default	Address	Comments
Regulator Programming		0x00-0x13	
AVDD_voltage	0x40	0x00	7 bits adjust AVDD regulator output from 5 V to 15 V in 78.74 mV step.
VCOM_voltage_msb	0x1	0x01	9 bits adjust VCOM regulator output from 2.5 V to 7.5 V in 9.785 mV step. Must be programmed in the order of MSB followed by LSB.
VCOM_voltage_lsb	0x0	0x02	
VGL_voltage	0x20	0x03	6 bits adjust VGL regulator output from –3.6 V to –13.03 V in –150 mV step.
VGH_voltage	0x40	0x04	7 bits adjust VGH regulator output from 9.9 V to 31.236 V in 168 mV step.
delay_startup_AVDD	0x0	0x05	Program the turn-on delay for AVDD. 100 µs step size. 0 ms to 25.5 ms.
delay_startup_VCOM	0x20	0x06	Program the turn-on delay for VCOM (after AVDD). 100 µs step size. 0 ms to 25.5 ms. See Startup Timing diagram.
delay_startup_VGL	0x40	0x07	Program the turn-on delay for VGL. 100 µs step size. 0 ms to 25.5 ms.
delay_startup_VGH	0x40	0x08	Program the turn-on delay for VGH (after VGL). 100 µs step size. 0 ms to 25.5 ms.
watchdog_timer	0x10	0x09	Maximum time allowing regulator to reach its target value. 3.2 ms step. 9.6 ms to 99.2 ms. Same value is used for all regulators.
fault_counter	0x8	0x0A	Programmable counter allowing system to reattempt 0 to 15 times at the event of fault.
cooldown_timer	0x20	0x0B	Prevent immediate reattempt after the fault. System will wait for timer to expire before possible reattempt to turn on the regulators. Step size 3.2 ms. Range 9.6 ms to 201.6 ms.
delay_shutdown_AVDD	0x0	0x0C	Program the turn-off delay for AVDD (after VCOM). 100 µs step size. 0 ms to 25.5 ms. See Shutdown Timing diagram.
delay_shutdown_VCOM	0x0	0x0D	Program the turn-off delay for VCOM. 100 µs step size. 0 ms to 25.5 ms.
delay_shutdown_VGL	0x0	0x0E	Program the turn-off delay for VGL (after VGH). 100 µs step size. 0 ms to 25.5 ms.
delay_shutdown_VGH	0x0	0x0F	Program the turn-off delay for VGH. 100 µs step size. 0 ms to 25.5 ms.
dither	0x0	0x10	Bit[1,0] for dither programming (off/5%/10%/15%); Bit4 for VGL/VGH power sequence option.
regulator_internal_enable	0x0	0x11	'1' = Turn all regulators on. '0' = OFF
spare1	0x0	0x12	Spare
spare2	0x0	0x13	Spare
Fault Status		0x14-0x1B	
output_status_now	0x0	0x14	Present output voltage status of regulators (over 10%, 30%, or 90%)
ilimt_status_now	0x0	0x15	Present output current status of regulators (OCP)
fault_status_now	0x0	0x16	Present fault status (TSD, FSET_short, SW_OVP, SW_OCP, etc.)
output_status_hold	0x0	0x17	Latched output voltage status (over 120% or under 80%)
ilimt_status_hold	0x0	0x18	Latched output current status
fault_status_hold	0x0	0x19	Latched fault status
rstatus_hold	0x01	0x1A	Retry counter status [bit 4:7], Diagnostic [2,3], Hard_Reset [1], and POR [0].
sstatus_hold	0x0	0x1B	OVP/UVP status of regulators during startup

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DIAGNOSTIC REGISTERS

All faults and critical signals are recorded into log registers. External devices can read these log registers for diagnostic or maintenance purposes.

The A8603 provides two types of diagnostic status registers:

- Registers 0x14-16 (#20-22 in decimal) store the real-time status bits for regulator voltage, current, and fault conditions.
- Registers 0x17-1B (#23-27 in decimal) store the 'latched' status bits for voltage, current, and fault conditions. In case of a fault shutdown, the real-time status bits may be cleared, but the user can read the latched status bits and determine the cause for the shutdown.

Real-Time Status Registers

Registers 0x14 to 0x16 are read-only (refer to Tables 6 - 8).

Table 6: Register 0x14 – Output Voltage Status During Startup/Shutdown

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
VGH > 90%	VGL > 90%	VCOM > 90%	AVDD > 90%	VGH > 30%	VGL > 30%	VCOM > 10%	AVDD > 10%

Each bit is set to '1' when its corresponding regulator voltage is above threshold. They are only useful during startup and shutdown.

Table 7: Register 0x15 – Output Current Status During Operation

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
-	-	-	-	VGH ILimit	VGL ILimit	VCOM ILimit	AVDD ILimit

Each bit is set to '1' when its corresponding regulator is operating at current limit. Note that those bits are ignored during startup phase (where all regulators must work at current limit to charge up output capacitors quickly). During normal operation mode, it is acceptable for any regulator to reach its current limit momentarily. Only if the overcurrent condition persists for 50 ms, then the FAULT pin is pulled down and a RailFault (Reg0x16 bit2) is recorded.

Table 8: Register 0x16 – Fault Status

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
FAULT	MaxRetry	WatchDog	SW ILimit2	SW OVP	Rail Fault	FSET fault	TSD

Explanation of each bit:
Bit7 = 1 if any Fault has occurred (it is *not* set in case of a POR or Hard-Reset).
Bit6 = 1 if the number of fault retries has reached MaxRetry limit.
Bit5 = 1 if the startup watchdog timer (Reg0x09) has expired before all output regulators can reach 90% target.
Bit4 = 1 if the boost switch current has exceeded its secondary OCP limit (150% of cycle-by-cycle current limit).
Bit3 = 1 if the boost switch voltage has exceeded its OVP threshold.
Bit2 = 1 if any output regulator reached its OCP limit for 50 ms.
Bit1 = 1 if the FSET pin is either open or shorted to GND.
Bit0 = 1 if a thermal shutdown has occurred.

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Latched Status Registers

Registers 0x17 to 0x1B hold the status bits after a fault has occurred. Each bit is read-only and can be only cleared by writing a '1' to it. In case of a fault shutdown, the user can read those registers to determine the cause of the shutdown, and then clear them by writing '0xFF' to each register.

Table 9: Register 0x17 – Latched Output Over- and Undervoltage Protection Fault

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
VGH > 120%	VGL > 120%	VCOM > 120%	AVDD > 120%	VGH < 80%	VGL < 80%	VCOM < 80%	AVDD < 80%

Each bit is set to '1' when its corresponding regulator has tripped OVP/UVP fault. Note that those bits can only be set after all regulators have finished startup stage and the IC is in normal operation mode.

Table 10: Register 0x18 – Latched Output Overcurrent Protection Fault

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved	-	-	-	VGH ILimit	VGL ILimit	VCOM ILimit	AVDD ILimit

Each bit is set to '1' when its corresponding regulator is operating at current limit during normal operation.

Table 11: Register 0x19 – Latched Fault Status

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
FAULT	MaxRetry	Watchdog	SW ILimit2	SW OVP	Rail Fault	FSET fault	TSD

See Register 0x16 for explanation of each bit.

Table 12: Register 0x1A – Latched Non-Fault Status

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Current Retry Counter (Read-Only)				SW ILimit1	Slow Shutdown	Hard Reset	Power-On Reset

Bit[4..7] = Current Retry Counter (0 to 15)
Bit3 = 1 if boost switch cycle-by-cycle current limit has be reached. This is not a fault condition and IC does not shutdown.
Bit2 = 1 if during shutdown, any regulator failed to decay below 10% (AVDD/VCOM) or 30% (VGL/VGH) before watchdog timer expires. This is not a fault since the IC still shuts down afterward.
Bit1 = 1 if the IC has finished a hardware-initiated shutdown (by EN = L briefly) and all registers are restored to default values.
Bit0 = 1 if the IC has finished a power-on reset and all registers are initialized to their default values.
Note that after a Power-On Reset (or a Hard Reset), the output regulator cannot be enabled until bit0 (or bit1) is cleared. This can be done by writing a '0x03' to Register0x1A.

Table 13: Register 0x1B – Latched Over- and Undervoltage Status During Startup

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
VGH > 120%	VGL > 120%	VCOM > 120%	AVDD > 120%	VGH < 80%	VGL < 80%	VCOM < 80%	AVDD < 80%

This is similar to Register 0x17, except it only records OVP/UVP during startup phase. Suppose, under certain unlikely situations, a regulator output rises above 120% or drops below 80% after it reached 90% but before the IC enters normal operation mode, then it will be recorded.

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DESCRIPTION OF REGULATORS

AVDD Regulator

The AVDD output is driven by a linear regulator, which takes its input power from the boost output voltage. The target voltage of AVDD is programmable through Register 0x00 (7 bits). Its range is between 5 V (Register = 0x00) and 15 V (Register = 0x7F) in 127 steps, with step resolution = 78.74 mV. A representative block diagram is shown in Figure 3.

The AVDD circuit monitors the voltage drop across its linear regulator. If this voltage drop is less than the headroom required (approximately 2 V between OUT and AVDD), the monitor circuit sends a control signal to cause the boost voltage to increase. This ensures there is always enough headroom for regulation.

VCOM Regulator

The VCOM output is also driven by a linear regulator similar to the case of AVDD, except that it takes its input power from the regulated AVDD output voltage. This arrangement gives VCOM exceptional stability over full operating temperature range. The target voltage of VCOM is programmable through Register 0x01-02 (9 bits total). Its range is between 2.5 V (Register=0x0000) and 7.5 V (Register=0x01FF) in 511 steps, with step resolution = 9.785 mV.

In order to ensure there is enough headroom, AVDD must be at least 1.5 V higher than VCOM.

If VCOM is not required, the VCOM pin can be left open, but a small output capacitor (approximately 0.1 µF) must be present to prevent oscillation.

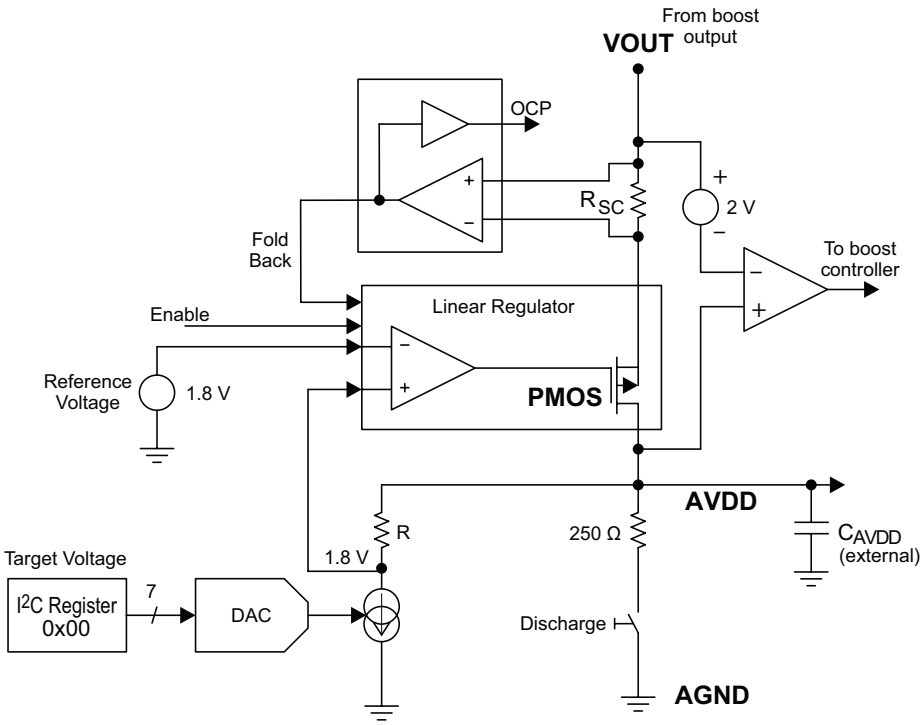

Figure 3: Representative Block Diagram of the AVDD Regulator

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VGL/VGH Charge Pumps

The A8603 uses a 2× charge pump to generate VGH from boost voltage. If necessary, a 3× charge pump can be implemented at the VGH3 pin using external components. See Representative Block Diagrams as shown in Figures 4 and 5. Depending on the magnitude of VGH, using a 3× charge pump may lower the boost output voltage and hence improve the system efficiency. See Boost Controller section for details.

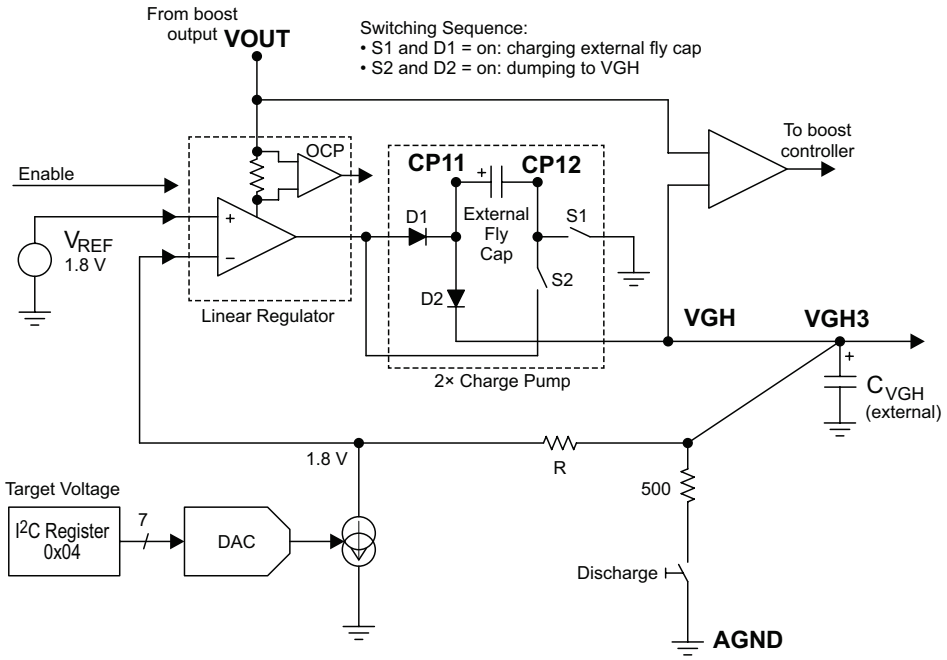

Figure 4: Representative Block Diagram of the VGH Regulator in 2× Charge Pump Mode

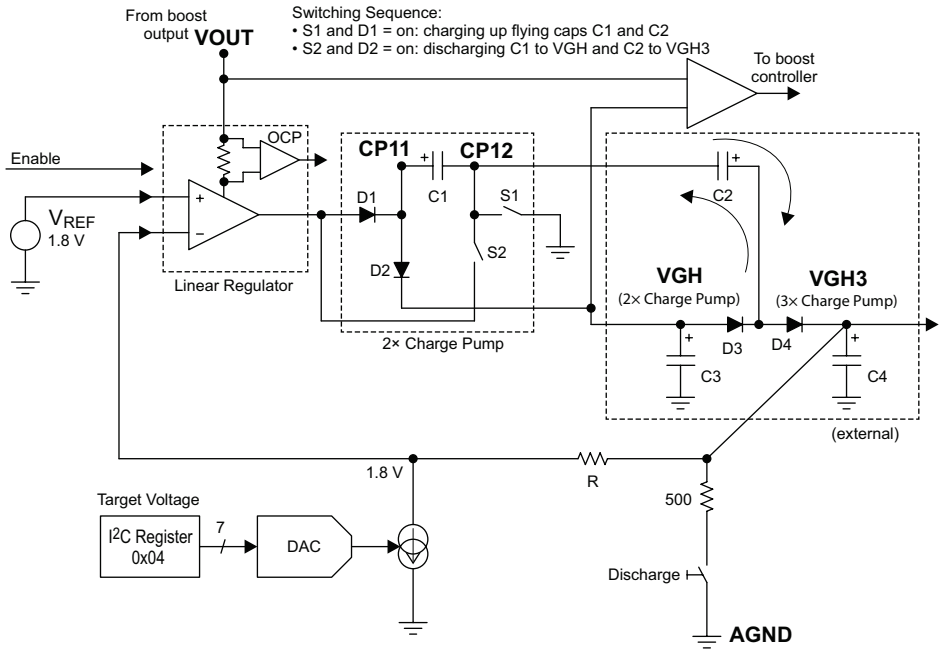

Figure 5: Representative Block Diagram of the VGH Regulator in 3× Charge Pump Mode

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An inverting charge pump is used to generate the negative voltage for VGL. A representative block diagram is shown in Figure 6.

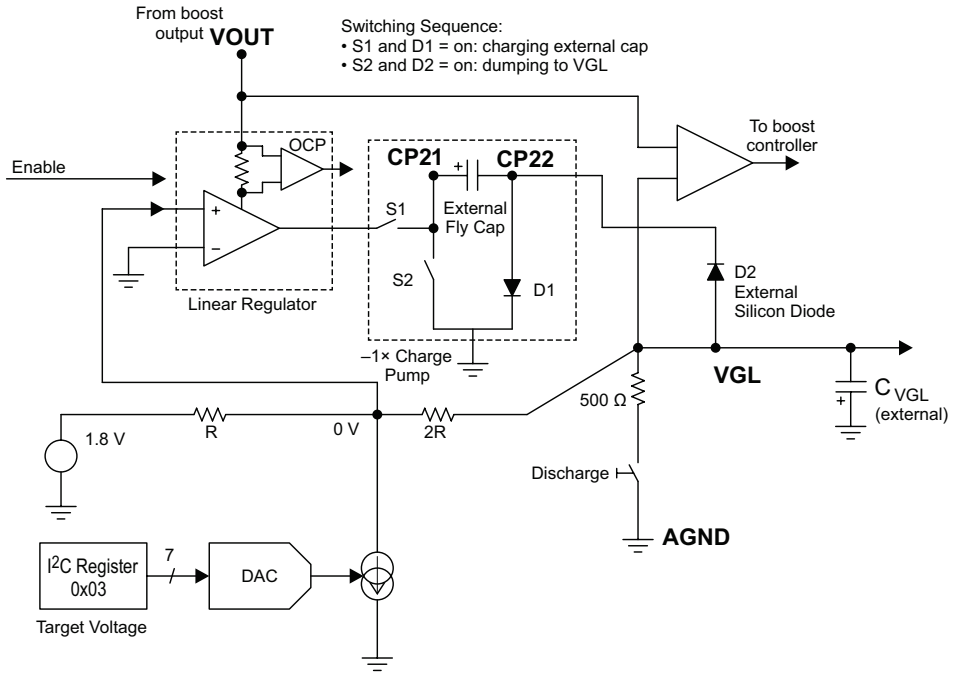

Figure 6: Representative Block Diagram of the VGL Negative Charge Pump Mode

The frequency of the charge pumps is the same as the boost switching frequency (or external SYNC frequency). When an external SYNC signal is used, it is internally converted into a clock signal with the same frequency, but at 50% duty cycle.

Recommended values of the external flying capacitor, C_{FLYx}, on the C_{Pxx} pins depends on the switching frequency as shown in the following table; a voltage rating of 25 V is sufficient.

Table 14: Recommended Flying Capacitor Values

Switching Frequency (MHz)	C_{FLYx} (µF)
2	0.1
1	0.22
0.35	0.47

The value of the flying capacitor can be calculates as follows:

1. The equivalent series resistance of the flying capacitor is:

$$ESR_{FLY2} = 1 / (f_{SW} \times C_{FLY2}) \quad (2)$$

2. Assuming a flying capacitor ripple voltage of 100 mV, and a maximum output current of 20 mA, the series resistance is:

$$R_{FLY2} \leq 0.1\ (V) / 0.02\ (A) = 5\ \Omega$$

3. Therefore at an f_{SW} of 2 MHz, the required capacitance, C_{FLY2}, is 0.1 µF.

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Boost Controller

The A8603 contains an integrated DMOS switch and PWM controller to drive a boost converter. The input voltage, V_{IN}, (3.3 V nominal) is boosted to an intermediate voltage, V_{OUT}, which is the lowest voltage required to keep all outputs within regulation. The final output voltage is decided by the regulator, which requires the highest boost voltage. This is illustrated in Figure 7.

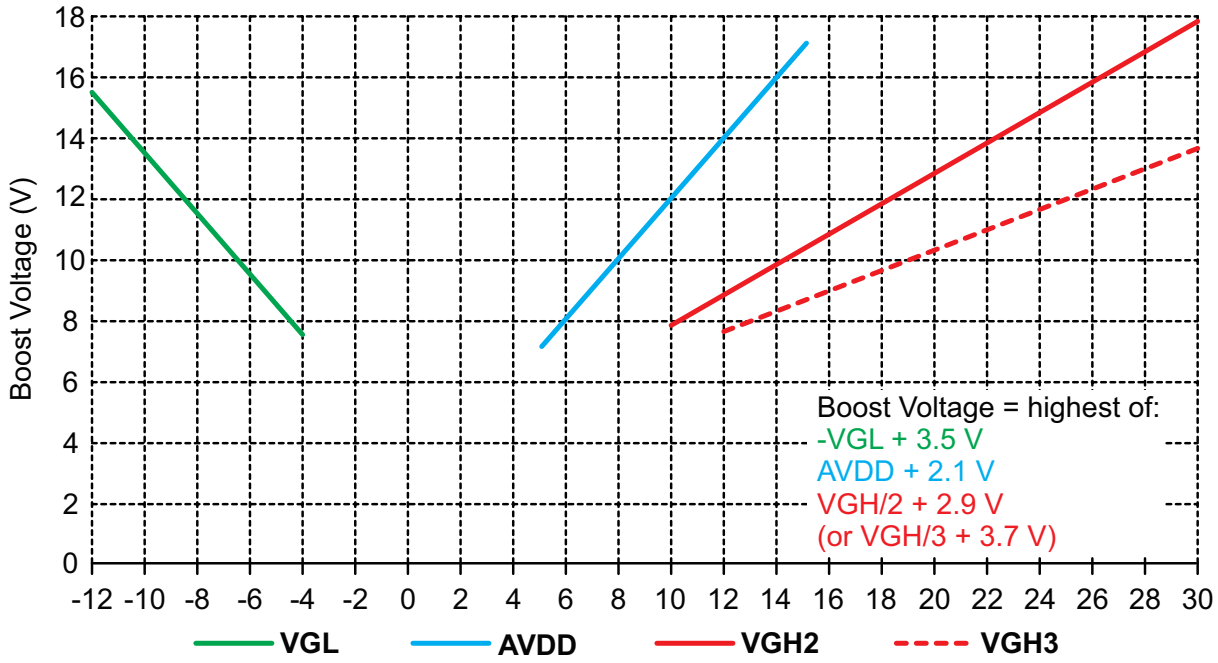

Figure 7: Boost Voltage Requirement with Respect to VGL, AVDD and VGH

For example: assume the output requirements for a certain LCD panel are: V_{AVDD} = 10 V, V_{VGH} = 18 V and V_{VGL} = –7 V, then:

- AVDD (LDO):

$$V_{OUT} \geq V_{AVDD} + 2.1\ (V) = 12.1\ V$$

- VGH (2× Charge Pump):

$$V_{OUT} \geq V_{VGH}\ /\ 2 + 2.9\ (V) = 11.9\ V$$

- VGL (Inverted Charge Pump):

$$V_{OUT} \geq -V_{VGL} + 3.5\ (V) = 10.5\ V$$

In this example, AVDD has the highest requirement, so the boost output voltage will be regulated at a V_{OUT} = 12.1 V approximately. However, if V_{VGH} were increased to 24 V, it would require higher voltage, and then the boost converter would increase the boost output voltage to 14.9 V to satisfy the 2× charge pump. This leads to higher voltage drop across the linear regulator for AVDD, and hence higher power loss. In such case, it is worthwhile to consider the option of 3× charge pump for VGH.

- VGH (2× Charge Pump):

$$V_{OUT} \geq V_{VGH}\ /\ 2 + 2.9\ (V) = 14.9\ V$$

- VGH (3× Charge Pump):

$$V_{OUT} \geq V_{VGH}\ /\ 3 + 3.7\ (V) = 11.7\ V$$

So by using 3× charge pump for VGH, the boost voltage is reduced to 12.1 V (as dominated by AVDD). This results in lower power loss and hence better system efficiency.

A block diagram of the A8603 boost controller circuit is shown in Figure 8. Typical values for external COMP components are R_Z = 511 Ω and C_Z = 0.22 µF. Note that the boost stage simply provides an intermediate voltage. The actual output voltages (AVDD, VGL, VGH) are controlled by linear regulators and charge pumps, which contain their own internal compensation.

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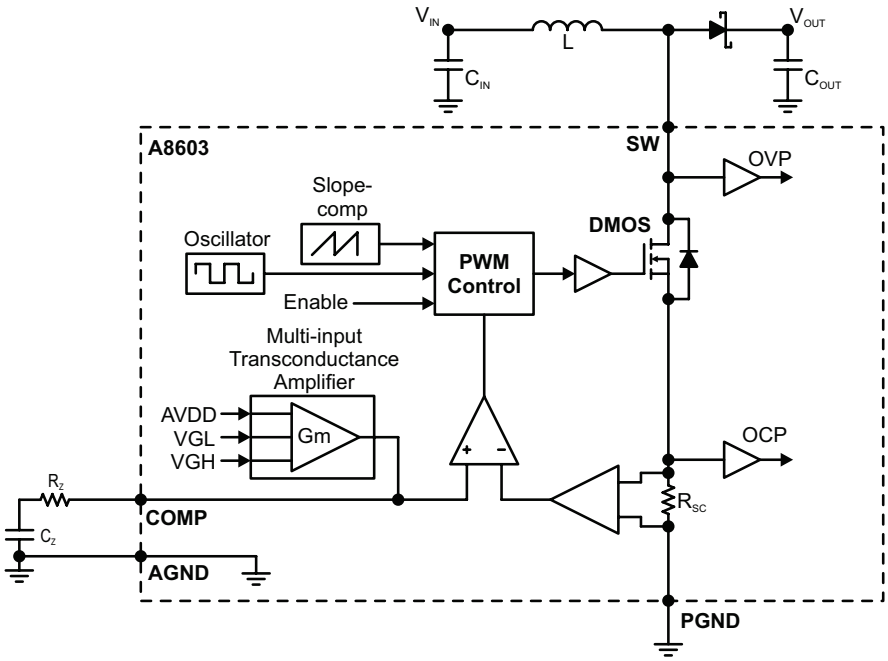

Figure 8: Boost Controller Circuit

The boost controller is protected against overvoltage and overcurrent fault conditions.

- The Switch OVP threshold, $V_{SW(OVP)}$, is internally set at approximately 21 V typical. Under normal operating conditions, the boost output voltage should always be lower than 18 V, so only in the event of a fault will SW_OVP be tripped (for example: boost diode open or VOUT pin open during startup).
- The switch current is protected by a cycle-by-cycle current limit (I_{SWILIM} , 2.6 A typical). In the event of a heavy load or during a transient, the SW peak current may reach SWILIM level momentarily. In this case, the present on-time is truncated immediately, but no signal is generated on the FAULT pin. The switching will continue with the same period.
- In the event of a catastrophic failure (such as shorted inductor), the SW current may exceed SWILIM2, which is 150% of the SWILIM threshold. In this case, the IC is shut down immediately.

It is important to note that the A8603 cannot protect the input current in case there is a short from boost output to GND. To do so requires the use of an input disconnect switch.

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Boost Switching Frequency

The boost stage switching frequency, f_{SW} , of the A8603 can be programmed by using an external resistor between the FSET pin to GND, or it can be synchronized to an external clock frequency between 350 kHz and 2.25 MHz.

During startup, the A8603 senses the FSET pin for any external SYNC signal. If periodic logic transitions are detected (Low < 0.4 V or High > 1.5 V), this is evaluated as an external clock signal, and the boost switching frequency is synchronized to it. If no periodic signal is detected, the bias current flowing through FSET_SYNC pin is used to determine the switching frequency. The bias current is set by an external resistor, R_{FSET} , on the FSET_SYNC pin. The relation between R_{FSET} and switching frequency is given as:

$$R_{FSET} = 10.21 / (f_{SW} - 0.0025) \quad (3)$$

where R_{FSET} is in kΩ and f_{SW} is in MHz.

This relationship is charted in Figure 9. For example, to get a switching frequency of 2 MHz requires an R_{FSET} of 5.11 kΩ.

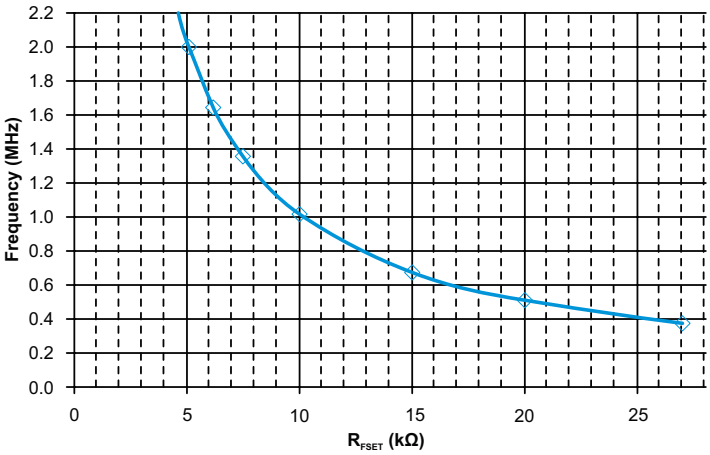

Figure 9: Boost Switching Frequency as a Function of FSET Resistance

Suppose the A8603 is started up with a valid external SYNC signal, but the SYNC signal is lost during normal operation. In that case, one of the following happens

- If the external SYNC signal is high impedance (open), the A8603 continues normal operation, at the switching frequency set by R_{FSET} . No FAULT flag is generated
- If the external SYNC signal is stuck at low (shorted to ground), the A8603 begins a shutdown sequence, at the switching frequency set by the internal 1 MHz oscillator. The FAULT pin is pulled low and the internal error counter is increased by 1.

Note:
To prevent generating a fault when the external SYNC signal is stuck at low, the circuit shown in Figure 10 can be used. When the external SYNC signal goes low, the A8603 will continue to operate normally at the switching frequency set by R_{FSET}. No FAULT flag is generated.

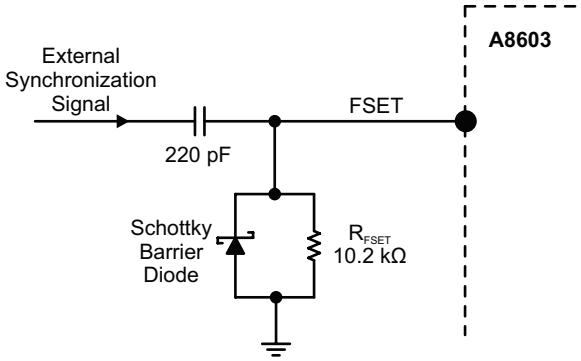

Figure 10: Countermeasure to Prevent External Sync Signal Stuck-at-Low Fault

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Boost Frequency Dithering

The A8603 has an optional dithering function for the boost switching frequency. When enabled, the switching frequency is varied linearly within a certain frequency range, as modulated by a triangular ramp signal. By spreading the frequency of the boost converter, the overall system noise magnitude can be greatly reduced. Note that the frequency dithering function is not available when an external synchronization signal is used at the FSET pin.

The dithering feature is controlled by Register 0x10. Frequency of the dithering modulation ramp signal is 12 kHz typical.

Table 15: Register 0x10 Dithering Feature

Reg0x10 Content (in binary)	Dithering Feature (frequency range)
'00'	0%
'01'	±5%
'10'	±10%
'11'	±15%

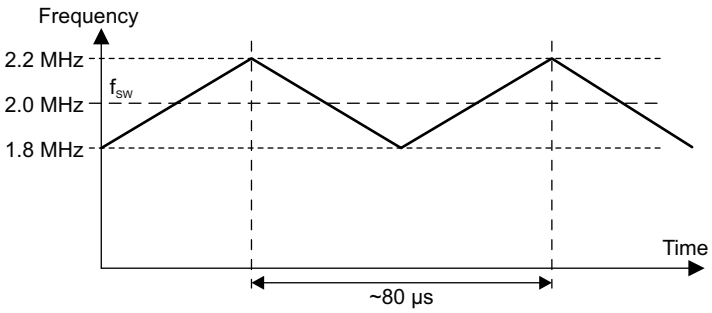

Figure 11: Switching Frequency Varied Linearly

In this example, Reg0x10 = '10' and the central switching frequency is f_{SW} = 2.0 MHz. The actual frequency is varied linearly between f_{SW} –10% and f_{SW} +10% by the modulating frequency at 12 kHz.

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FAULT CONDITIONS

The A8603 has extensive fault detection mechanisms, to protect against all perceivable faults at the IC level (pin open, pin short to GND, pin short to neighboring pins, and so forth) and at the system level (external component open/short, component value changes from –50% to +100%, and so forth).

The FAULT pin of the A8603 has an open-drain pull-down device internally. An external resistor is required to pull this pin to the desired logic-high level (such as 5 V or 3.3 V) at no-fault. Choose a resistor value such that, in case of fault, the current into the FAULT pin is not more than 1 mA. For example, if the external supply is 5 V, then the pull-up resistor should be 5 kΩ or higher.

In general, if a fault is detected, the A8603 halts operation and pulls the FAULT pin low. It then attempts to restart operation after a delay, $t_{RESTART}$ (programmable between 10 and 200 ms). Internally there is a Fault counter that keeps track of how many times any fault has occurred. If the Fault counter reaches maximum retry limit (programmable between 0 and 15), the A8603 stops any further attempts and returns to initial state with all regulators disabled. The Fault status register can be read through I^2C commands, but internal enable signal is prohibited in this state. The Fault counter is cleared only by a completed shutdown sequence after EN = low, or by a power reset (V_{IN} drops below UVLO).

As an example: If the FSET pin is either open or shorted to GND, the A8603 will report a fault by asserting FAULT = L once EN = H. All output regulators are disabled in this case, but the user can still use an I^2C Read command to read the fault status registers, and find out which type of fault has occurred. See “Diagnostic Registers” section for details.

Over- and Undervoltage Protections

All regulator output pins (AVDD, VGL, VGH, VCOM) are monitored for overvoltage and undervoltage faults during normal operation.

In case of an output short, the output voltage may make a sudden change that is either +20% over, or –20% under the target voltage. This will trigger the OVP/UVP fault and force the A8603 to shut down. The offending regulator is turned off immediately. The other outputs are then shut down following normal sequence.

OVP/UVP detections are disabled during the startup sequence. If any output fails to reach 90% of its target voltage within a time-out period, $t_{SS(TO)}$ (50 ms typical), a fault is generated and then the A8603 shuts down.

Each regulator output (AVDD, VGH, VGL and VCOM) is protected by its own independent overcurrent limit. When an output current exceeds its limit, the corresponding regulator goes into overcurrent protection mode to protect itself from damage. See next section for illustrations of the protection characteristics.

If the overcurrent condition persists for 50 ms, all regulators are turned off following the normal shutdown sequence. This is different from output OVP/UVP fault, where the offending regulator is shut down immediately, while other regulators are shut down in sequence.

Overcurrent Protection Mechanisms for AVDD, VCOM, VGH and VGL

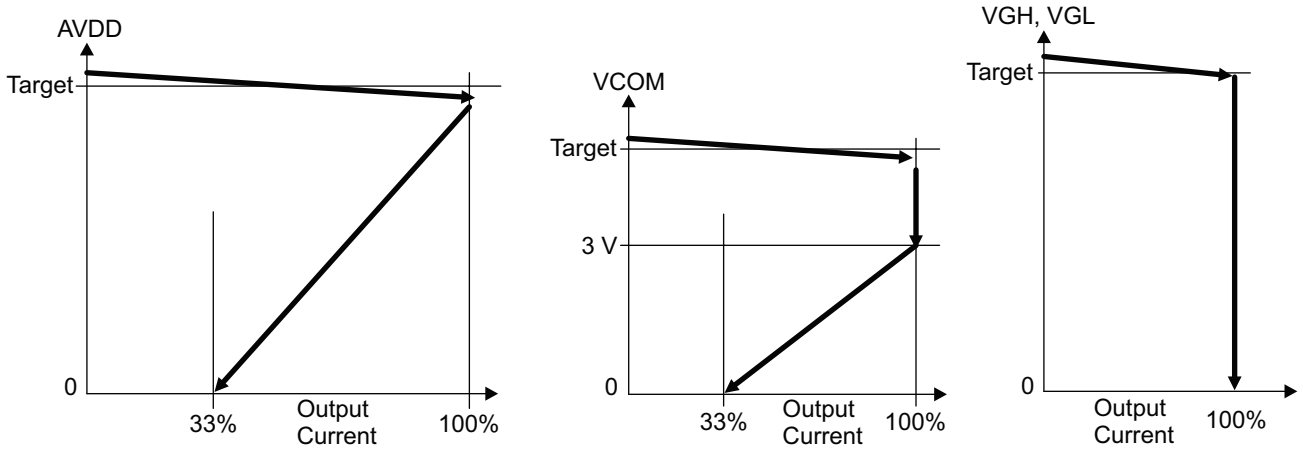

Figure 12: Regulator Current Fold-Back in Case of Overcurrent Conditions

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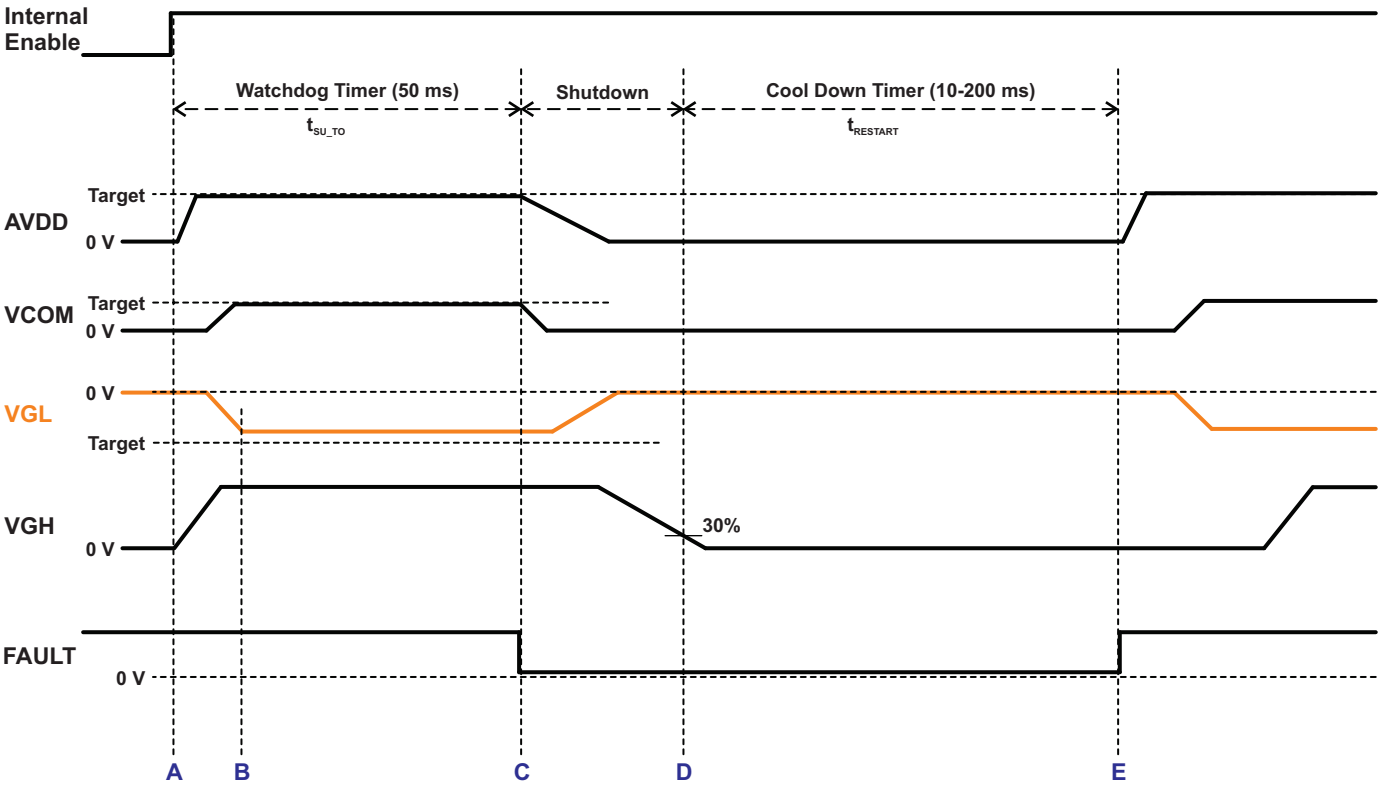
Overcurrent Protection

Each output regulator has a built-in current limit to prevent damages from overcurrent. During startup, a regulator may initially operate in overcurrent protection mode while its output capacitor is being charged. Normally, the current will reduce once the output voltage has reached target value. In case there is an output short, or if the output capacitor is much larger than expected, the OCP mode may last for 50 ms. At this point, an OCP fault is generated. The IC then begins to shut down all regulators according to programmed shutdown sequence.

Examples of Various Fault Conditions



Sequence of events:

A: User issues I²C command to set INT_EN = H, to enable all output regulators.

B: During startup, VGL is unable to reach its regulation target due to an output short or unexpected heavy load.

C: After Watchdog Timer expired, the A8603 reports that a fault has occurred (by asserting FALUT = L) and begins to shutdown all its output regulators in normal sequence. Fault counter is incremented by 1.

D: When the last regulator (VGH in this case) has finished shutdown, the A8603 waits for a cooldown period (programmable between 10 and 200 ms).

E: Retry startup as long as the maximum number or retries (programmable between 0 and 15) is not exceeded.

Figure 13: Timing Diagram where VGL Failed to Reach Its Target Voltage at Startup

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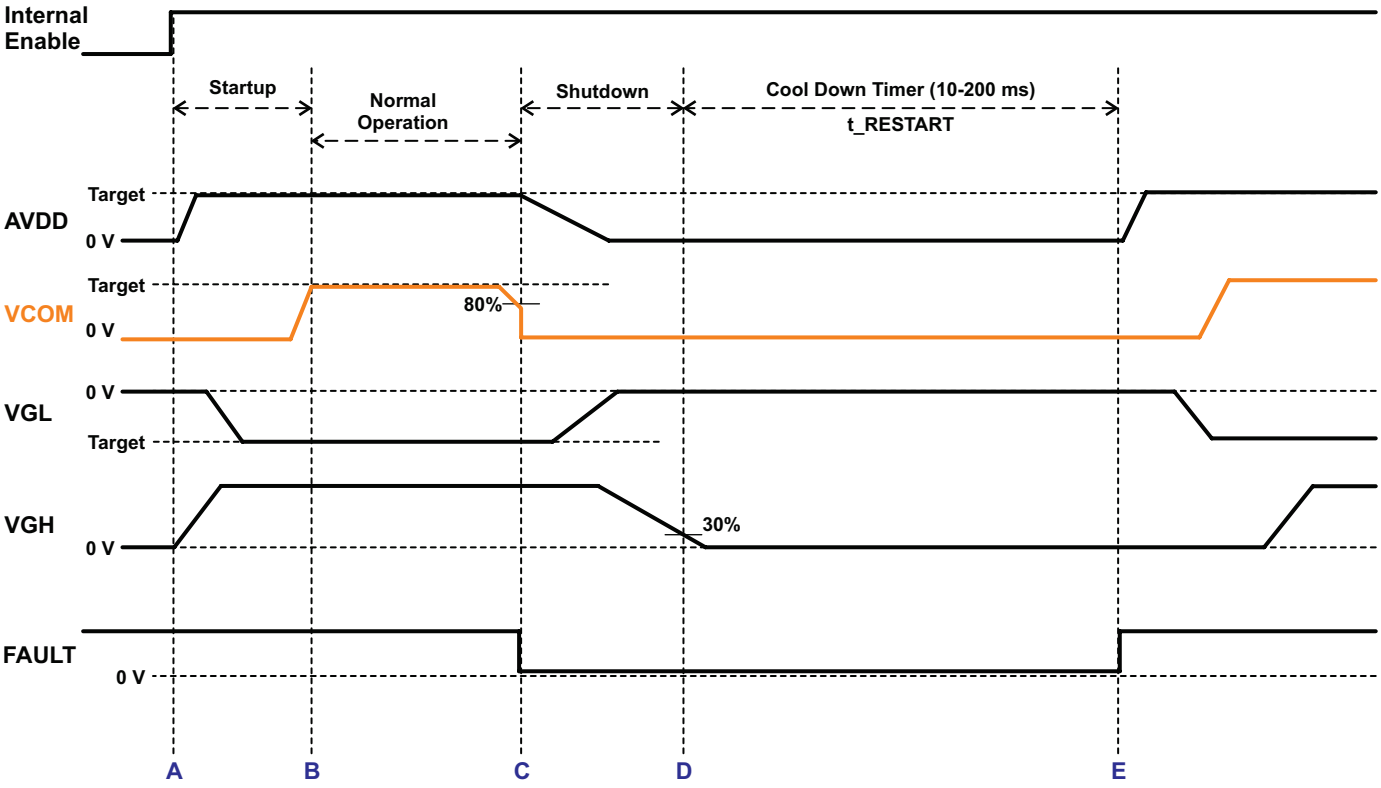

Sequence of events:

A: User issues I²C command to set INT_EN = H, to enable all output regulators.

B: Startup is completed successfully when the last regulator (VCOM in this case) has reached 90% target voltage.

C: VCOM output voltage drops to below 80% target due to an output short or unexpected heavy load. The A8603 detects an Output_UVP fault and shuts down VCOM immediately. All other regulators are then shut down in normal sequence.

D: When the last regulator (VGH in this case) has finished shutdown, the A8603 waits for a cooldown period (programmable between 10 and 200 ms).

E: Retry startup as long as the maximum number or retries (programmable between 0 and 15) is not exceeded.

Figure 14: Timing Diagram where VCOM Suffered an Output Undervoltage Fault during Normal Operation

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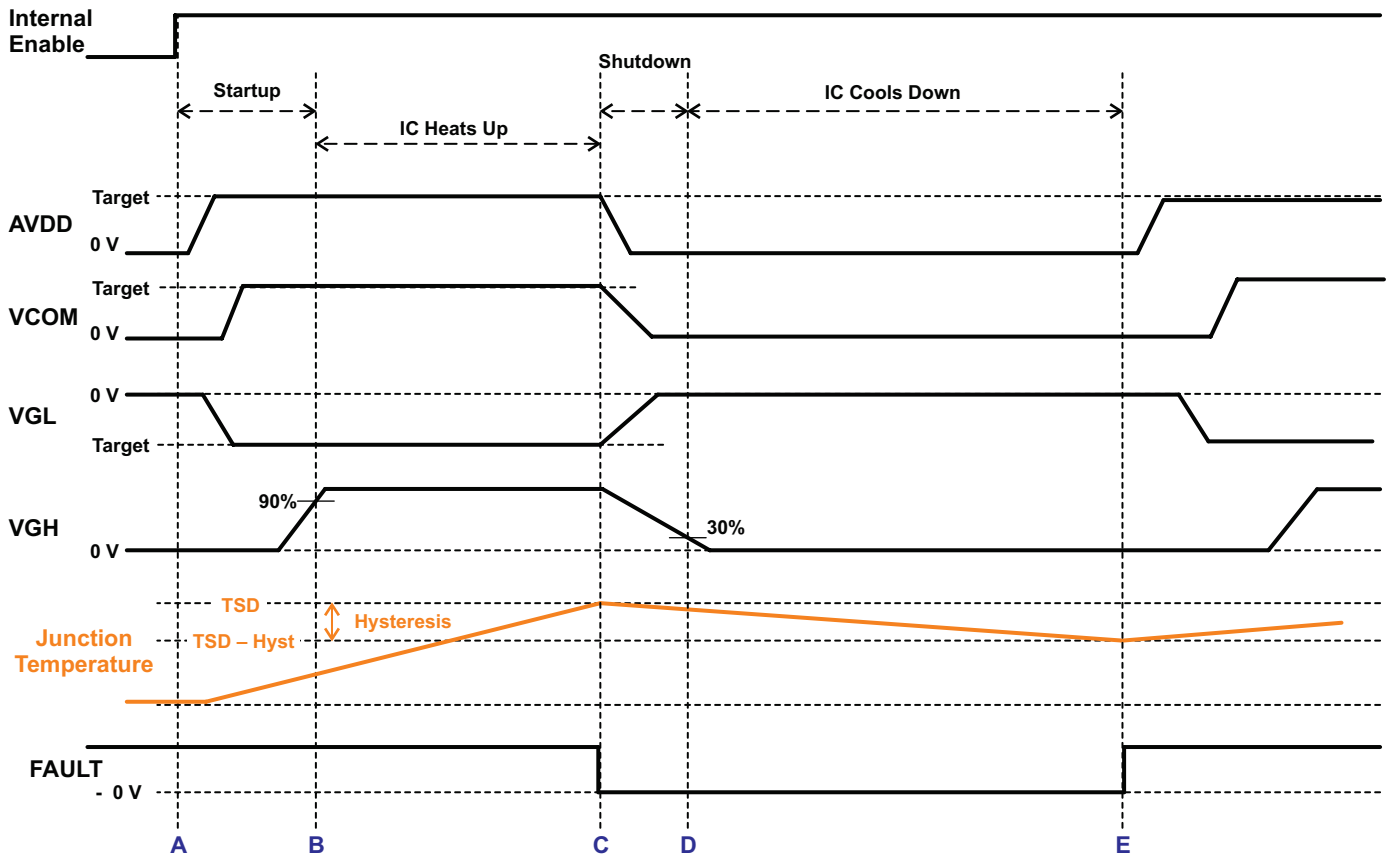

Sequence of events:

A: User issues I²C command to set INT_EN = H, to enable all output regulators.

B: Startup is completed successfully when the last regulator (VGH in this case) has reached 90% target voltage.

C: During operation, should the junction temperature rises to TSD threshold (due to high ambient temperature or unexpected heavy load), the IC turns off all output regulators immediately without following normal shutdown sequence. FAULT is pulled low and fault counter is incremented by 1.

D: After shutdown is completed, the IC waits for junction temperature to drop to TSD-Hyst (typically 20°C below TSD) before attempting retry.

E: Retry startup as long as the maximum number or retries (programmable between 0 and 15) is not exceeded.

Figure 15: Timing Diagram Showing a Thermal Shutdown and Restart

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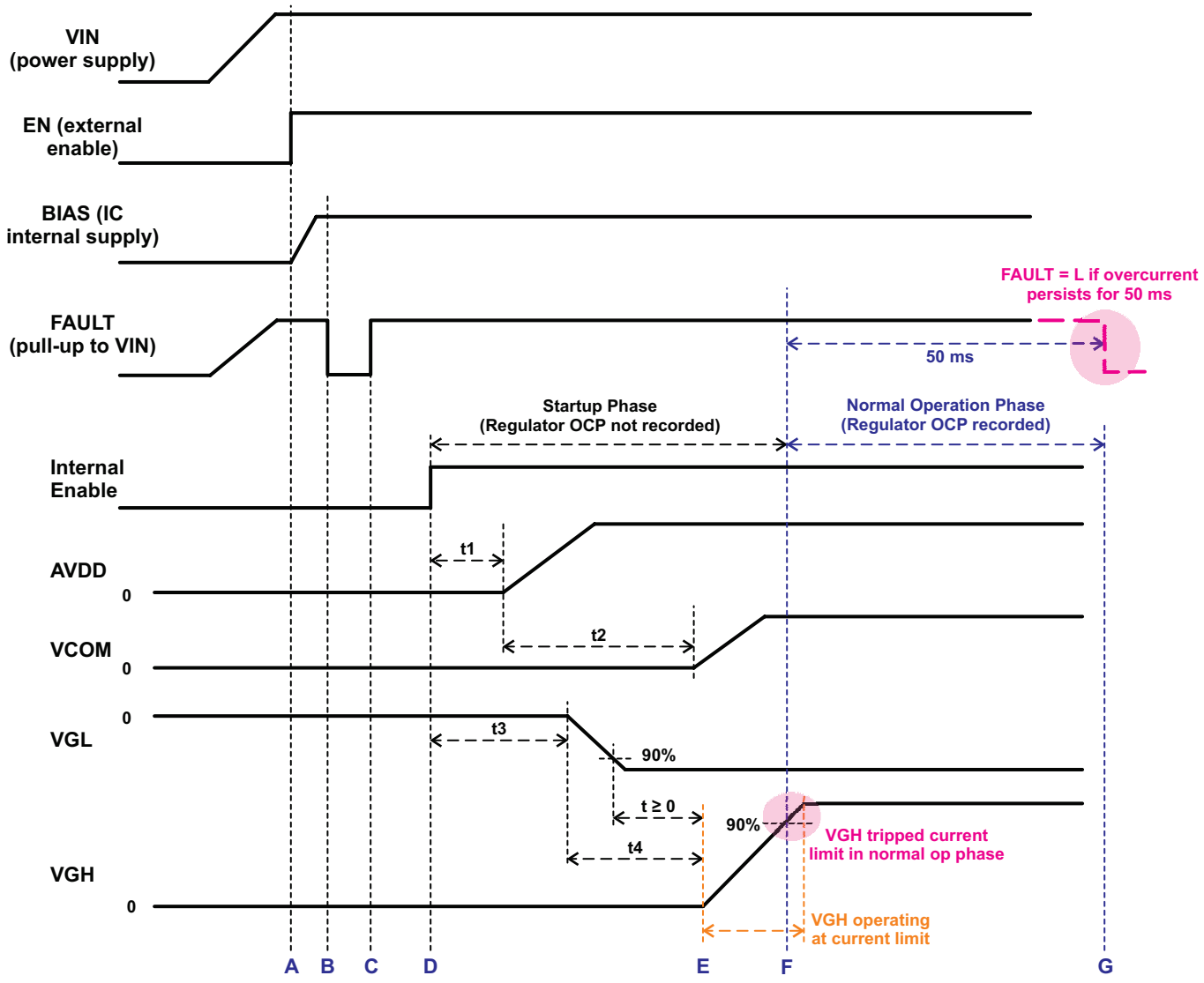

Sequence of events:

A: System controller brings EN = H to enable the A8603.

B: After A8603 performs a POR (Power-On Reset), it pulls down FAULT flag to signal that it is ready for I²C commands.

C: System controller detected FAULT = L and sends in I²C command to clear the POR status bit. This resets FAULT to H (unless there were other faults detected).

D: After programming the A8603 registers, system controller sets the internal_enable bit to 1, to turn on all output regulators.

E: The last regulator (VGH in this example) starts charging.

F: When all regulators have reached 90% of regulation target, the A8603 declares Startup Phase over and enters into normal operation phase. However, VGH is still operating at its current limit, to charge its output cap to 100% . Therefore A8603 records this overcurrent status in Reg0x18, bit3. This is not considered a fault.

G: During normal operation phase, if any regulator shows overcurrent for 50 ms, then the A8603 will pull FAULT = L and shutdown all regulators in sequence.

Figure 16: Timing Diagram Showing when a Regulator Overcurrent Condition is Reported

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Pre-Output Fault Detection

When EN = High and the A8603 output regulators are enabled through I^2C command, a startup sequence is followed before the regulators are powered up. The sequence checks for extreme conditions and proceeds as described in Table 16.

General Fault Detection

The faults described in Table 17 are continuously monitored, whether during startup, normal operation, or shutdown.

Table 16: Pre-Output Fault Detection Sequence

Step Number	Step Description	Step Description	Fault Tripped?
1	Check VIN UVLO	A8603 remains powered-down until V_{IN} is above V_{UVLO}.	No
2	Power-up internal rail	A8603 initializes.	No
3	Check internal rail UVLO	BIAS charges internal rail indefinitely, until V_{BIAS} is above UVLO.	No
4	Turn on AVDD	Enable AVDD and check to see if output reaches >90% of target voltage within $t_{SS(TO)}$.	Yes
5	Turn on VGL	Enable VGL and check to see if output reaches >90% of target voltage within $t_{SS(TO)}$.	Yes
6	Turn on VGH	Enable VGH and check to see if output reaches >90% of target voltage within $t_{SS(TO)}$.	Yes
7	Turn on VCOM	Enable VCOM and check to see if output reaches >90% of target voltage within $t_{SS(TO)}$.	Yes

Table 17: General Fault Detection

Fault Description	A8603 Response to Fault	Fault Tripped?
AVDD, VCOM,VGH or VGL 20% under target	Shutdown using shutdown sequence. Fault counter increased by one, retry after $t_{RESTART}$.	Yes: FAULT set during $t_{RESTART}$.
AVDD, VCOM,VGH or VGL 20% over target	Over target regulator rail shutdown immediately. Other regulator rails shutdown using shutdown sequence. Fault counter increase by one retry after $t_{RESTART}$.	Yes: FAULT set during $t_{RESTART}$.
Overcurrent limit for i_{AVDD}, i_{VCOM}, i_{VGH} or i_{VGL}	Offending regulator rail goes into current fold-back or current limit. Shutdown using shutdown sequency after t_{OCP}. Fault counter increase by one, retry after $t_{RESTART}$.	Yes: FAULT set during $t_{RESTART}$.
SW_OVP exceeded	Shutdown all regulators immediately without using shutdown sequence. Fault counter increased by one, retry after $t_{RESTART}$.	Yes: FAULT set during $t_{RESTART}$.
External UVLO reached	Shutdown all regulators immediately without using shutdown sequence. Fault counter reset to 0, retry after $t_{RESTART}$.	No
Internal (Bias) UVLO	Shutdown all regulators immediately without using shutdown sequence. Fault counter reset to 0, retry after $t_{RESTART}$.	No
TSD exceeded	Shutdown all regulators immediately without using shutdown sequence. Fault counter increase by one, retry after $t_{RESTART}$.	Yes: FAULT set during $t_{RESTART}$.
SWILIM2 (150% of cycle-by-cycle limit) exceeded	Shutdown all regulators immediately without using shutdown sequence. Fault counter increased by one, retry after $t_{RESTART}$.	Yes: FAULT set during $t_{RESTART}$.

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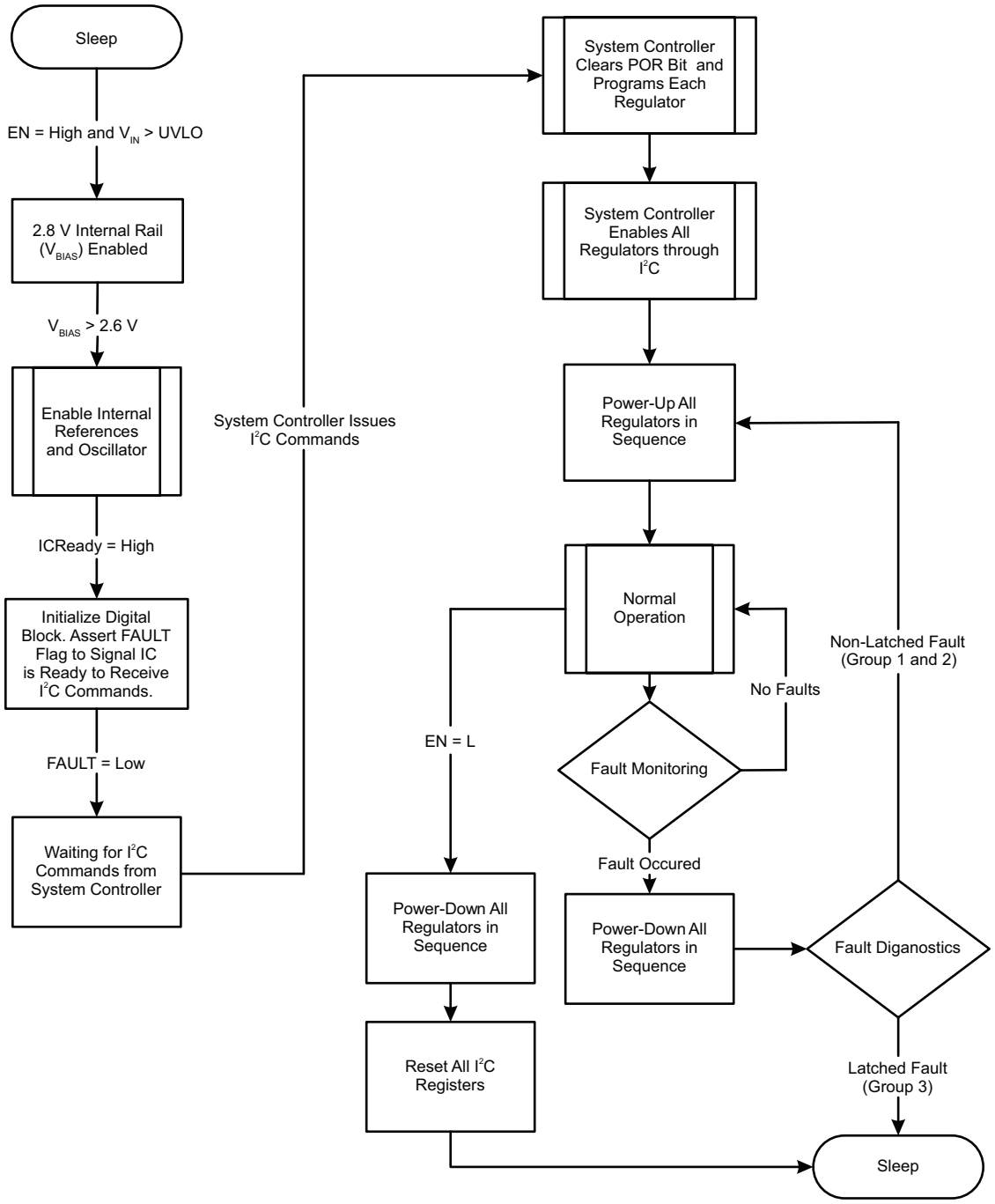

Figure 17: Fault Checking During Startup and Normal Operation

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Fault Monitoring

The fault monitoring system prioritizes the fault in three different categories. Based on the severity of the fault, diagnostic algorithm handle the shutdown sequence of all regulators.

FAULT1 (GROUP1)

If any fault from the below list is detected, the A8603 halts operation and pulls the FAULT pin low. All regulators shut down in sequence. It then attempts to restart operation after a delay, $t_{RESTART}$ (default 100 ms). Internally, there is a fault counter that keeps tracks of how many times any fault has occurred. If the fault counter reaches its programmed limit (default 8), the A8603 is completely shutdown. A hardware reset (either by EN = L or V_{IN} below UVLO) is then required before the A8603 can restart.

Startup Fail	Regulator output voltage fails to reach 90% of its target voltage within timeout period
Regulator Undervoltage	Regulator output voltages are below 80% of the target voltage. This signal is ignored during startup.
Regulator Overvoltage	Regulator output voltage are above 120% of the target voltage. This signal is ignored during startup.
Regulator Overcurrent	Regulator output currents are above the current limit threshold. This signal is ignored during startup.
FSET Shorted	FSET pin shorted to ground. IC moves to internal fixed 1 MHz oscillator.

- Each regulator output is protected by its own independent overcurrent limit. When an output current exceeds its limit, the corresponding regulator goes in to overcurrent protection mode to protect itself from damage. If the overcurrent condition persists for 50 ms, all regulators are turned off following the normal shutdown sequence.
- Each regulator output is protected by its own overvoltage fault detection. When an output voltage exceeds its limit, the corresponding regulator is turned off immediately. The other outputs then shut down following normal sequence. The same applies to undervoltage fault detection.
- When FSET pin is shorted to ground, IC begins a shutdown sequence, at the switching frequency set by the internal 1 MHz oscillator. The FAULT pin is pulled low and the internal error counter is increased by 1.

FAULT2 (GROUP2)

When following faults are detected, the A8603 halts operation and pulls the FAULT pin low. All outputs are shut off immediately. It then attempts to restart operation after a delay, $t_{RESTART}$ (default 100 ms). Internally, there is a fault counter that keeps tracks of how many times any fault has occurred. If the fault counter reaches its programmed limit (default 8), the A8603 is completely shut down. A hardware reset (either by EN = L or V_{IN} below UVLO) is then required before the A8603 can restart.

SW Overvoltage	SW pin voltage exceeds SW_{OVP}
SW Overcurrent	SW pin current exceeds $I_{SWILIM2}$.
Thermal Shutdown	IC die temperature exceeds T_{TSD}

FAULT3 (GROUP3)

When a supply undervoltage fault is detected, the A8603 shuts down immediately. All outputs are turned off without following the shutdown sequence. All digital states are erased. The FAULT flag will not be asserted. The device will not attempt to restart.

VIN UVLO	V_{IN} (input supply) is below 2.8 V.
BIAS UVLO	V_{BIAS} (internal rail) is below 2.6 V.

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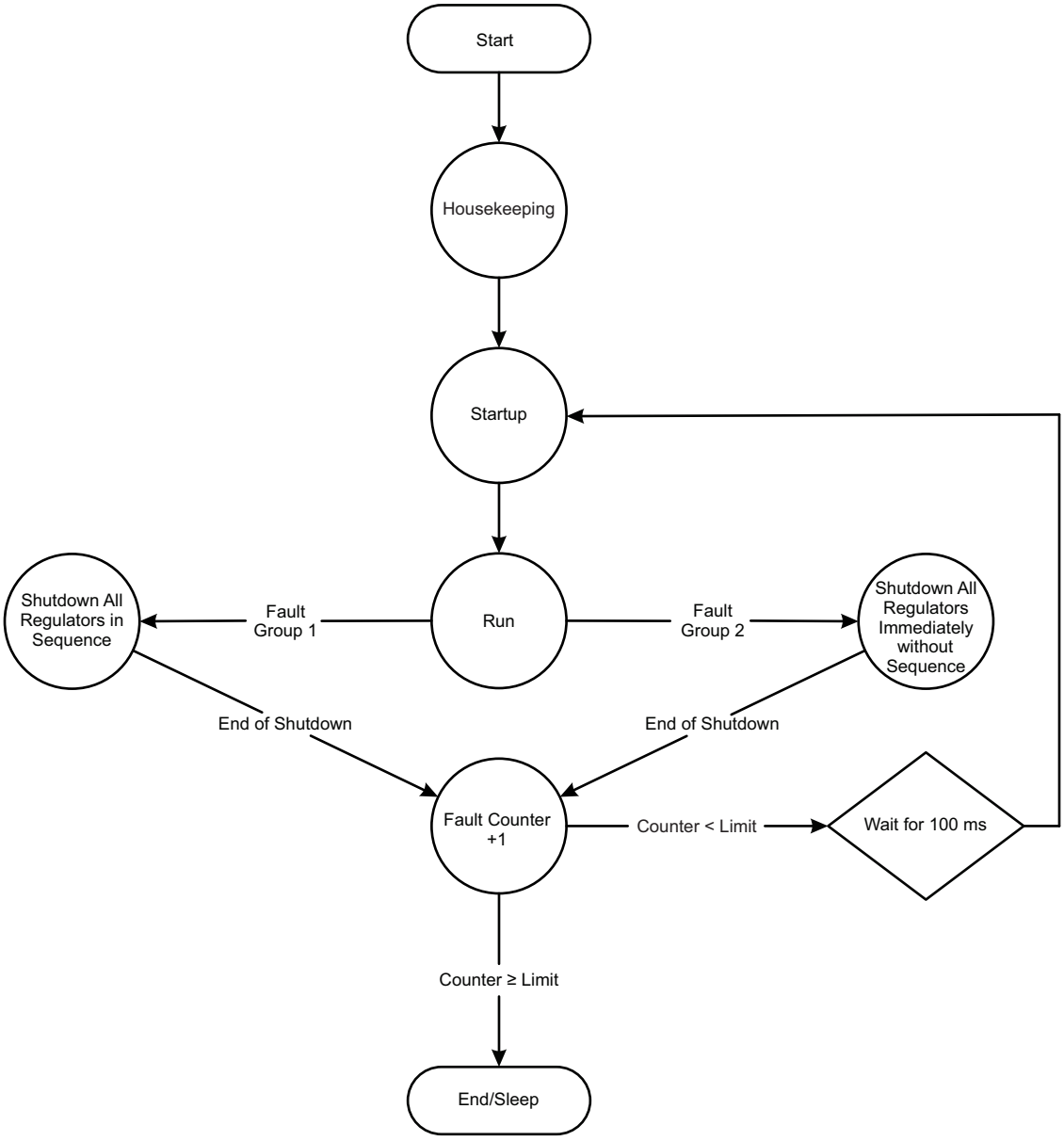

Figure 18: Fault-Retry Counter

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THERMAL ANALYSIS

The thermal resistance, $R_{\theta JA}$, of the QFN-24 thermally enhanced package is 37°C/W. For long-term reliability, the package junction temperature should be kept at 150°C or below. Assuming a maximum ambient temperature of 85°C, the power dissipation budget, $P_{D(max)}$, is:

$$P_{D(max)} = (T_{J(max)} - T_{A(max)})/R_{\theta JA}$$

$$= (150\ (°C) - 85\ (°C))\ /\ 37\ (°C/W) = 1.75\ W$$

The power losses of the IC come from two main contributors: the boost stage and the output regulators. These losses are calculated separately, and then summed as follows.

Boost Stage Power Loss

To estimate the dissipation of the boost stage, calculate and sum the losses due to switching losses, P_{SW}, and conduction losses in the switch, P_{COND}:

$$P_{D(BOOST)} = P_{COND} + P_{SW}$$

As an example, consider the following load conditions:

	AVDD	VCOM	VGL	VGH	Boost
Voltage (V)	10	4	-8	18	12.1
Max. Current (mA)	100	4	2	2	110

1. Estimate the maximum output power for boost stage:

$$P_{OUT(max)} = V_{OUT(max)} \times I_{OUT\ (max)}$$

$$I_{OUT} = I_{AVDD} + I_{VCOM} + I_{VGL} + 2 \times I_{VGH}$$

Based on the above load conditions, we conclude that Boost V_{OUT} = 12.1 V (see "Boost Controller" section for explanation) and I_{OUT} = 110 mA. Therefore $P_{OUT(max)}$ = 12.1 V × 0.11 A = 1.33 W

2. Estimate the maximum input current:

$$I_{IN} = P_{IN}/V_{IN}$$

$$P_{IN} = P_{OUT}/\eta$$

where η is efficiency.

Assume minimum V_{IN} of 3 V and a conservative efficiency of 80%:

$$I_{IN} = (1.33\ W/0.8)/3\ V = 0.55\ A.$$

3. Estimate conduction loss for the internal switch:

$$P_{COND} = (I_{IN})2 \times R_{DS(on)} \times D$$

$$D = 1 - V_{IN}/(V_{OUT} + V_D)$$

where D = Duty Cycle of boost switch, V_D is the forward voltage drop of the external boost diode.

Substitute minimum V_{IN} = 3 V, V_{OUT} = 12.1 V, V_D = 0.4 V to get D = 0.76.

$$P_{COND} = (0.55\ A)2 \times 0.7\ \Omega \times 0.76 = 0.16\ W$$

Note that $R_{DS(on)}$ is 0.5 Ω typical, plus 40% for temperature compensation at 125°C.

4. Estimate switching loss for the internal boost switch:

$$P_{SW} = I_{SW} \times V_{SW} \times (t_r + t_f) \times f_{SW}/2$$

Where $I_{SW} = I_{IN}$ approximately, $V_{SW} = V_{OUT} + V_D$; t_r is the rise time, and t_f the fall time, of V_{SW}.

Assume $t_r = t_f$ = 10 ns,

$$P_{SW} = 0.55\ A \times 12.5\ V \times (10\ ns + 10\ ns) \times 2\ MHz/2 = 0.14\ W$$

Therefore the total power dissipation on the boost stage is:

$$P_{D(BOOST)} = P_{COND} + P_{SW} = 0.30\ W$$

Output Regulator Power Loss

The output regulator power dissipation is the sum of the individual linear regulators:

$$P_{D(REG)} = P_{LDO1} + P_{LDO2} + P_{LDO3} + P_{LDO4}$$

Where LDO1-4 are linear regulators for AVDD, VCOM, VGL and VGH, respectively.

$$P_{LDO1} = (V_{OUT} - V_{AVDD}) \times (I_{AVDD} + I_{VCOM})$$

$$P_{LDO2} = (V_{AVDD} - V_{VCOM}) \times I_{VCOM}$$

$$P_{LDO3} = (V_{OUT} - |V_{VGL}|) \times I_{VGL}$$

$$P_{LDO4} = (V_{OUT} - V_{VGH}/2) \times 2 \times I_{VGH}$$

Using the previously stated operating conditions, we then have:

$$P_{LDO1} = (12.1\ V - 10\ V)\ x\ 104\ mA = 218\ mW)$$

$$P_{LDO2} = (10\ V - 4\ V) \times 4\ mA = 24\ mW$$

$$P_{LDO3} = (12.1\ V - 8\ V) \times\ 2\ mA = 8\ mW$$

$$P_{LDO4} = (12.1\ V - 18\ V/2) \times\ 2 \times 2\ mA = 12\ mW$$

Finally, the IC consumes a bias current of approximately 5 mA

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from VIN when output regulators are enabled. This adds power consumption of approximately 15 mW at minimum V_{IN}. Therefore the sum of power dissipations for all output regulators is approximately 280 mW.

The total power dissipation of the IC is then the sum of the boost stage and the linear regulators: 0.30 W + 0.28 W = 0.58 W. This corresponds to a temperature rise of just 21.5°C. Therefore, at the highest ambient temperature of 85°C, the estimated junction temperature is 106.5°C under the above worst-case conditions.

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PACKAGE OUTLINE DRAWINGS

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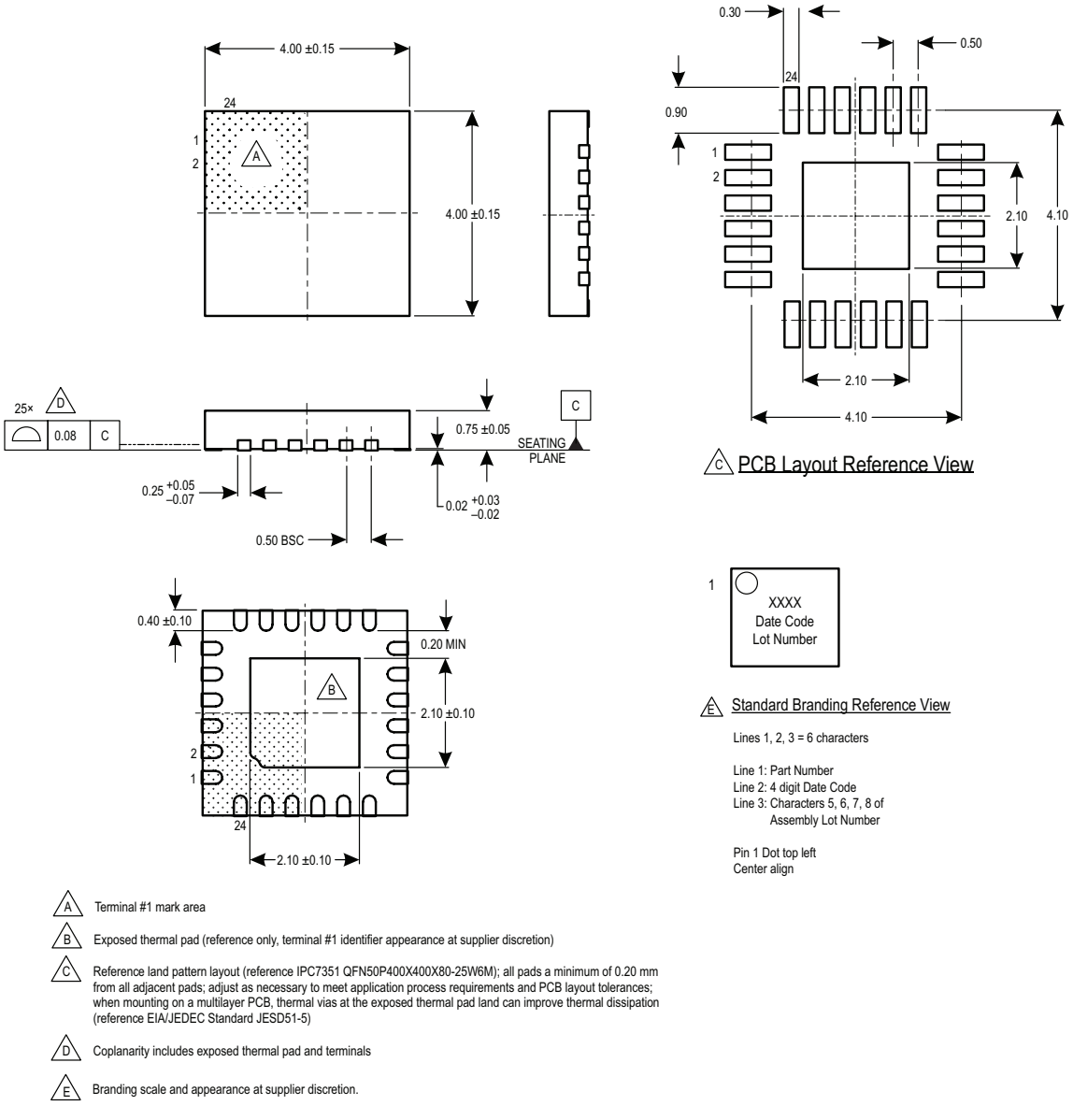
(Reference Allegro DWG-0000222 Rev. 2 or JEDEC MO-220WGGD.)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P400X400X80-25W6M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion.

Figure 20: Package ES, 24-Pin 4 mm × 4 mm QFN with Exposed Thermal Pad

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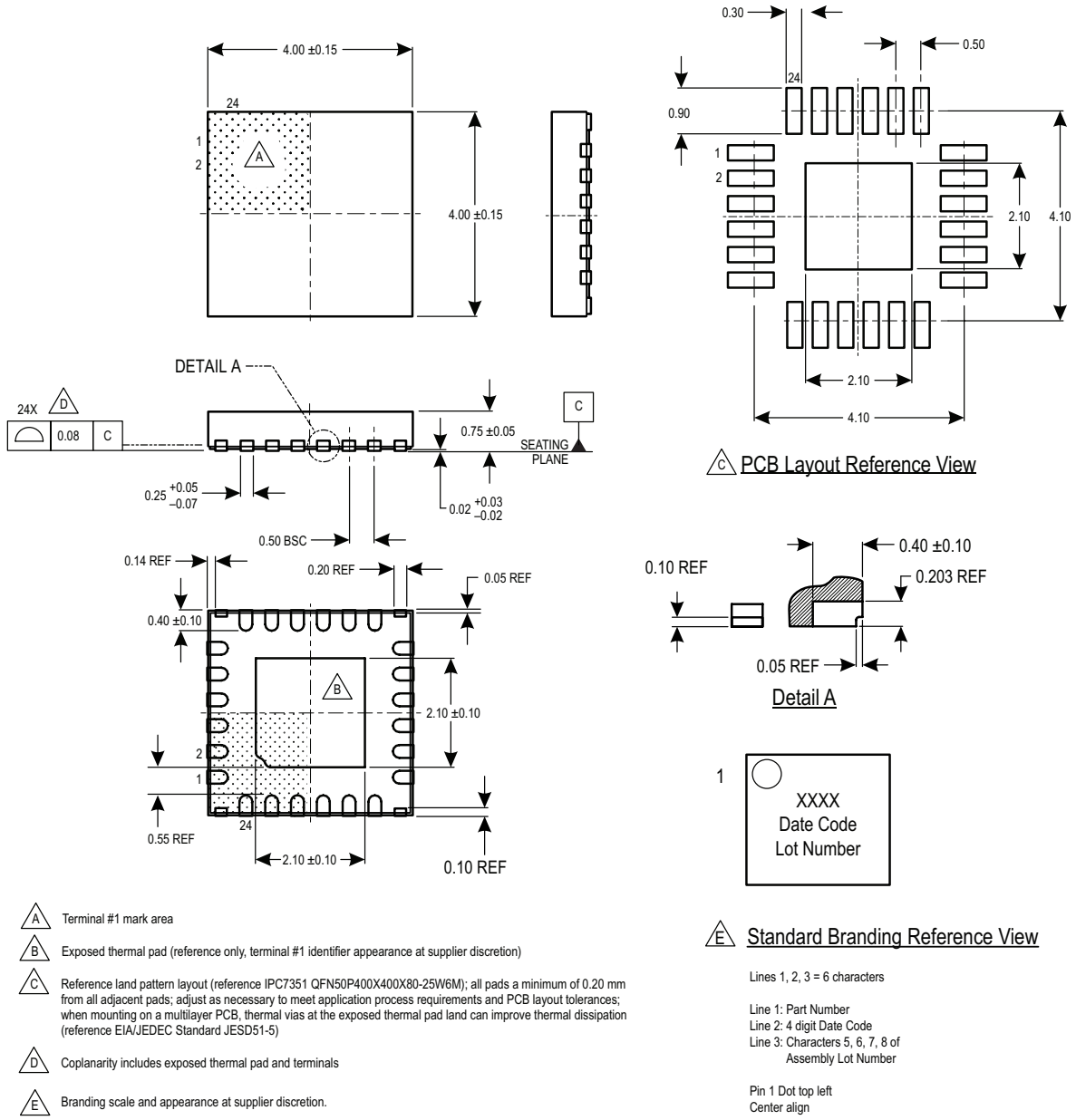
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P400X400X80-25W6M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion.

Figure 21: Package ES, 24-Pin 4 mm × 4 mm QFN with Exposed Thermal Pad and Wettable Flank

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Revision History

Revision	Revision Date	Description of Revision
–	November 17, 2014	Initial Release
1	January 20, 2015	Added Appendix A
2	March 12, 2015	Removed LP Package option
3	April 13, 2015	Corrected Table 13 title
4	October 9, 2015	Added A8603KESTR-J to Selection Guide; corrected Terminal List Table and Shutdown Timing Diagram
5	January 5, 2016	Updated Fault Conditions; corrected Package Outline Drawing
6	March 3, 2016	Corrected Packing info in Selection Guide (page 2), Absolute Maximum Rating of FAULT pin (page 3), and EN pin Pull-Down Resistance (page 7)
7	October 24, 2016	Corrected Pad corner in Pinout Diagram (page 4)
8	January 5, 2017	Updated Boost Controller section (pages 20-21); added wettable flank package option drawings (pages 1 and 36)
9	January 18, 2017	Corrected pins CP11 to CP21 and CP12 to CP22 in Figure 6: Representative Block Diagram of the VGL Negative Charge Pump Mode (page 19)
10	January 15, 2019	Minor editorial updates
11	January 27, 2020	Minor editorial updates
12	January 28, 2021	Updated Package Outline Drawings (pages 35-36).

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APPENDIX A

I²C Interface Description

The A8603 provides an I²C-compliant serial interface that exchanges commands and data between a system microcontroller (master) and the A8603 (slave). Two bus lines, SCL and SDA, provide access to the internal control registers. The clock input on the SCL pin is generated by the master, while the SDA line functions as either an input or an open drain output for the A8603, depending on the direction of the data flow.

The I²C input thresholds depend on the V_{BIAS} voltage of the A8603. The threshold levels across the operating V_{BIAS} range are compatible with 3 V logic.

Timing Considerations

I²C communication is composed of several steps, in the following sequence:

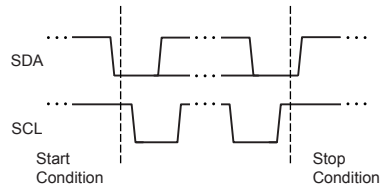
1. Start Condition. Defined by a negative edge on the SDA line, while SCL is high (see figure A-1).

2. Address Cycle. 7 bits of address, plus 1 bit to indicate write (0) or read (1), and an acknowledge bit (see figure A-2).

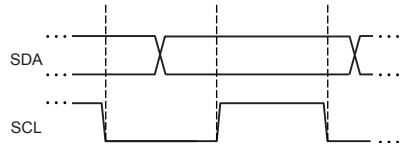
3. Data Cycles. Reading or writing 8 bits of data followed by an acknowledge bit (see figure A-2).

4. Stop Condition. Defined by a positive edge on the SDA line, while SCL is high (see figure A-1).

It is possible for the Start or Stop condition to occur at any time during a data transfer. The A8603 always responds by resetting the data transfer sequence. Except to indicate a Start or Stop condition, SDA must be stable while the clock is high (figure A-2). SDA can only be changed while SCL is low.



(A) Start and Stop conditions



(B) Clock and data bit synchronization

Figure A-1. Bit transfer on the I²C bus

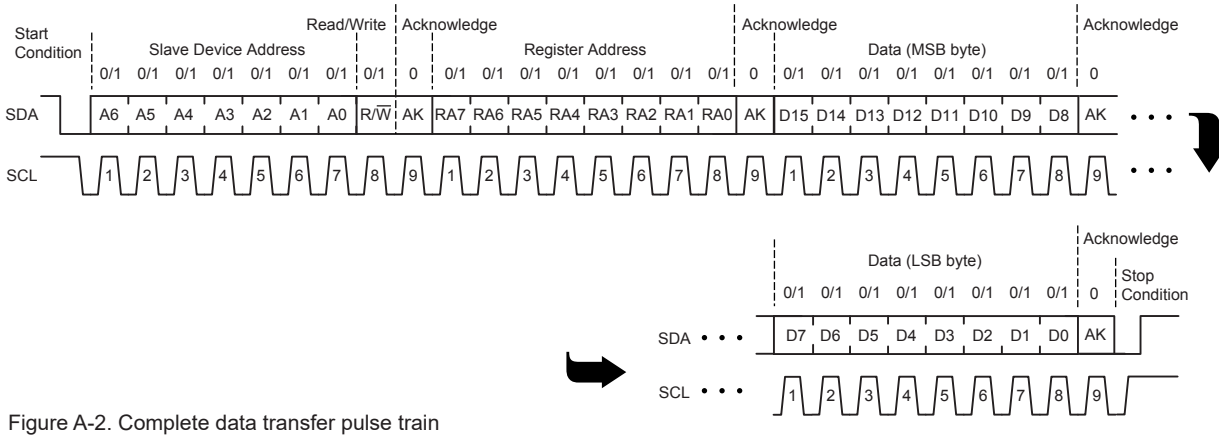


Figure A-2. Complete data transfer pulse train

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The state of the Read/Write bit (R/$\overline{W}$) is set low to indicate a Write cycle and set high to indicate a Read cycle.

The master monitors for an acknowledge bit to determine if the slave device is responding to the address byte sent to the A8603. When the A8603 decodes the 7-bit address field as a valid address, it acknowledges by pulling SDA low during the ninth clock cycle.

During a data write from the master, the A8603 pulls SDA low during the clock cycle that follows each data byte, in order to indicate that the data has been successfully received.

After sending either an address byte or a data byte, the master device must release the SDA line before the ninth clock cycle, in order to allow the handshaking to occur.

I²C Command Write to the A8603

The master controls the A8603 by programming it as a slave. To do so, the master transmits data bits to the SDA input of the A8603, synchronized with the clocking signal the master transmits simultaneously on the SCL input (figure A-3).

A complete transmission begins with the master pulling SDA low (Start bit), and completes with the master releasing the SDA line (Stop bit). Between these points, the master transmits a pattern of address bits with a Write command bit (R/$\overline{W}$), then the register

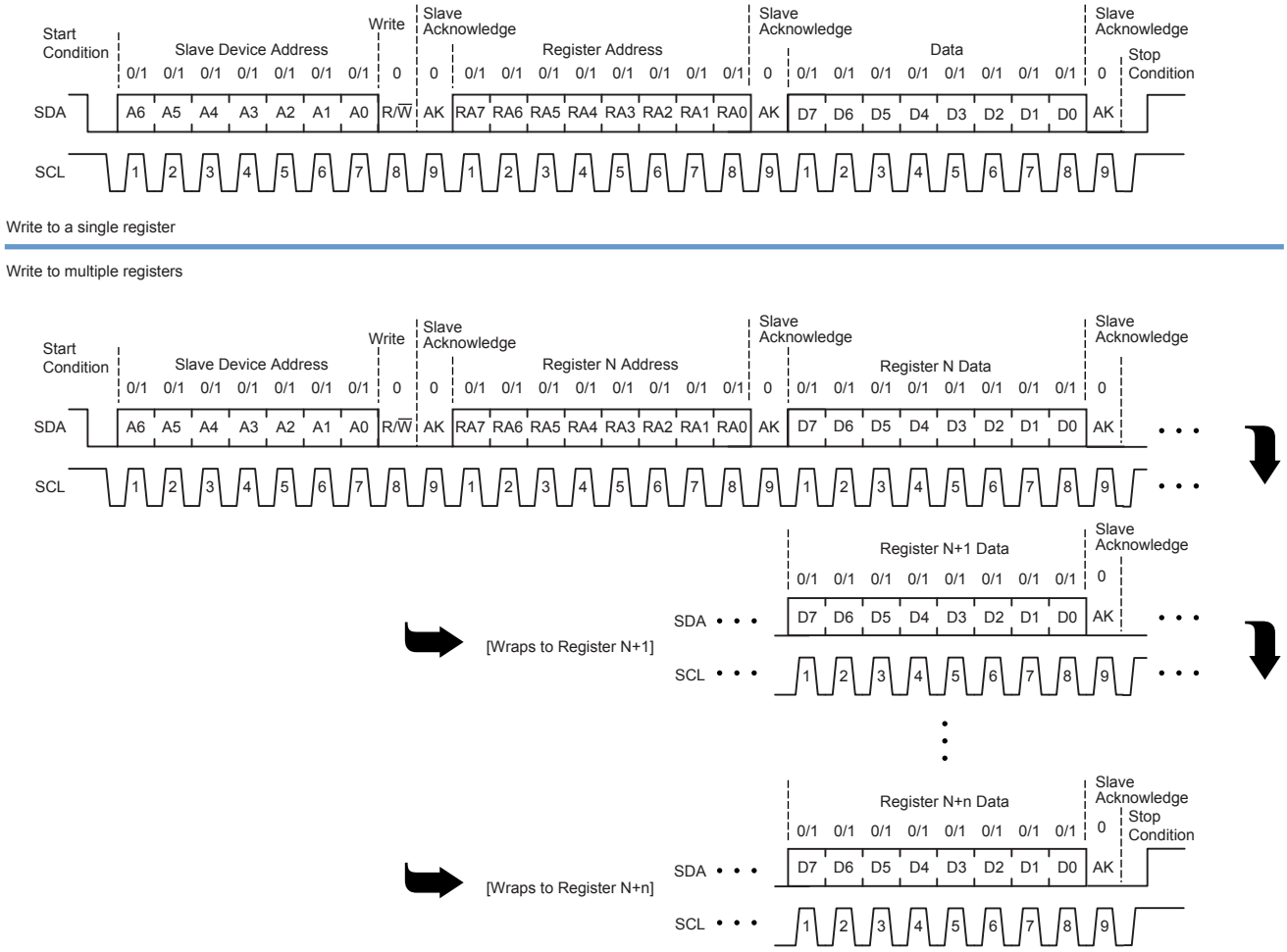

Figure A-3. Writing to single and to multiple registers

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address, and finally the data. The address therefore consists of two bytes, comprised of the A8603 chip address, with the write enable bit, followed by the address of the individual register.

After each byte, the slave A8603 acknowledges by transmitting a low to the master on the SDA line. After writing data to a register the master must provide a Stop bit if writing is completed. Otherwise, the master can continue sending data to the device and it will automatically increase the register value by one for additional data byte. This allows faster data entry but restricts the data entry to sequential registers.

I²C Command Read from the A8603

The master can read back the register values of the A8603. The Read command is given in the R/$\overline{W}$ bit of the address byte. To do so, the master transmits data bits to the SDA input of the A8603, synchronized with the clocking signal the master transmits simultaneously on the SCL input. The pulse train is shown in figure A-4. A complete transmission begins with the master pulling SDA low (Start bit), and completes with the master releasing the SDA pin (Stop bit). Between these points, the master transmits a pattern of chip address with the Read command (R/$\overline{W}$ = 1) and then the address of the register to be read. Again, the address consists of two bytes, comprising the address of the A8603 (chip address) with the read enable bit, followed by the address of the individual register. The bus master then executes a Master Restart, reissues the slave address, then the A8603 exports the data byte for that register, synchronized with the clock pulse supplied by the master. The master must provide the clock pulses, as the A8603 slave does not have the capability to generate them.

If the master does not send an non-acknowledge bit (AK = 1) after receiving the data, the A8603 will continue sending data from the sequential registers after the addressed one, as shown in figure A-3. After the master provides an non-acknowledge bit, the A8603 will stop sending the data. After that, if additional register reads are required, the process must start over again.

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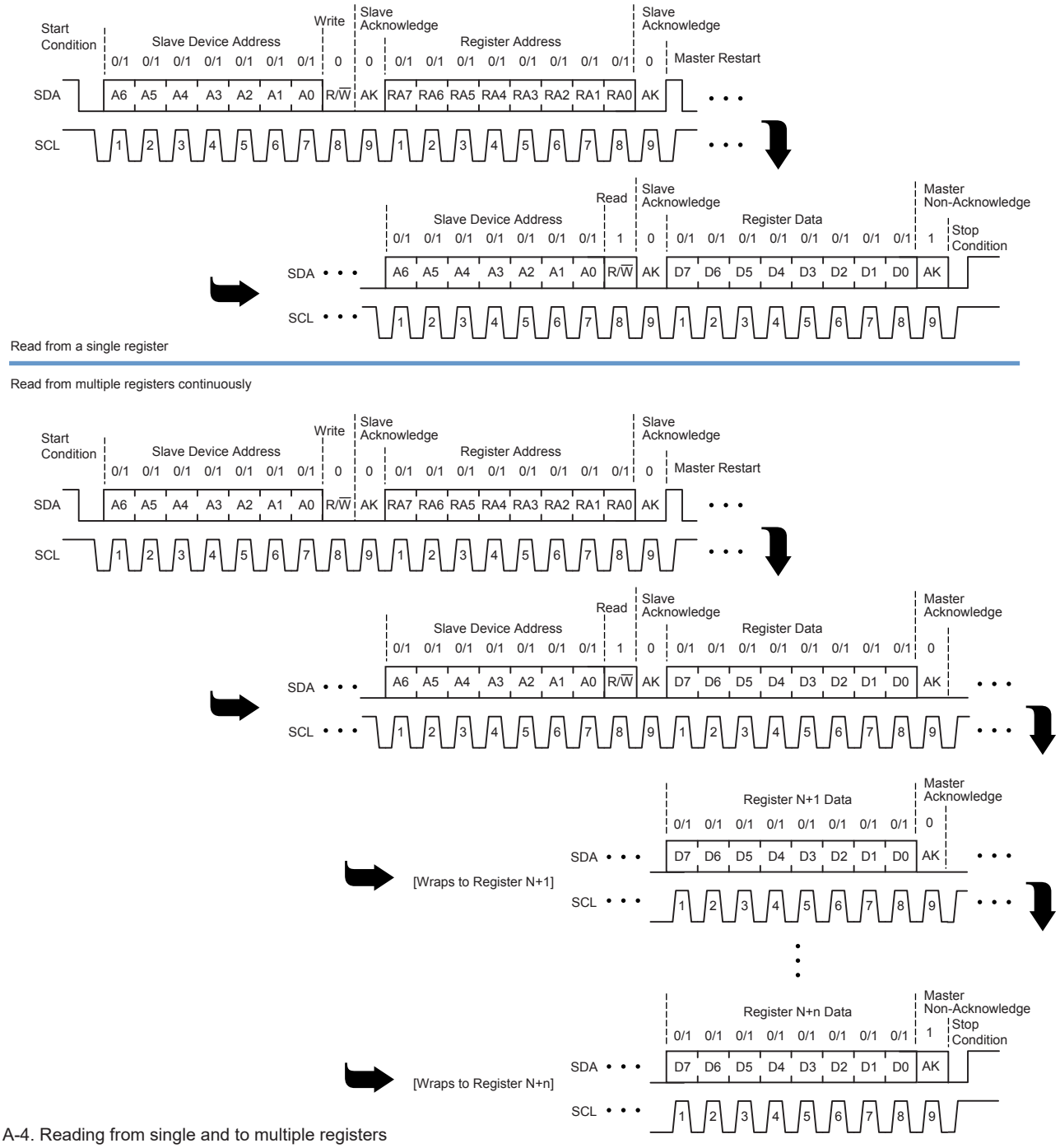

Figure A-4. Reading from single and to multiple registers

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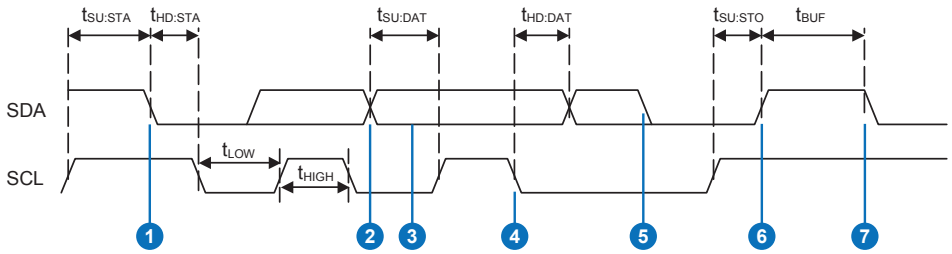
I²C-Compatible Interface Timing Diagram



1. Start
2. SDA can change state only when SCL = low
3. SDA must be stable before SCL goes high

4, 5. SCL and SDA output fall time < 250 ns

6. Stop
7. Restart

I²C-Compatible Timing Requirements

Characteristics	Symbol	Min.	Typ.	Max.	Units
Bus Free Time Between Stop/Start	t_{BUF}	1.3	–	–	µs
Hold Time Start Condition	$t_{HD:STA}$	0.6	–	–	µs
Setup Time for Start Condition	$t_{SU:STA}$	0.6	–	–	µs
SCL Low Time	t_{LOW}	1.3	–	–	µs
SCL High Time	t_{HIGH}	0.6	–	–	µs
Data Setup Time	$t_{SU:DAT}$	100	–	–	ns
Data Hold Time*	$t_{HD:DAT}$	0	–	900	ns
Setup Time for Stop Condition	$t_{SU:STO}$	0.6	–	–	µs
Output Fall Time from $V_{SCL(H)}$ to $V_{SCL(L)}$	t_{OF}	–	–	250	ns

*For $t_{HD:DAT}$(min), the master device must provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the SCL signal falling edge.

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