

PIC12(L)F1571/2 Family Silicon Errata and Data Sheet Clarification

The PIC12(L)F1571/2 family devices that you have received conform functionally to the current Device Data Sheet (DS40001723D), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).


The errata described in this document will be addressed in future revisions of the PIC12(L)F1571/2 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (**A0**).

Data Sheet clarifications and corrections start on [page 4](#), following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
 - a) For MPLAB IDE 8, select *Programmer > Reconnect*.
 - b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ().
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC12(L)F1571/2 silicon revisions are shown in [Table 1](#).

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID	Revision ID (Silicon Revision)
		A0
PIC12F1571	3051h	2000h
PIC12LF1571	3053h	2000h
PIC12F1572	3050h	2000h
PIC12LF1572	3052h	2000h

- Note 1:** The Revision ID and Device ID are located in the Configuration memory at addresses 8005h and 8006h, respectively.
- 2:** Refer to the “*PIC12(L)F1571/2 Memory Programming Specification*” (DS40001713) for detailed information on Device and Revision IDs for your specific device.

PIC12(L)F1571/2

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revision ⁽¹⁾
				A0
Enhanced Universal Synchronous Receiver Transmitter (EUSART)	Transmit mode	1.1	Possible duplicate byte transmitted.	X
16-Bit Pulse-Width Modulation (PWM)	Continuous Run Slave Offset	3.1	Anomalous behavior	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A0**).

1. Module: Enhanced Universal Synchronous Receiver Transmitter (EUSART)

1.1 Transmit Mode

Under certain conditions, a byte written to the TXREG register can be transmitted twice. This happens when a byte is written to TXREG just as the TSR register becomes empty. This new byte is immediately transferred to the TSR register, but also remains in the TXREG register until the completion of the current instruction cycle. If the new byte in the TSR register is transmitted before this instruction cycle has completed, the duplicate in the TXREG register will subsequently be transferred to the TSR register on the following instruction clock cycle and transmitted.

Work around

1. Monitor the Transmit Interrupt Flag bit (TXIF). Writes to the TXREG register can be performed once the TXIF bit is set, indicating that the TXREG register is empty.
2. Monitor the TMRT bit of the TXxSTA register. Writes to the TXREG register can be performed once the TMRT bit is set, indicating that the Transmit Shift Register (TSR) is empty.

Affected Silicon Revisions

A0								
X								

2. Module: 16-Bit Pulse-Width Modulation (PWM)

3.1 Continuous Run Slave Offset Mode Anomaly

The 16-bit PWM in Continuous Run Slave mode (PWMxOFTCON<6:5>=11) may get stuck in anomalous behavior. The behavior is that the slave PWM output will toggle when the master PWM matches the master PWM offset value, then toggle again on the next master offset match event. The slave PWM output will then remain steady for the number of master periods equal to the slave PWM period value, after which the sequence repeats. The slave PWM may occasionally start to operate as described by either writing the slave PWMxOFTCON register or enabling the slave PWM from an Idle state.

Work around

None.

Affected Silicon Revisions

A0							
X							

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Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001723D).

<p>Note: Corrections are shown in bold. Where possible, the original bold text formatting has been removed for clarity.</p>

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (11/2013)

Initial release of this document.

Rev B Document (05/2015)

Data Sheet Clarifications: Added Module 1.

Rev C Document (09/2015)

Added Modules 1 and 2 (EUSART and 16-Bit PWM);
Other minor corrections.

Data Sheet Clarifications: Removed Module 1 (Data
Sheet updated).

Rev D Document (06/2017)

Changed the text in Module 1, Section 1.1, Work
around section. Other minor corrections.

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