Ordering number : ENA1408B

LV49152V

ON Semiconductor®

http://onsemi.com

Bi-CMOS LSI

Class-D Audio Power Amplifier BTL 15W × 2ch

Overview

The LV49152V is a 15W per channel stereo digital power amplifier that takes analog inputs. The LV49152V uses unique Our developed feedback technology to achieve excellent audio quality despite being a class D amplifier and can be used to implement high quality flat display panel (FDP) based systems.

Features

- BTL output, class D amplifier system
- Unique Our developed feedback technology achieves superb audio quality
- High-efficiency class D amplifier
- Soft muting function reduces impulse noise at power on/off
- Full complement of built-in protection circuits : over current protection, thermal protection, and low power supply voltage protection circuits
- Built in Power limiter

Functions

- Power : 15W × 2ch output (VD = 15V, R_L = 8Ω, fin = 1kHz, AES17, THD + N = 10%)
- Efficiency : 93% (VD = 15V, R_L = 8Ω, fin = 1kHz, P_O = 15W)
- THD + N : 0.08% (VD = 15V, R_L = 8Ω, fin = 1kHz, P_O = 1W, Filter : AES17)
- Noise : 90μVrms (Filter : A-weight)
- Package SSOP44J (275mil)

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	VD	Supply voltage	20	V
Allowable power dissipation	Pd max	Our PCB, Soldered *	5.05	W
Package thermal resistance	θjc	Our PCB, Soldered *	2.1	°C/W
		Our PCB, Not soldered *	3.6	°C/W
Maximum junction temperature	Tj max		150	°C
Operating temperature	Topr		-25 to +75	°C
Storage temperature	Tstg		-50 to +150	°C

* : Mounted on a specified board 110.0mm × 100.0mm × 1.5mm, glass epoxy (two-layer)

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Range at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage range	VD	Supply voltage	9	15	18	V
Load impedance range	R_L	Speaker load	4	8		Ω

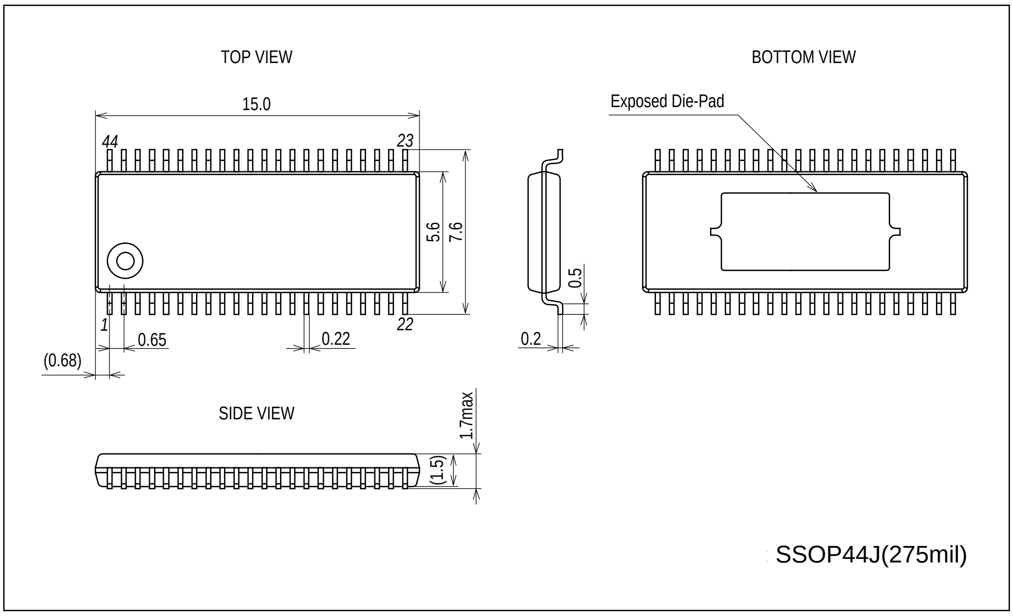
Electrical Characteristics at Ta = 25°C, VD = 15V, R_L = 8Ω, L = 33μH (TOKO : A7502BY-330M), C = 0.1μF, C_L = 0.47μF

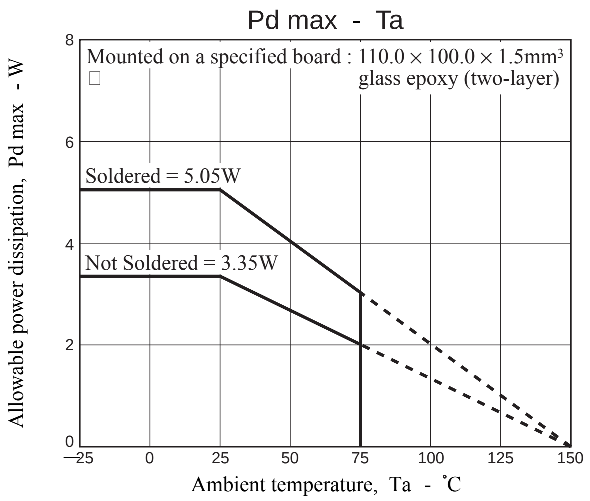
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Standby current	Ist	$\overline{\text{STBY}}$ = L, $\overline{\text{MUTE}}$ = L		1	10	μA
Mute current	Imute	$\overline{\text{STBY}}$ = H, $\overline{\text{MUTE}}$ = L	14	20	26	mA
Quiescent current	I_{CCO}	$\overline{\text{STBY}}$ = H, $\overline{\text{MUTE}}$ = H	35	45	55	mA
Voltage gain	VG	fin = 1kHz, V_O = 0dBm	28	30	32	dB
Offset voltage	Voffset	Rg = 0	-150		150	mV
Total harmonic distortion	THD+N	P_O = 1W, fin = 1kHz, AES17		0.08	0.4	%
Output power	P_O@10%	THD+N = 10%, AES17	13	15		W
Channel separation	CHsep.	Rg = 0, V_O = 0dBm, DIN AUDIO	55	70		dB
Ripple rejection ratio	SVRR	fr = 100Hz, Vr = 0dBm, Rg = 0, DIN AUDIO	50	60		dB
Noise	V_{NO}	Rg = 0, A-weight		90	300	μVrms
High-level input voltage	V_{IH}	$\overline{\text{STBY}}$ and $\overline{\text{MUTE}}$ pin	3		VD	V
Low-level input voltage	V_{IL}	$\overline{\text{STBY}}$ and $\overline{\text{MUTE}}$ pin	0		1	V
Under voltage protection UPPER	UV_UPPER	VD voltage measure		8.0		V
Under voltage protection LOWER	UV_LOWER	VD voltage measure		7.0		V

Note : The values of these characteristics were measured in the Our test environment. The actual values in an end system will vary depending on the printed circuit board pattern, the external components actually used, and other factors.

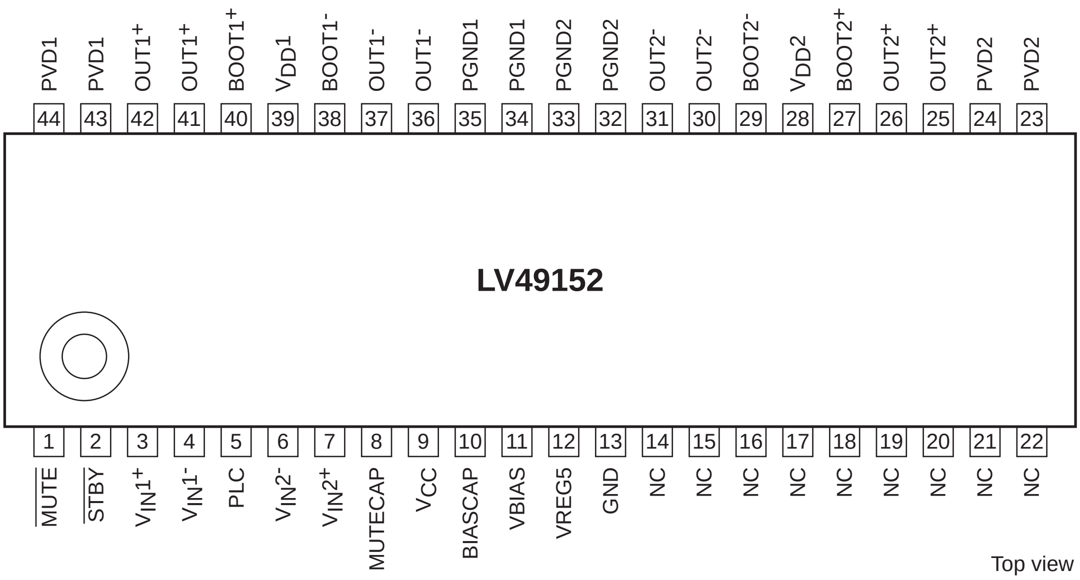
Package Dimensions

unit : mm (typ)
3285

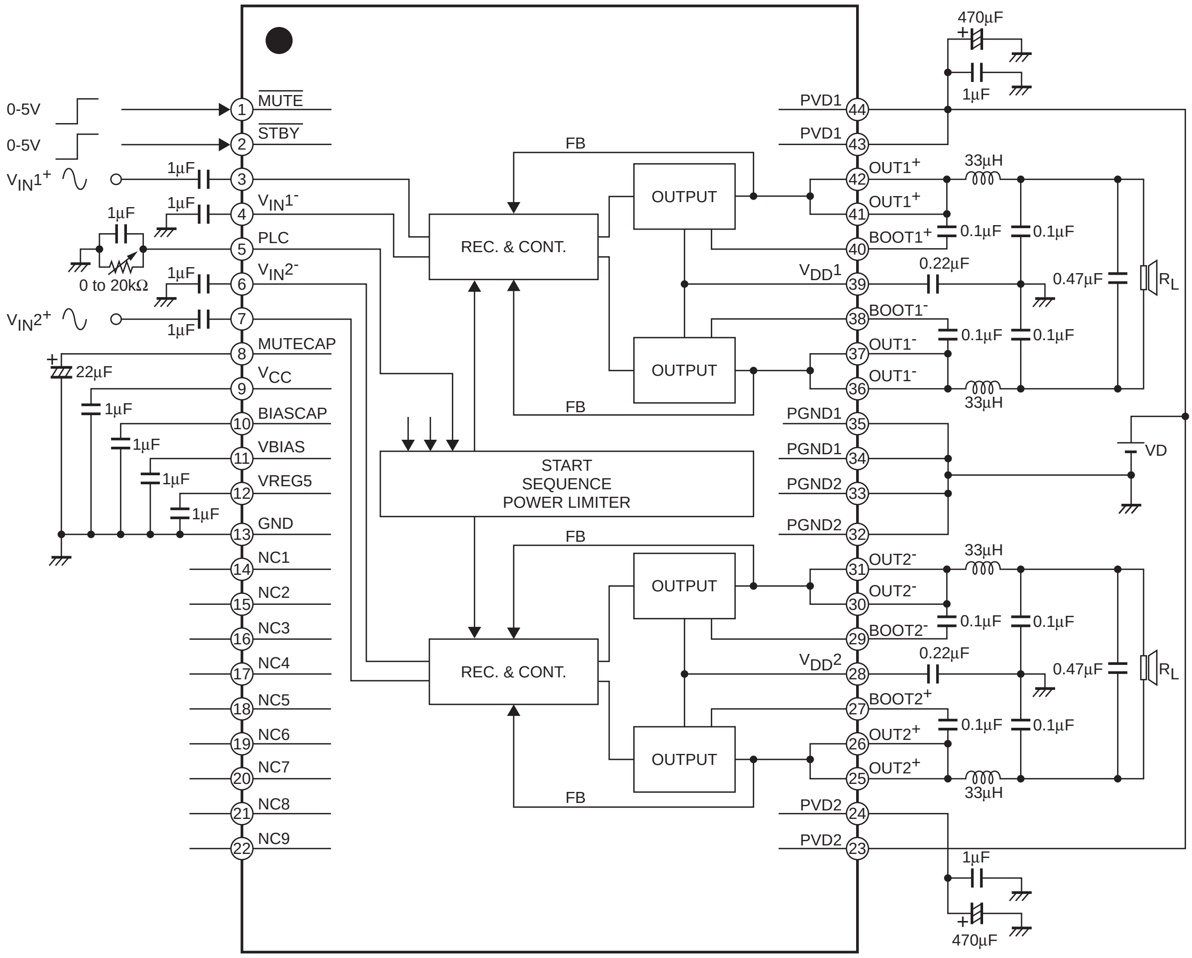




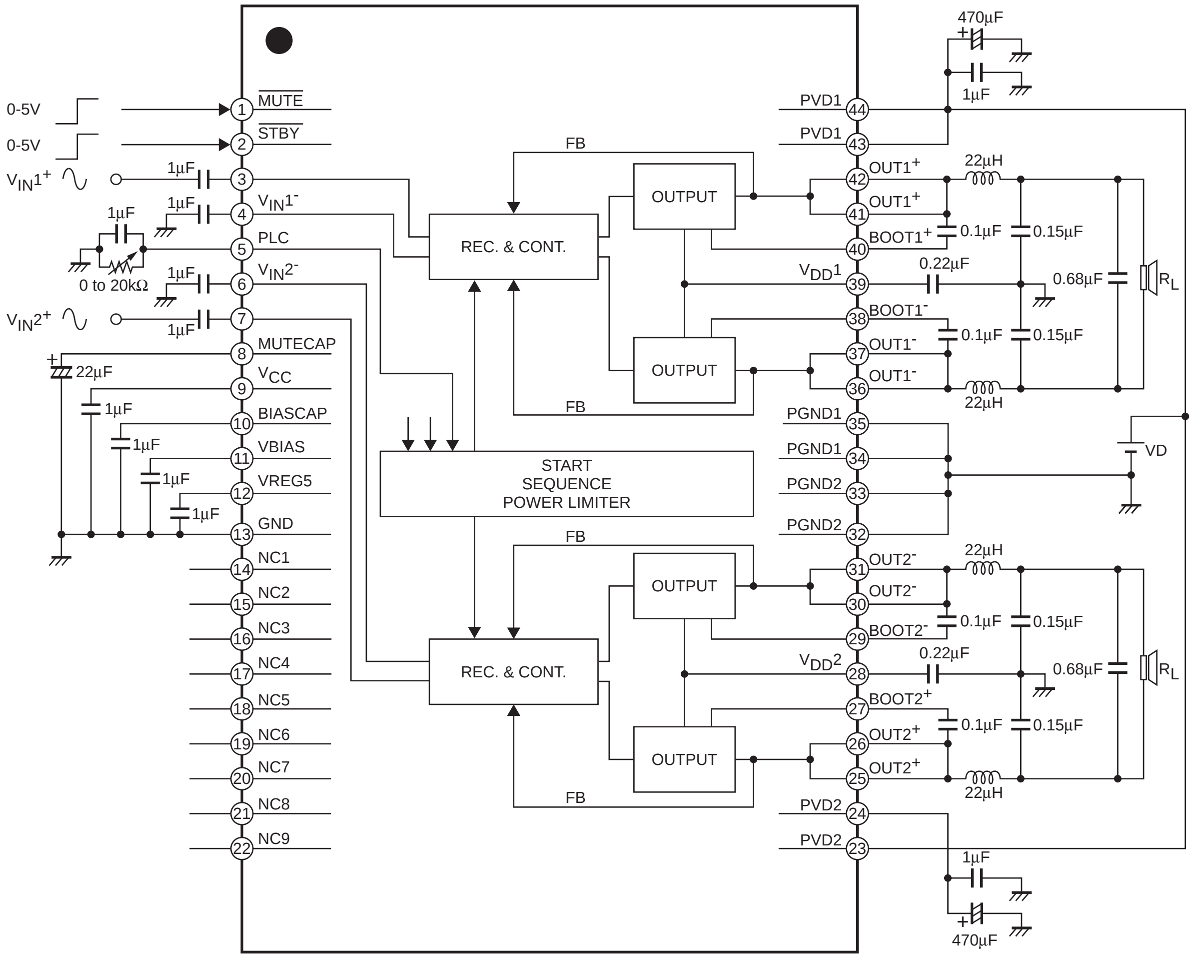
Pin Assignment



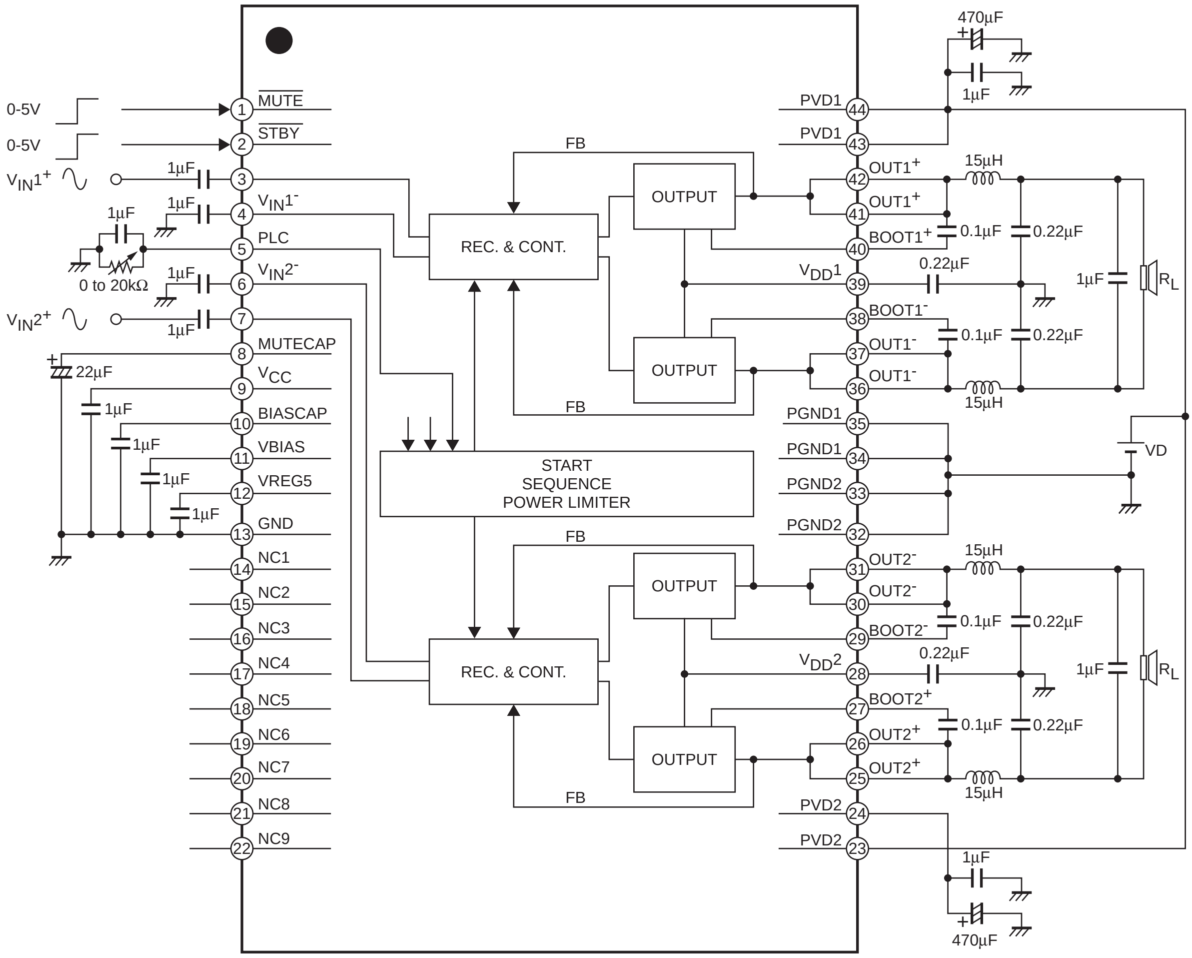
Block Diagram and Application Circuit Example 1 (R_L = 8Ω)



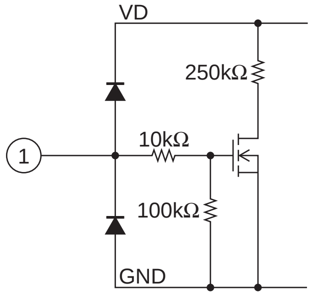
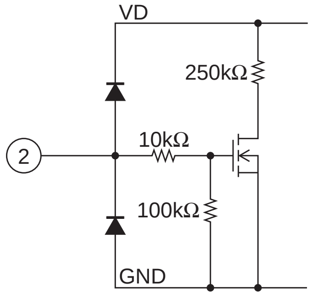
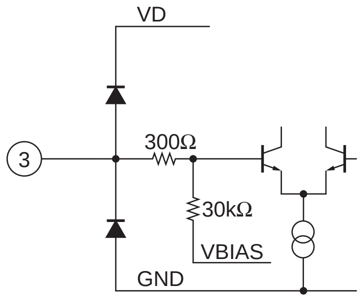
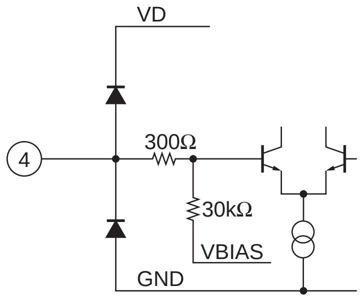
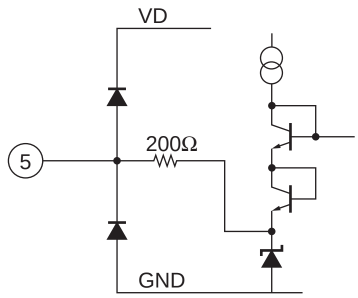
Application Circuit Example 2 (R_L = 6Ω)



Application Circuit Example 3 ($R_L = 4\Omega$)



Pin Equivalent Circuit

Pin No.	Pin name	I/O	Description	Equivalent Circuit
1	$\overline{\text{MUTE}}$	I	Mute control pin	
2	$\overline{\text{STBY}}$	I	Standby control pin	
3	$V_{IN}1^{+}$	I	Input pin, CH1 plus	
4	$V_{IN}1^{-}$	I	Input pin, CH1 minus	
5	PLC	I	Power level control pin	

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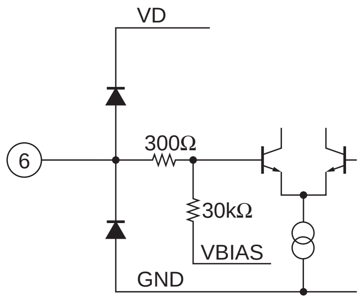
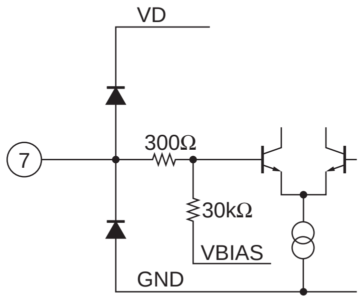
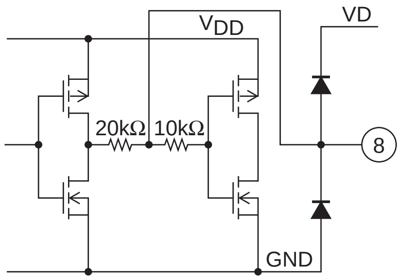
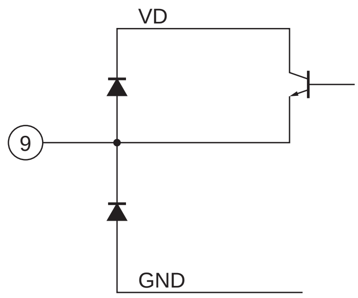
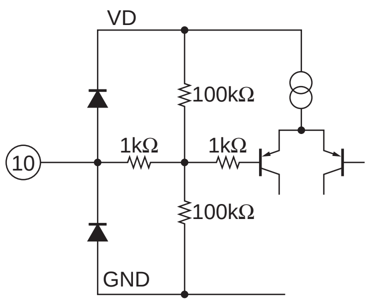
Pin No.	Pin name	I/O	Description	Equivalent Circuit
6	$V_{IN}2^-$	I	Input pin, CH2 minus	
7	$V_{IN}2^+$	I	Input pin, CH2 plus	
8	MUTECAP	O	Muteing sysytem capcitor connection	
9	V_{CC}	O	Internal power supply decupling capacitor connection	
10	BIASCAP	O	Internal regulator decupling capacitor connection	

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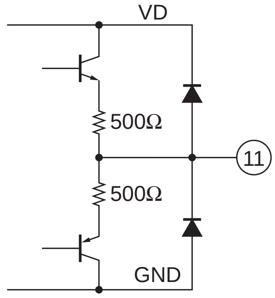
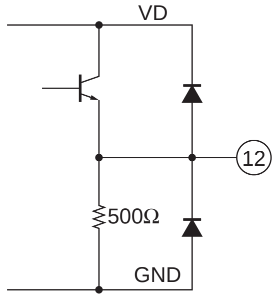
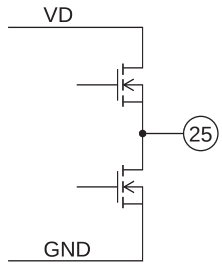
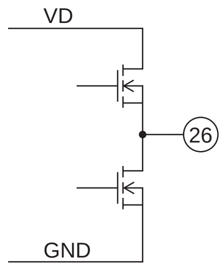
Pin No.	Pin name	I/O	Description	Equivalent Circuit
11	VBIAS	O	Internal regulator decupling capacitor connection	
12	VREG5	O	Internal regulator decupling capacitor connection	
13	GND		Analog Ground	
14	NC		Non connection	
15	NC		Non connection	
16	NC		Non connection	
17	NC		Non connection	
18	NC		Non connection	
19	NC		Non connection	
20	NC		Non connection	
21	NC		Non connection	
22	NC		Non connection	
23	PVD2		CH2 power supply	
24	PVD2		CH2 power supply	
25	OUT2+	O	Output pin, CH2 plus	
26	OUT2+	O	Output pin, CH2 plus	

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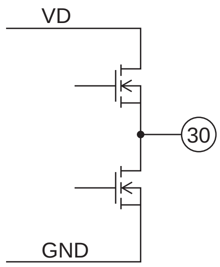
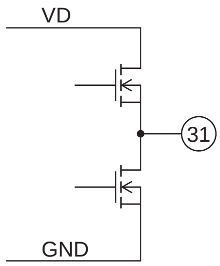
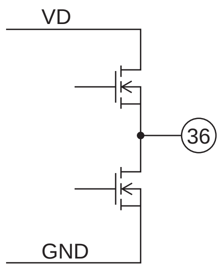
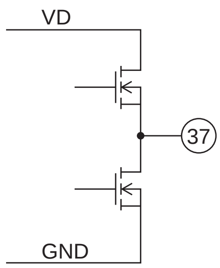
Pin No.	Pin name	I/O	Description	Equivalent Circuit
27	BOOT2^{+}	I/O	Boot strap pin, CH2 plus	
28	$V_{DD}2$	O	CH2 internal regulator decupling capacitor connection	
29	BOOT2^{-}	I/O	Boot strap pin, CH2 minus	
30	OUT2^{-}	O	Output pin, CH2 minus	
31	OUT2^{-}	O	Output pin, CH2 minus	
32	PGND2		CH2 Power Ground	
33	PGND2		CH2 Power Ground	
34	PGND1		CH1 Power Ground	
35	PGND1		CH1 Power Ground	
36	OUT1^{-}	O	Output pin, CH1 minus	
37	OUT1^{-}	O	Output pin, CH1 minus	
38	BOOT1^{-}	I/O	Boot strap pin, CH1 minus	
39	$V_{DD}1$	O	CH1 internal regulator decupling capacitor connection	
40	BOOT1^{+}	I/O	Boot strap pin, CH1 plus	

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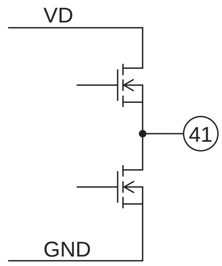
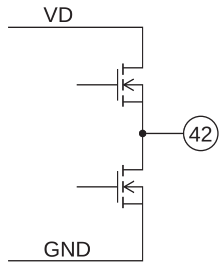
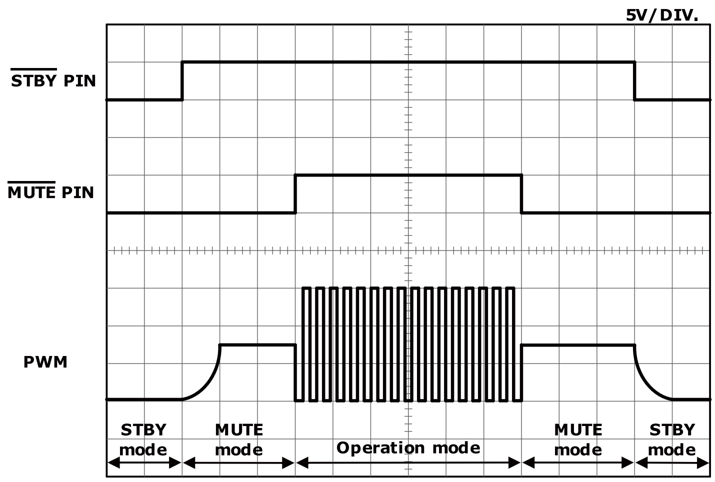
Pin No.	Pin name	I/O	Description	Equivalent Circuit
41	$OUT1^{+}$	O	Output pin, CH1 plus	
42	$OUT1^{+}$	O	Output pin, CH1 plus	
43	PVD1		CH1 power supply	
44	PVD1		CH1 power supply	

Operation Mode Summary

STBY mode ($\overline{\text{STBY}}$ = L and $\overline{\text{MUTE}}$ = L)
Each bias becomes off state when the regulator in IC has been turned off.
The most of circuits becomes off state.
The supply current : 1µA (typical).

MUTE mode ($\overline{\text{STBY}}$ = H and $\overline{\text{MUTE}}$ = L)
Each bias becomes on state when the regulator in IC has been turned on.
When more than half of the circuits are active, the amplifier in the output stages become off.
The supply current : 20mA (typical).

Operation mode ($\overline{\text{STBY}}$ = H and $\overline{\text{MUTE}}$ = H)
The LV49152V operates as D-class amplifier.
The output signal is synchronized with the input signal.
The supply current : 45mA (typical)

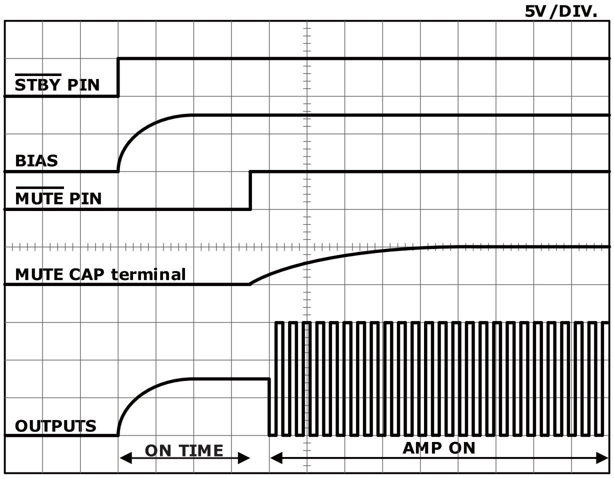


Function image

ON TIME/OFF TIME

ON TIME

Please secure ON TIME of 350msec or more for reducing Pop noise.

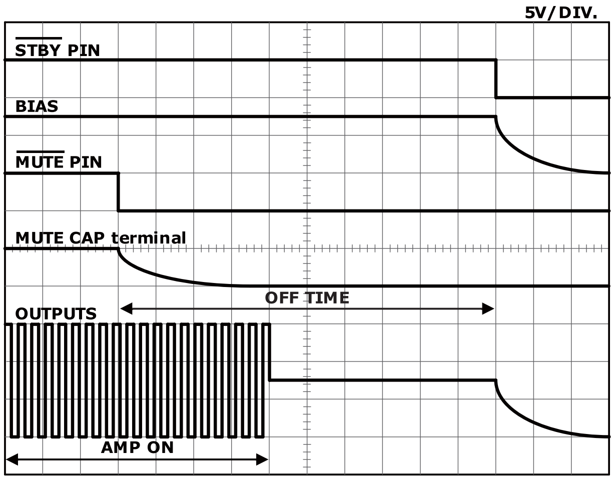


Function image

ON TIME • • • the time until the $\overline{\text{MUTE}}$ pin is set to high level after the $\overline{\text{STBY}}$ pin is set to high level

OFF TIME

Please secure OFF TIME of 1000msec or more for reducing Pop noise.



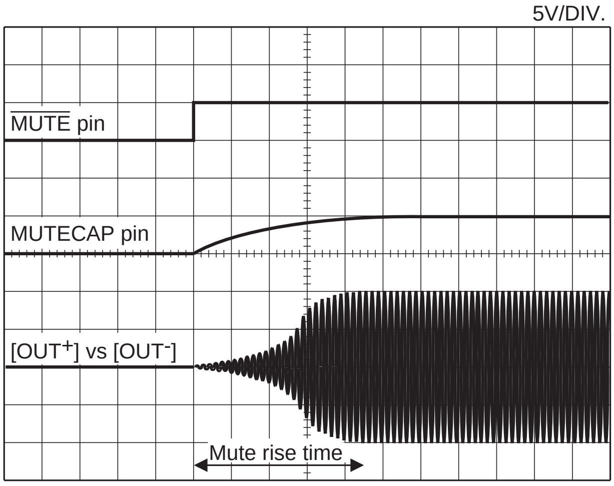
Function image

OFF TIME • • • the time until the $\overline{\text{STBY}}$ pin is set to low level after the $\overline{\text{MUTE}}$ pin is set to low level

SOFT MUTE

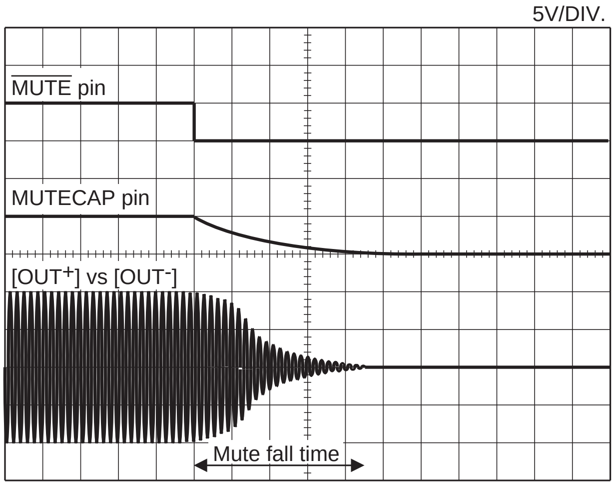
The soft mute circuit is able to use fade in/fade out function, and can set Rise time and fall time by the time constant of the MUTECAP capacitor.

FADE IN
Mute rise time is Applpx.450msec in our recommended external components.



Function image

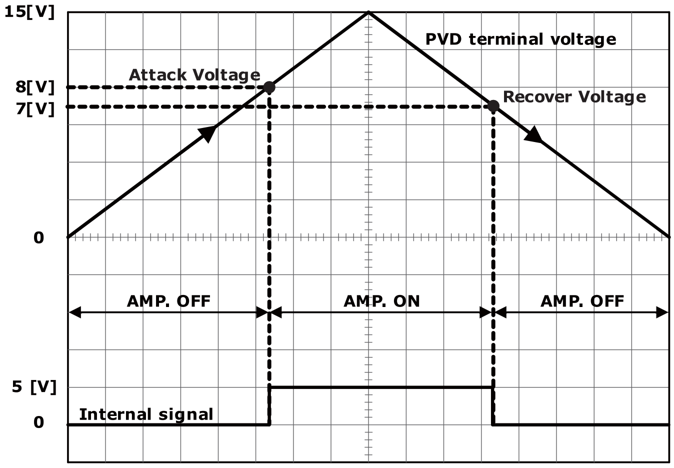
FADE OUT
Mute fall time is Applpx.450msec in our recommended external components.



Function image

Power supply lowering protection circuit

Since the instable operation in the low voltage is prevented by using this circuit, after the voltage of the PVD pin is monitored and the voltage below the Attack voltage (PVD = 8V typ.), AMP is turned off.
Also, to prevent the instable operation when the voltage of the PVD pin is decreased by any cause during operations, the Attack voltage (PVD = 7V typ.) is set.
The voltage of Attack and Recover has hysteresis (About 1V) to prevent ON/OFF continuous action of the power supply lowering protection circuit.

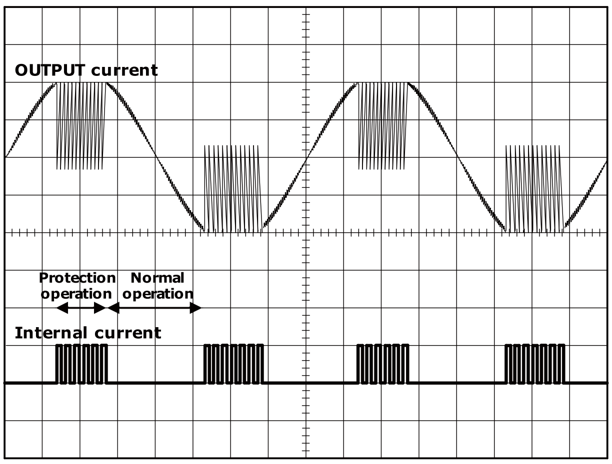


Function image

Also, this IC is designed to turn off AMP in the same sequence that the MUTE is on as a pop noise measures when the plug of products are put off.

Over current protection circuit

The over current protection circuit is a protection circuit * to protect the output DMOS from the over current and corresponds to any mode of the power supply, GND and a load short.
The protection operation is performed when the current reaches the detection current value set out in IC and the output DMOS is compulsorily turned off for about 20μsec.
After compulsorily tuning off the output DMOS, when the Amplifier is automatically reset in usual operation and the over current flows continuously, the protection operation is performed again.

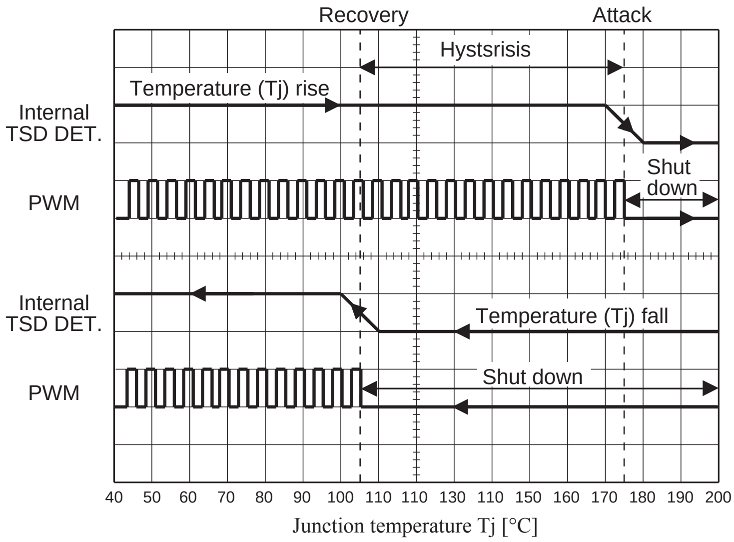


Function image

* The over current protection circuit is a function to avoid the abnormal state like the output short-circuit temporarily. Unfortunately, we cannot guarantee that IC is not destroyed.

Thermal protection circuit

The LV49152V includes a thermal protection circuit to prevent damage to or destruction of the IC should abnormal internal heat generation occur.
This means that should the IC junction temperature (Tj) rise above about 175°C due to inadequate heat dissipation or other reason, the thermal protection circuit will operate to stop IC operation should the temperature rise further.
If the temperature is reduced by lowering the input level or other means, the thermal protection circuit will recover automatically (about 105°C).



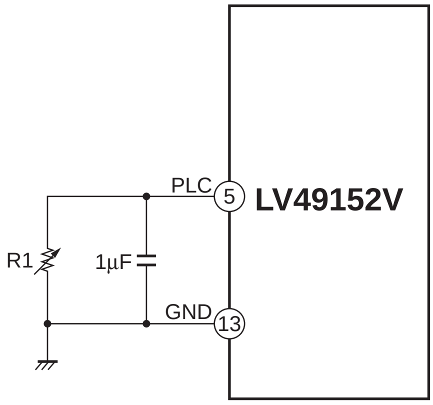
Function image

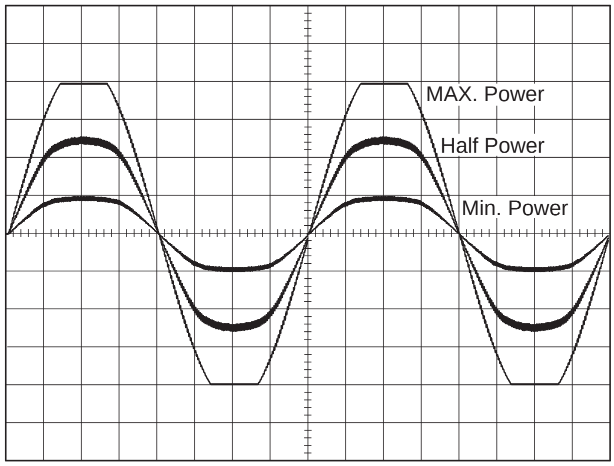
* The thermal protection circuit is a function to avoid the abnormal state temporarily.
  Unfortunately, we cannot guarantee that IC is not destroyed.

PLC

The PLC (power level control) function is able to control the maximum index modulation by setting a value of external PLC resistance R1 voluntarily, and prevent a PWM signal from becoming the over modulation mode. In addition, this circuit can be use as output power limit circuit because the PLC function can set the maximum index modulation voluntarily, and variable from 2W to 15W with output power linearly in the state that made the power supply voltage and load resistance fixation. Because the PLC function can set the suitable rated output with the same power supply voltage/speaker regardless of screen size in flat screen televisions by this, set can plan the commonization of the board.

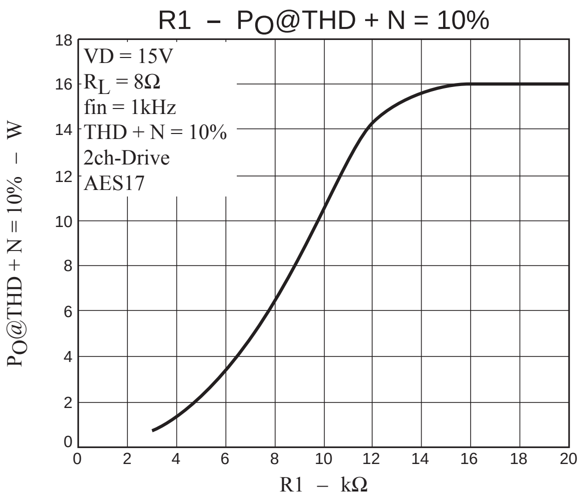
Furthermore, The PLC function can reduce abnormal noise in the hard clip so that output wave pattern becomes the soft clip when it limited output power.





Function image

Measuring condition
VD = 15V, R_L = 8Ω, L = 33μH (TOKO : A7502BY-330M), C = 0.1uF,C_L = 0.47μF,Ta = 25°C

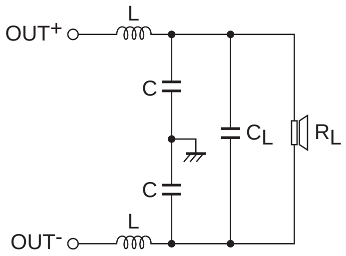


R1 [kΩ]	Po@10% [W]
3.0	0.694
3.6	1.073
4.7	1.982
6.2	3.642
7.5	5.562
8.2	6.855
9.1	8.591
10	10.64
13	15.32
15	15.94
20	16.01

Setting example of the output power limit value

* When it is used this function as output power limit, please use the high-precision resistance such as the metal film resistor when precision of the electricity value is necessary.
* The value of external PLC resistance R1 please connects more than 3kΩ.
* When it is changed a value of external PLC resistance R1, please turn off an amplifier.

Cut-off frequency calculation method and the output LC filter setting



The cut off frequency fc of the output LC filter is calculated by the following formula.

$$fc = \frac{1}{2\pi\sqrt{2LC_L}}$$

Also, by setting the cut off frequency fc, the value of C_L and L is calculated by using the following formula.

$$C_L = \frac{1}{2\sqrt{2} \times \pi\ R_L fc}$$

$$L = \frac{\sqrt{2} \times R_L}{4\pi\ fc}$$

In general, the value from 20% to 30% of C_L is set to C.

In case of fc = 30kHz

R_L [Ω]	L [μH]	C_L [μF]	C [μF]	Q
4	15	1	0.22	0.650
6	22	0.68	0.15	0.636
8	33	0.47	0.1	0.704
16	68	0.22	0.047	0.739

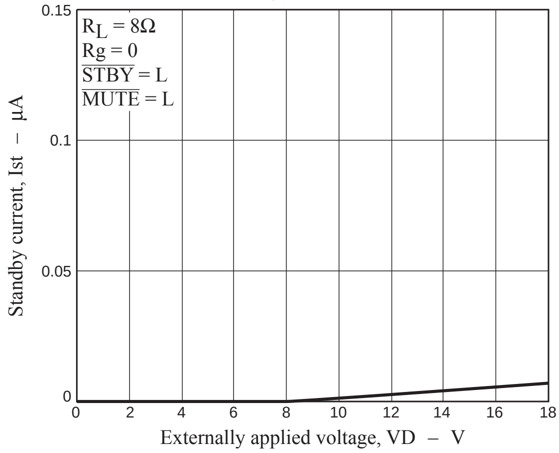
Above formula is common calculation method and is a measure of constant setting.
In fact, it is necessary to set with each set that considers the speaker characteristics.

In addition, please set the fixed number to become Q ≤ 1 in currents in the fc neighborhood increasing if Q value of the LC filter is big.

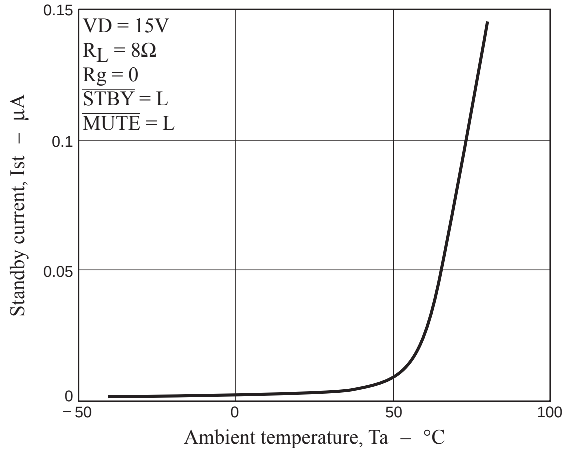
Glaph deta

L = 33µH (TOKO : A7502BY-330M), C = 0.1µF, C_L = 0.47µF

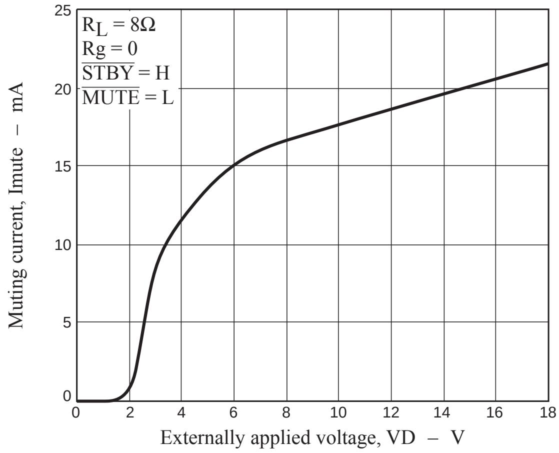
Ist – VD



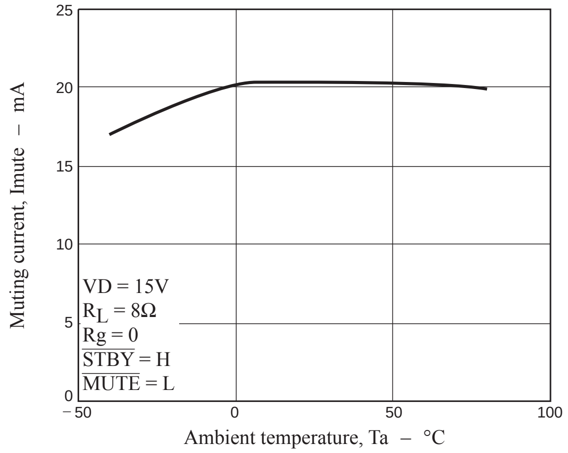
Ist – Ta



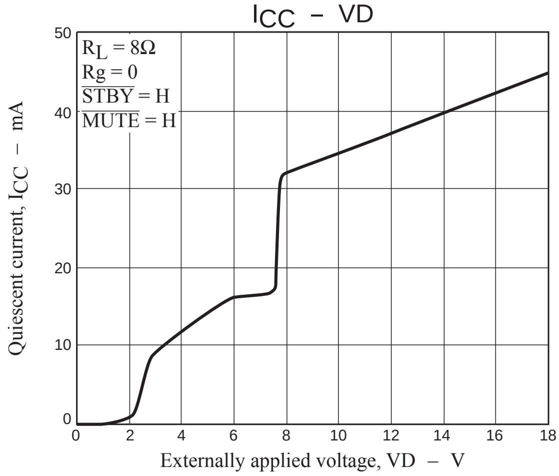
Imute – VD



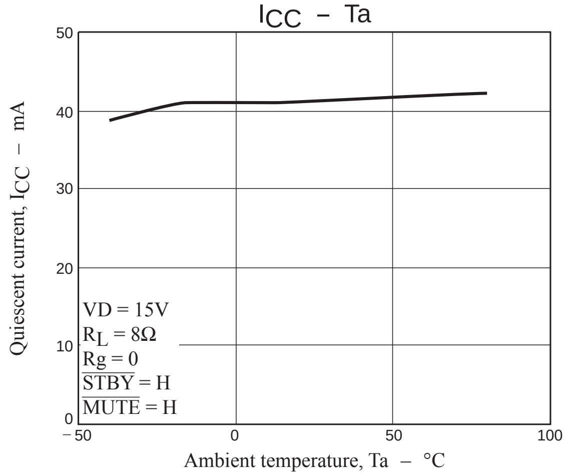
Imute – Ta



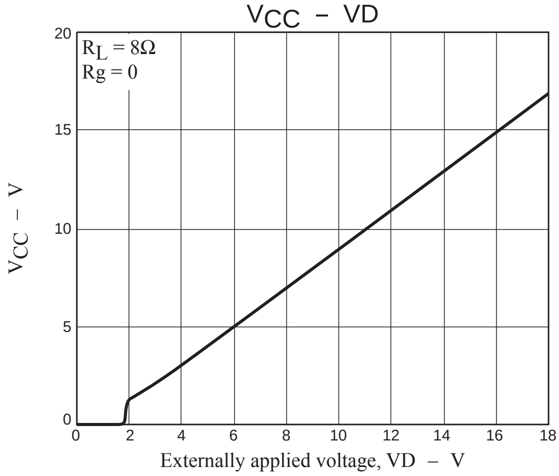
I_{CC} – VD



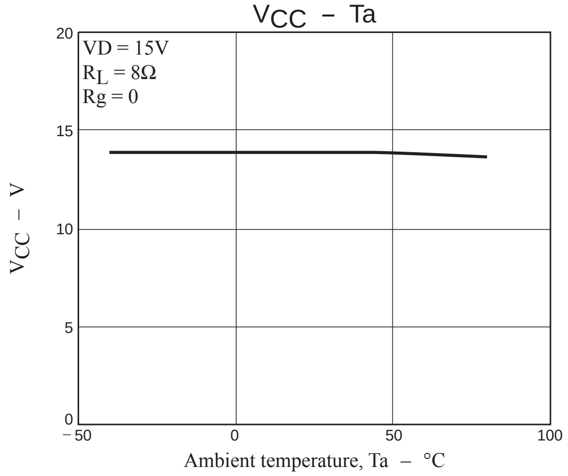
I_{CC} – Ta



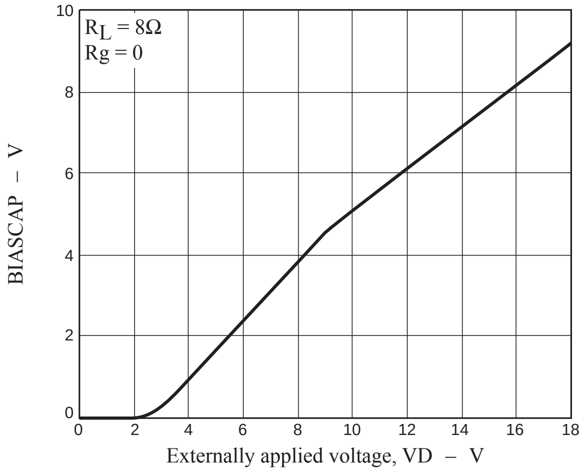
V_{CC} – VD



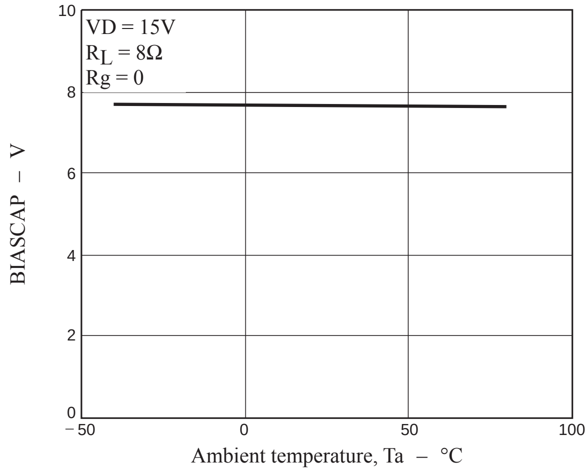
V_{CC} – Ta



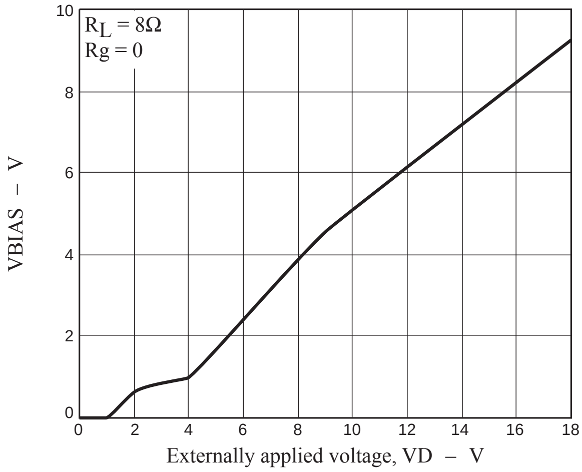
BIASCAP – VD



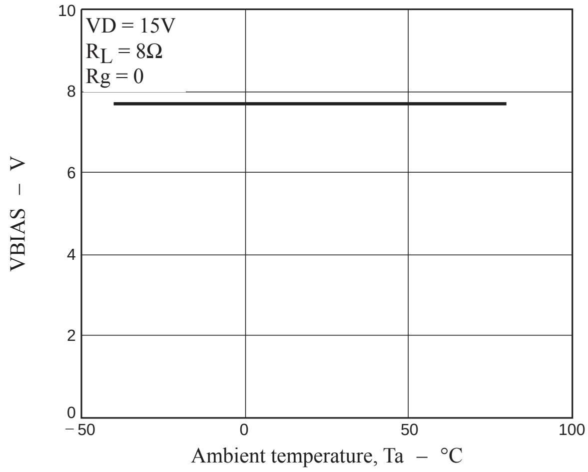
BIASCAP – Ta



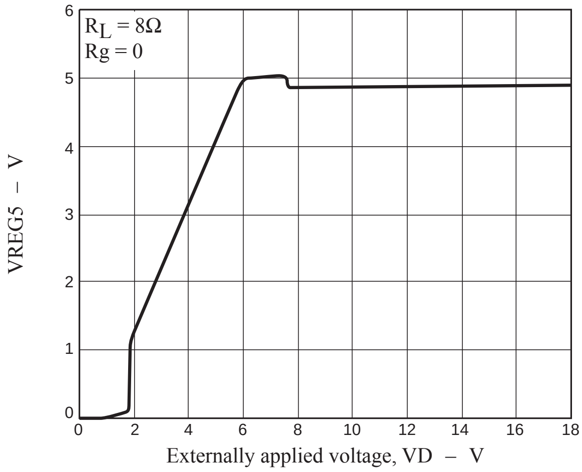
VBIAS – VD



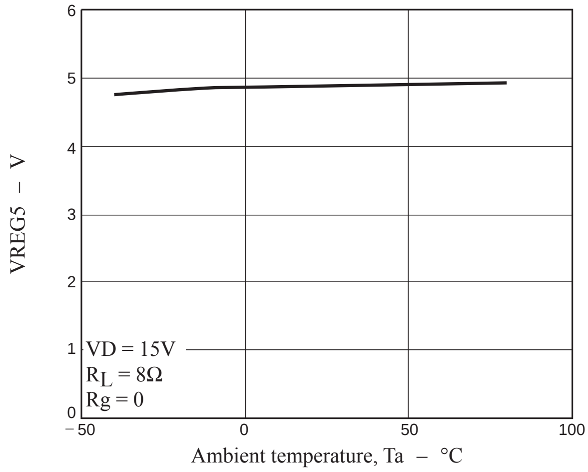
VBIAS – Ta



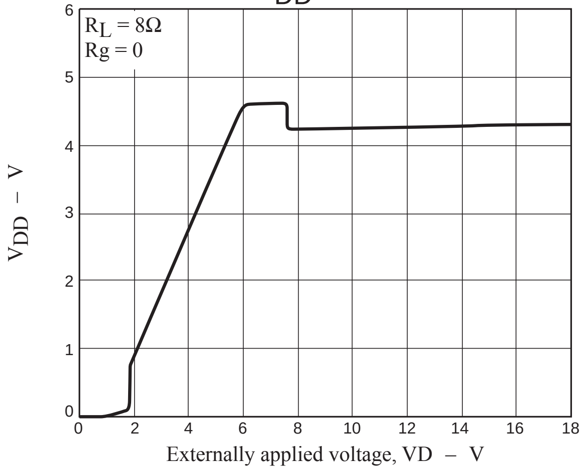
VREG5 – VD



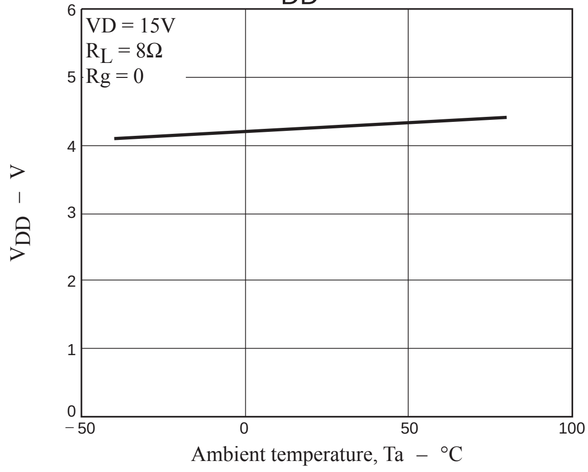
VREG5 – Ta



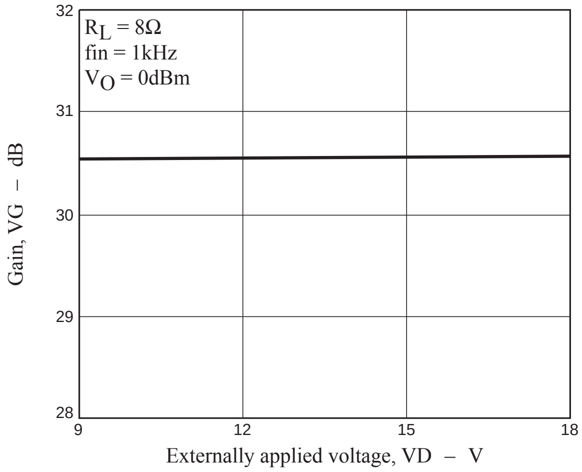
V_{DD} – VD



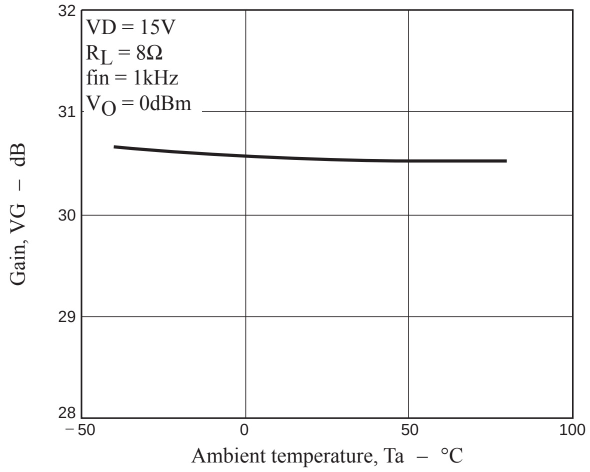
V_{DD} – Ta



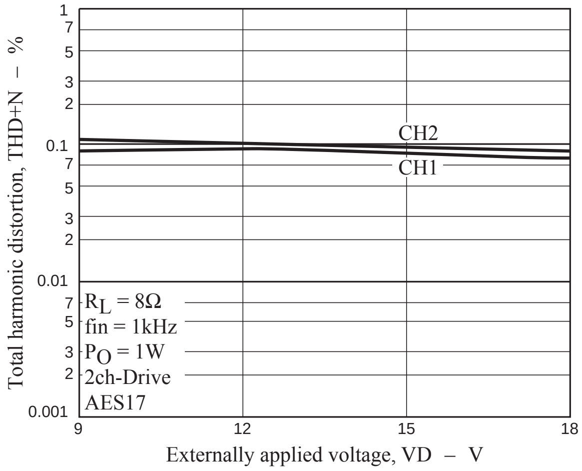
VG – VD



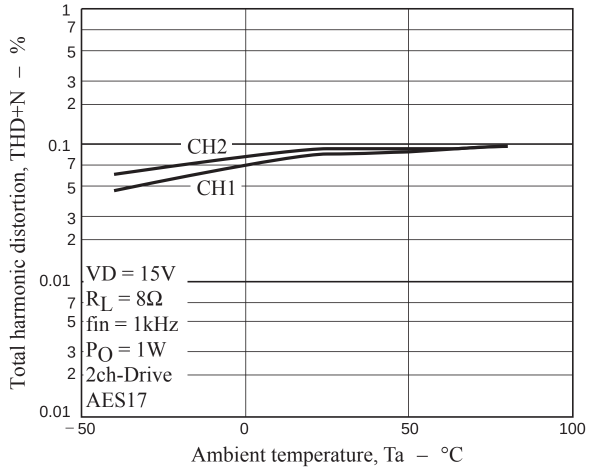
VG – Ta



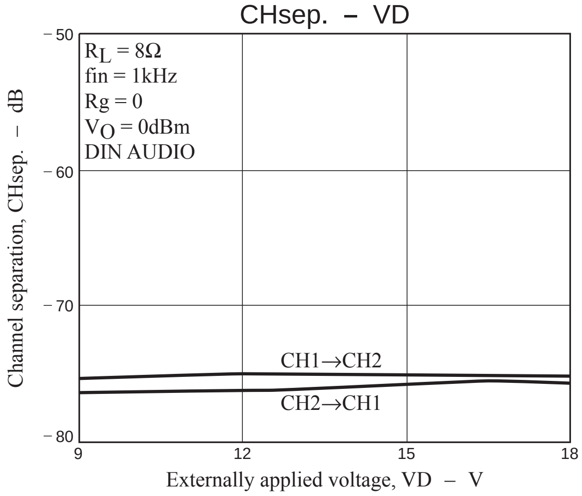
THD+N – VD



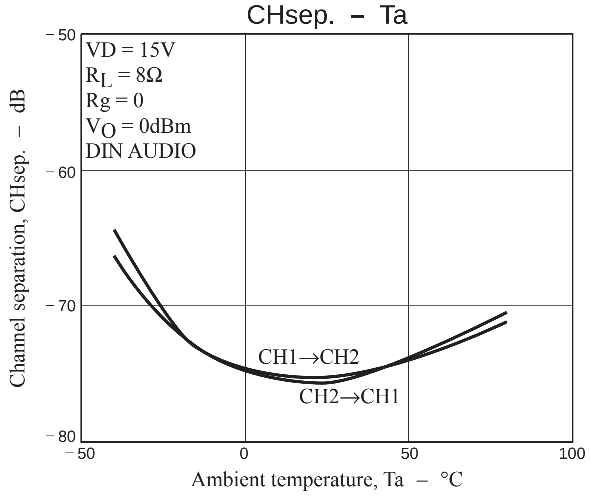
THD+N – Ta



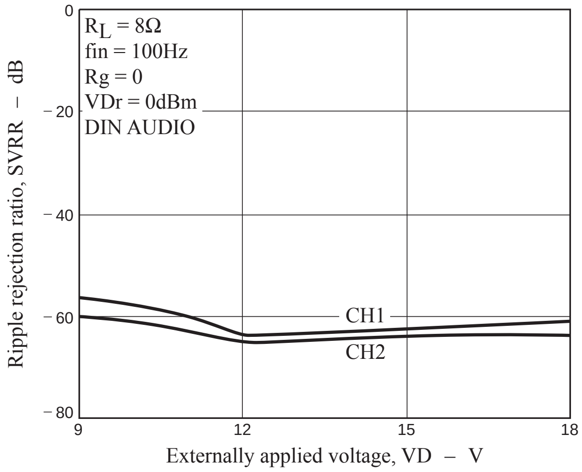
CHsep. – VD



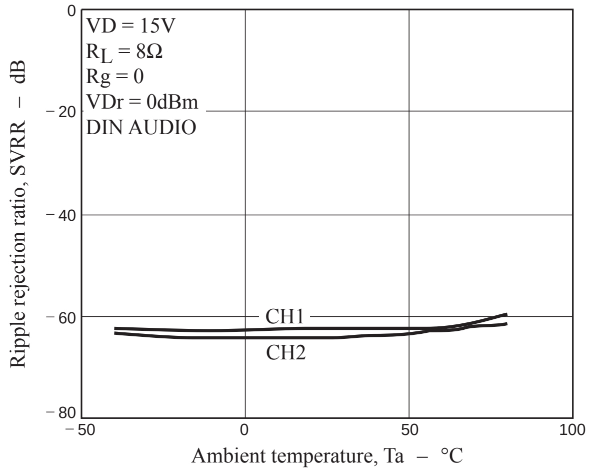
CHsep. – Ta

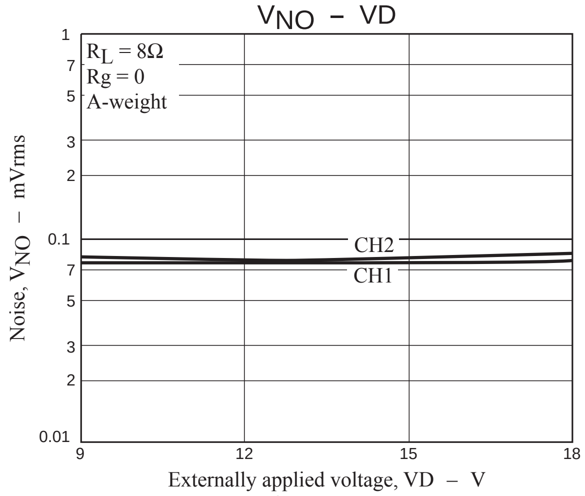


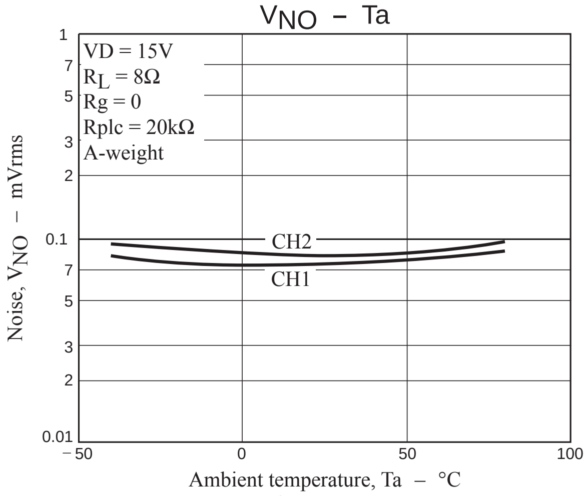
SVRR – VD

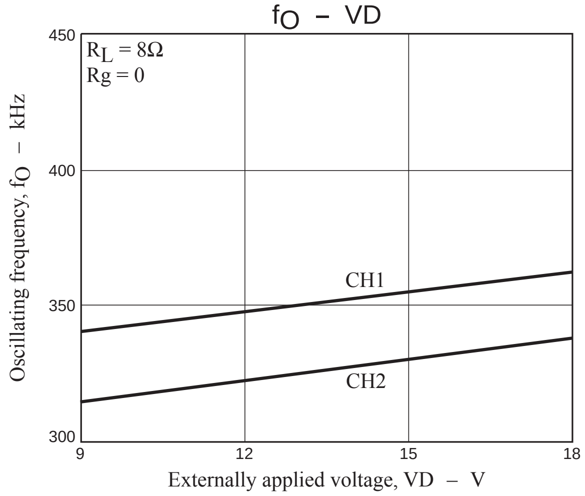


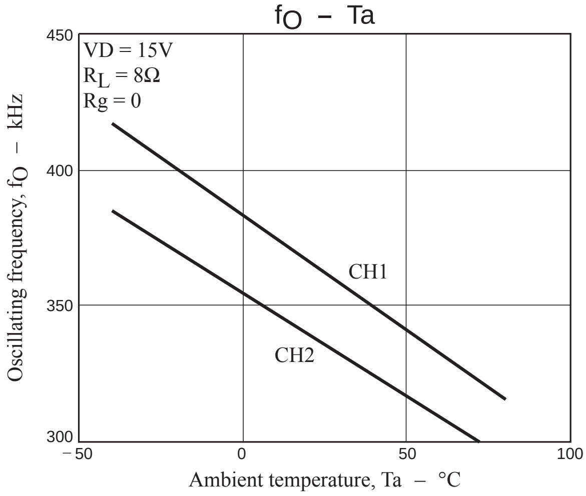
SVRR – Ta

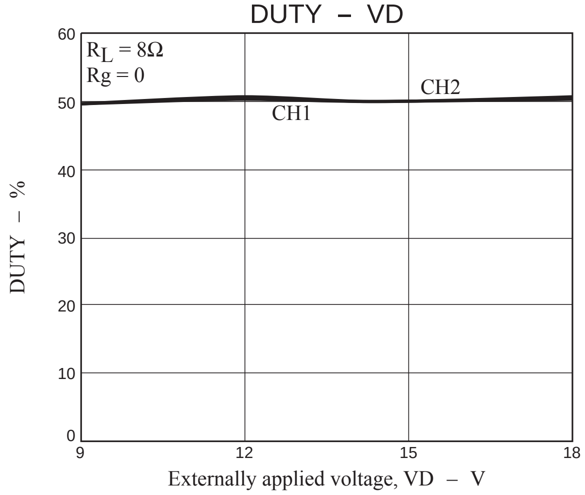


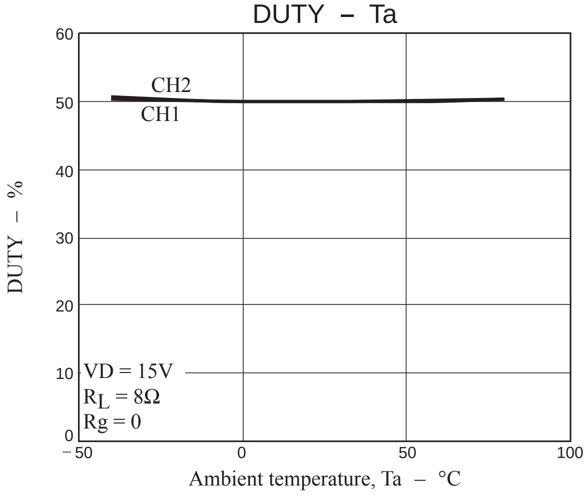

VNO – VD
RL = 8Ω
Rg = 0
A-weight
CH2
CH1
Noise, VNO – mVrms
Externally applied voltage, VD – V

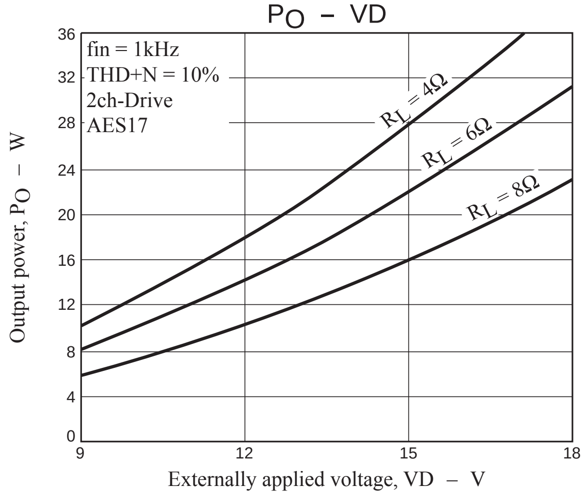

VNO – Ta
VD = 15V
RL = 8Ω
Rg = 0
Rplc = 20kΩ
A-weight
CH2
CH1
Noise, VNO – mVrms
Ambient temperature, Ta – °C

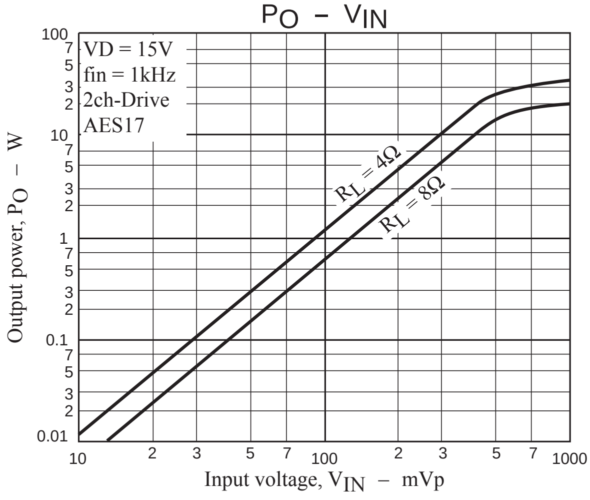

fO – VD
RL = 8Ω
Rg = 0
CH1
CH2
Oscillating frequency, fO – kHz
Externally applied voltage, VD – V


fO – Ta
VD = 15V
RL = 8Ω
Rg = 0
CH1
CH2
Oscillating frequency, fO – kHz
Ambient temperature, Ta – °C

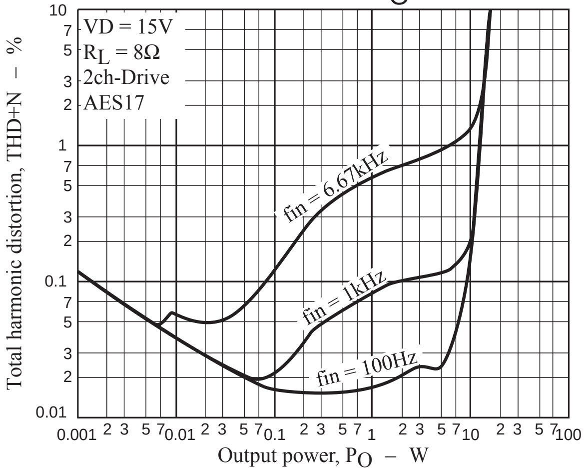

DUTY – VD
RL = 8Ω
Rg = 0
CH2
CH1
DUTY – %
Externally applied voltage, VD – V


DUTY – Ta
CH2
CH1
VD = 15V
RL = 8Ω
Rg = 0
DUTY – %
Ambient temperature, Ta – °C

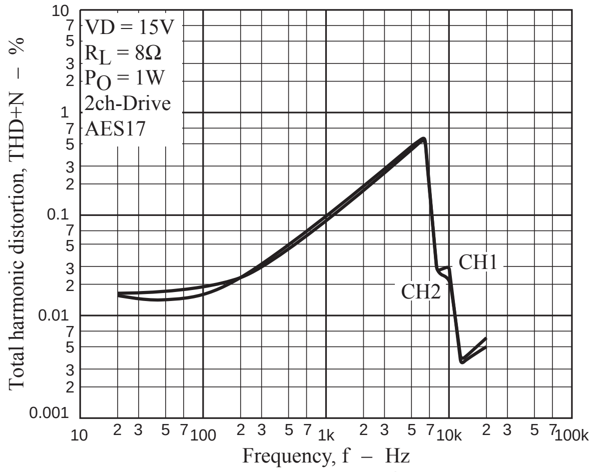

PO – VD
fin = 1kHz
THD+N = 10%
2ch-Drive
AES17
RL = 4Ω
RL = 6Ω
RL = 8Ω
Output power, PO – W
Externally applied voltage, VD – V


PO – VIN
VD = 15V
fin = 1kHz
2ch-Drive
AES17
RL = 4Ω
RL = 8Ω
Output power, PO – W
Input voltage, VIN – mVp

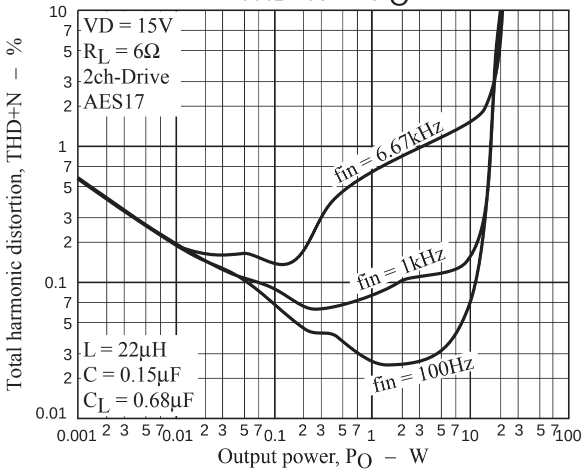
THD+N – P_O



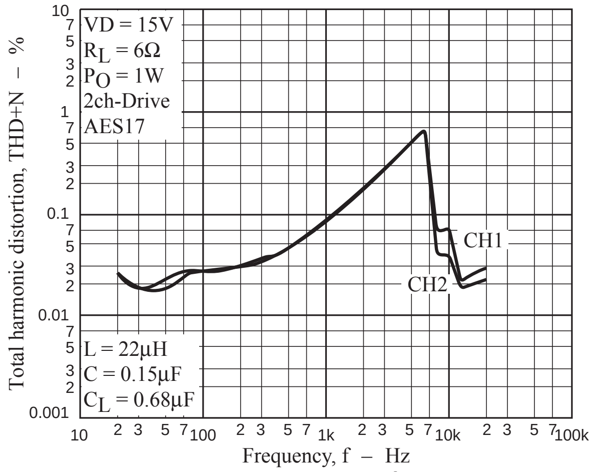
THD+N – f



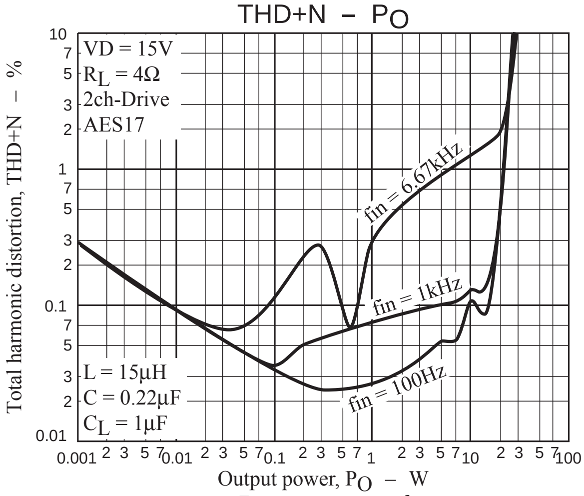
THD+N – P_O



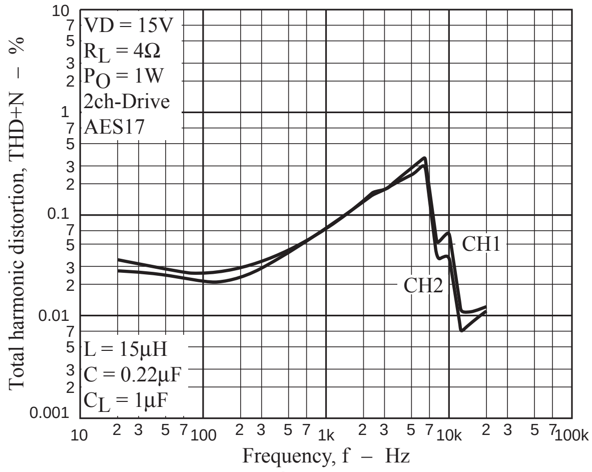
THD+N – f



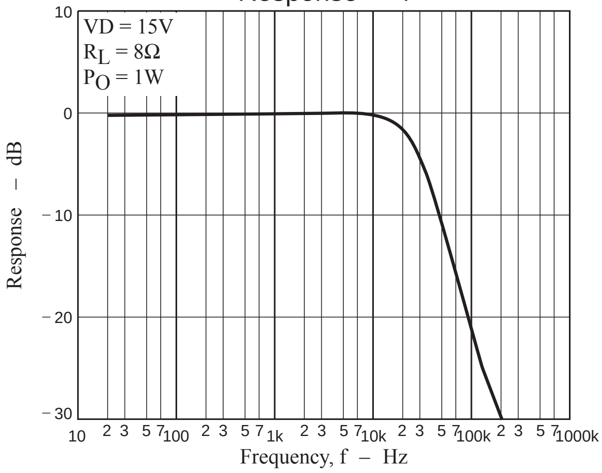
THD+N – P_O



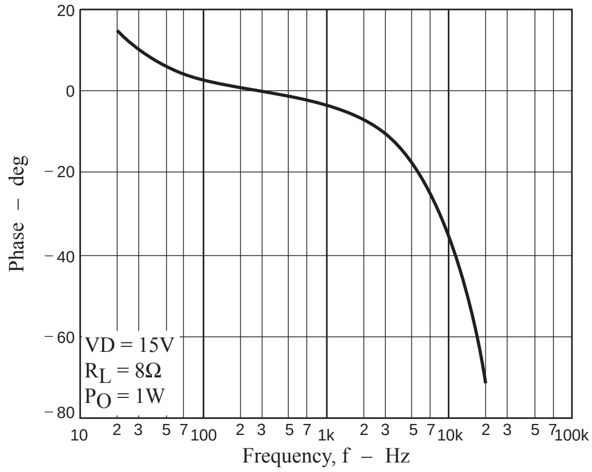
THD+N – f

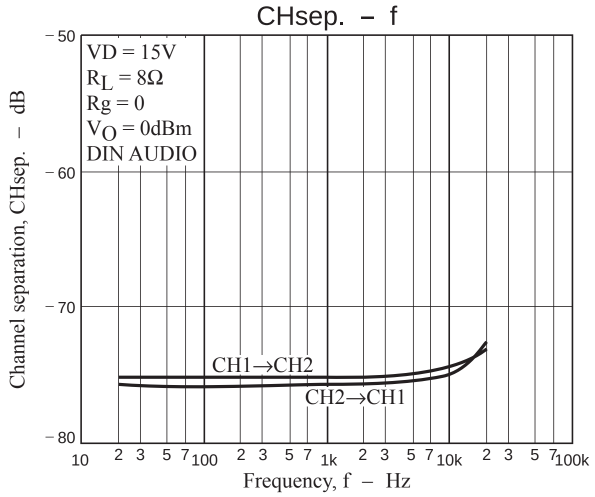


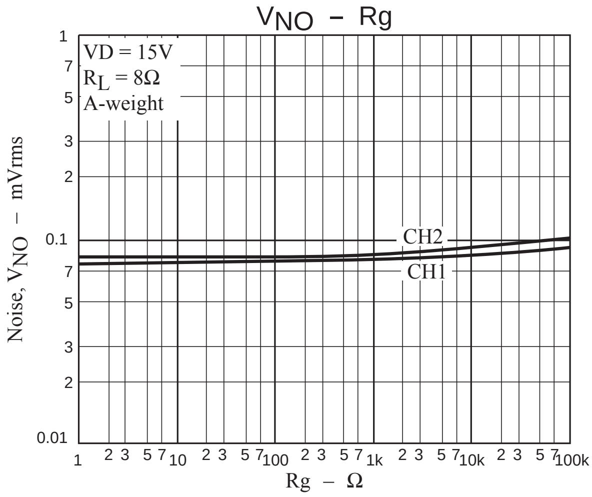
Response – f

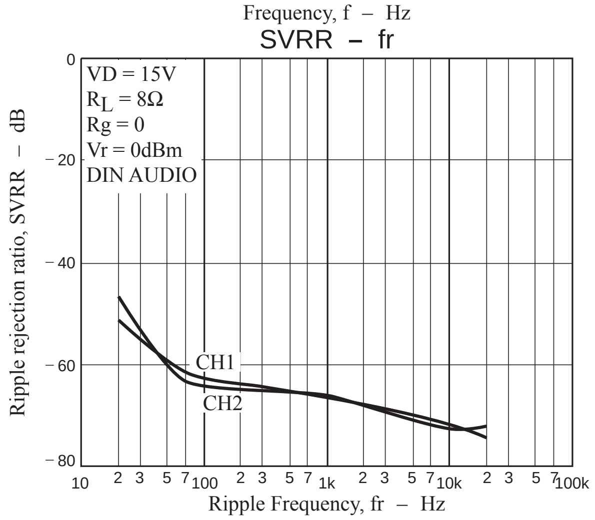


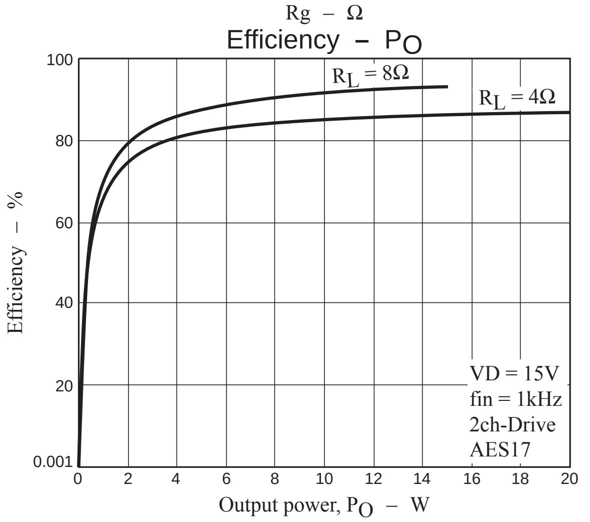
Phase – f




CHsep. – f
VD = 15V
RL = 8Ω
Rg = 0
VO = 0dBm
DIN AUDIO
CH1→CH2
CH2→CH1
Channel separation, CHsep. – dB
Frequency, f – Hz


VNO – Rg
VD = 15V
RL = 8Ω
A-weight
CH2
CH1
Noise, VNO – mVrms
Rg – Ω


SVRR – fr
VD = 15V
RL = 8Ω
Rg = 0
Vr = 0dBm
DIN AUDIO
CH1
CH2
Ripple rejection ratio, SVRR – dB
Ripple Frequency, fr – Hz


Efficiency – PO
RL = 8Ω
RL = 4Ω
VD = 15V
fin = 1kHz
2ch-Drive
AES17
Efficiency – %
Output power, PO – W