International
IOR Rectifier

Data Sheet No. PD60170-G

IR2137/IR2237(J)(Q)

3-PHASE BRIDGE DRIVER

Features

- Floating channel up to +600V or +1200V
- "soft" over-current shutdown turns off all six outputs
- Integrated high side desaturation circuit
- Controlled "soft" turn on for EMI reduction
- Integrated brake IGBT driver
- Three independent low side COM pins
- Separate pull-up/pull-down output drive pins
- Matched delay outputs
- 3.3V logic compatible
- Under voltage lockout with hysteresis band

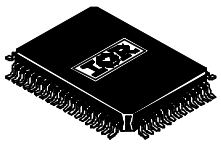
Description

The IR2137/IR2237(J)(Q) are a high voltage, high speed 3-phase IGBT driver best suited for AC motor drive applications. Integrated desaturation logic provides ground fault protection as well as other mode of over current protection. Soft shutdown is initiated in the event of any overcurrent/ground fault conditions, and all six outputs are simultaneously turned off. Output drivers have separate turn on/off pins to facilitate independent gate drive impedance with EMI soft turn on. Optimum matched delays between phases, and between high/low side enables small deadtime, thus improving low speed performance. The brake driver eliminates additional circuits.

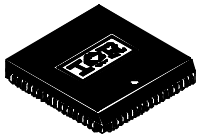
Product Summary

V_{OFFSET}	600V max. or 1200V max.
I_O+/-	220mA / 460mA
V_{OUT}	12.5V - 20V
Brake Io+/-	40mA/80mA
Matched delay	75nsec
Deadtime (typ.)	300 nsec
DESAT Blanking time (typ.)	2.0usec
DESAT input voltage threshold (typ.)	Vt+ = 5.0V

Packages

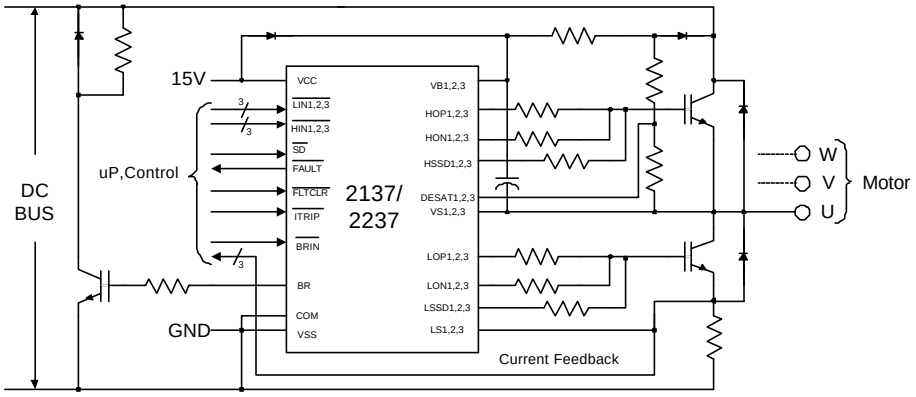


64-Lead MQFP



68-Lead PLCC

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
$V_{S1,2,3}$	High side offset voltage	$V_{B1,2,3}$ -25	$V_{B1,2,3}$ +0.3	V
$V_{B1,2,3}$	High side floating supply voltage (IR2137)	-0.3	625	
	(IR2237)	-0.3	1225	
V_{HO}	High side floating output voltage (HOP, HON, HSSD)	$V_{S1,2,3}$ - 0.3	$V_{B1,2,3}$ + 0.3	
V_{CC}	Low side and logic fixed supply voltage	-0.3	25	
V_{SS}	Logic ground	V_{CC} - 25	V_{CC} + 0.3	
$V_{LO1,2,3}$	Low side output voltage (LOP, LON, LSSD)	$V_{LS1,2,3}$ -0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage ($\overline{HIN}$, $\overline{LIN}$,$\overline{SD}$, $\overline{ITRIP}$, $\overline{FLTCLR}$, $\overline{BRIN}$)	V_{SS} - 0.3	(V_{SS} + 15) or (V_{CC} + 0.3) which ever is lower	
V_{FLT}	FAULT output voltage	V_{SS} - 0.3	V_{CC} + 0.3	
V_{DESAT}	DESAT input voltage	$V_{S1,2,3}$ - 0.3	$V_{B1,2,3}$ + 0.3	
V_{BR}	BRAKE output voltage	- 0.3	V_{CC} + 0.3	
$V_{LS1,2,3}$	Low side output return voltage	V_{CC} - 25	V_{CC} + 0.3	
dV/dt	Allowable offset supply voltage slew rate	—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$ (MQFP64)	—	2.0	W
	(PLCC68)		3.0	
Rth_{JA}	Thermal resistance, junction to ambient (MQFP64)	—	60	°C/W
	(PLCC68)	—	40	
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High side floating supply voltage	$V_{S1,2,3}$ + 13	$V_{S1,2,3}$ + 20	V
$V_{S1,2,3}$	High side floating supply offset voltage (IR2137)	Note 1	600	
	(IR2237)	Note 1	1200	
$V_{HO1,2,3}$	High side output voltage (HOP, HON, HSSD)	$V_{S1,2,3}$	$V_{S1,2,3}$ + 20	
$V_{LO1,2,3}$	Low side output voltage (LOP, LON, LSSD)	$V_{LS1,2,3}$	V_{CC}	
V_{CC}	Low side and logic fixed supply voltage	12.5	20	
V_{SS}	Logic ground	-5	+5	
V_{IN}	Logic input voltage ($\overline{HIN}$, $\overline{LIN}$,$\overline{SD}$, $\overline{ITRIP}$, $\overline{FLTCLR}$, $\overline{BRIN}$)	V_{SS}	V_{SS} + 5	
V_{BR}	BRAKE output voltage	0	V_{CC}	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_{FLT}	FAULT output voltage	V_{SS}	V_{CC}	V
$V_{LS1,2,3}$	Low side output return voltage	-5.0	+5.0	
V_{DESAT}	DESAT pin input voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of COM -5 to COM +600V/+1200V. Logic state held for V_S of COM -5V to -COM V_{BS}.
Note 2: All input pins are internally clamped with a 5.2V zener diode.

Static Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS}1,2,3$) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to all six channels (HOP/HON1,2,3 and LOP/LON1,2,3). The V_O and I_O parameters are referenced to $V_{LS}1,2,3$ and $V_S1,2,3$ and are applicable to the respective output leads: $H_{O1,2,3}$ and $L_{O1,2,3}$. V_{DESAT} and I_{DESAT} parameters are referenced to $V_{S1,2,3}$

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	10.3	11.4	12.5	V	
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	9.5	10.4	11.3		
V_{CCUVH}	V_{CC} supply undervoltage lockout hysteresis	—	1.0	—		
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	10.3	11.4	12.5		
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	9.5	10.4	11.3		
V_{BSUVH}	V_{BS} supply undervoltage lockout hysteresis	—	1.0	—		
I_{LK}	Offset supply leakage current (IR2137)	—	—	50	µA	$V_{B1,2,3} = V_{S1,2,3}$ = 600V
	(IR2237)	—	—	50		$V_{B1,2,3} = V_{S1,2,3}$ = 1200V
I_{QBS}	Quiescent V_{BS} supply current	—	120	200		
I_{QCC}	Quiescent V_{CC} supply current	—	2	6	V	V_{CC} = 12.5 to 20V
V_{IH}	Logic "0" input voltage (OUT=LO) ($\overline{HIN}$,$\overline{LIN}$,$\overline{ITRIP}$,$\overline{SD}$,$\overline{BRIN}$,$\overline{FLTCLR}$)	3.15	—	—		
V_{IL}	Logic "1" input voltage (OUT=HI) ($\overline{HIN}$,$\overline{LIN}$,$\overline{ITRIP}$,$\overline{SD}$,$\overline{BRIN}$,$\overline{FLTCLR}$)	—	—	0.8		
V_{t+}	Logic input positive going threshold ($\overline{HIN}$,$\overline{LIN}$,$\overline{ITRIP}$,$\overline{SD}$,$\overline{BRIN}$,$\overline{FLTCLR}$)	1.6	2.5	3.1		
V_{t-}	Logic input negative going threshold ($\overline{HIN}$,$\overline{LIN}$,$\overline{ITRIP}$,$\overline{SD}$,$\overline{BRIN}$,$\overline{FLTCLR}$)	0.9	1.5	2.4		
V_T	Logic input hysteresis ($\overline{HIN}$,$\overline{LIN}$,$\overline{ITRIP}$,$\overline{SD}$,$\overline{BRIN}$,$\overline{FLTCLR}$)	0.7	1.0	—		

Static Electrical Characteristics - cont.

V_{BIAS} (V_{CC}, V_{BS}1,2,3) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to all six channels (HOP/HON1,2,3 and LOP/LON1,2,3). The V_O and I_O parameters are referenced to V_{LS}1,2,3 and V_S1,2,3 and are applicable to the respective output leads: $H_{O1,2,3}$ and $L_{O1,2,3}$. V_{DESAT} and I_{DESAT} parameters are referenced to $V_{S1,2,3}$

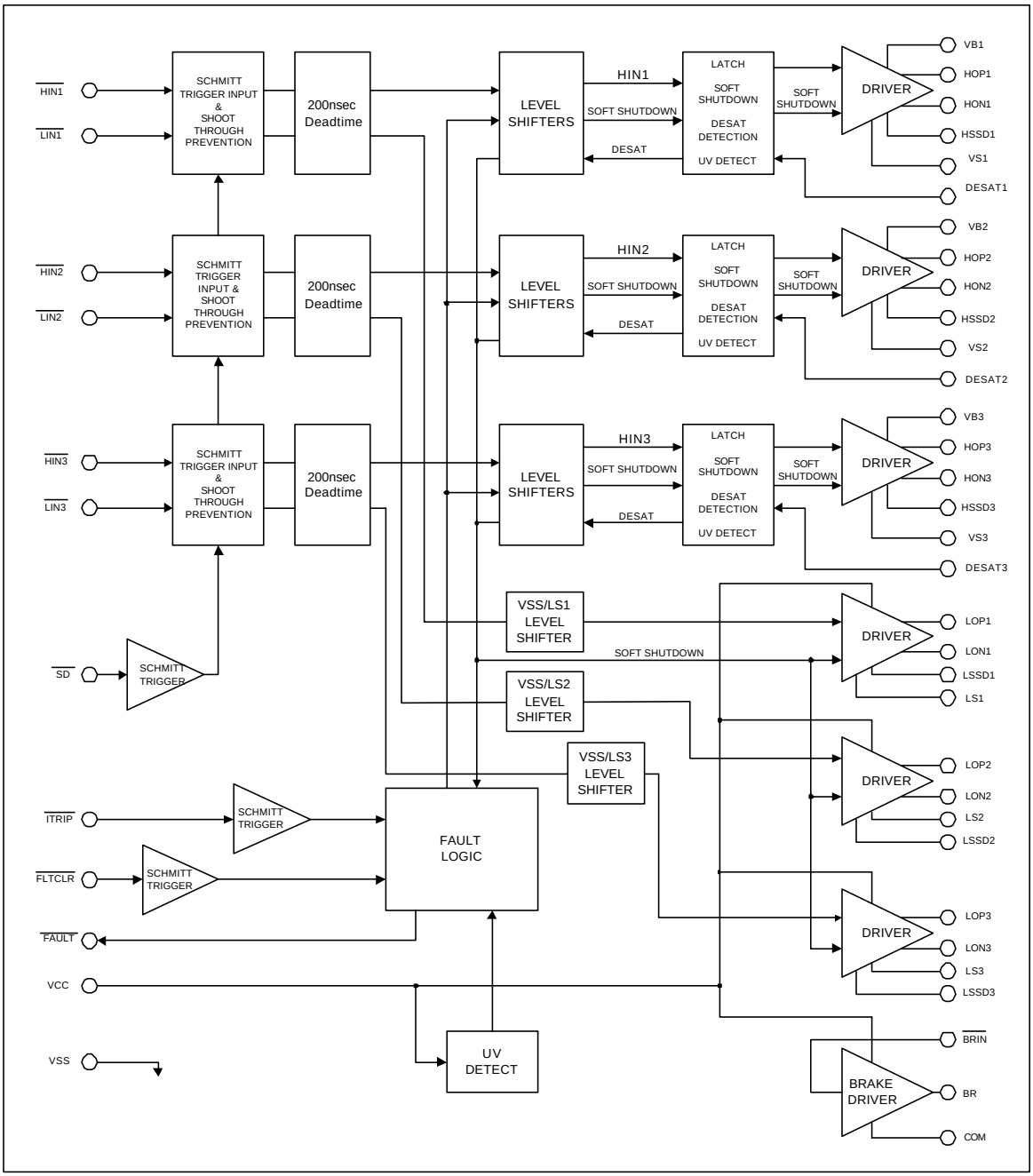
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{OH}	High level output voltage, V_{BIAS} - V_O (normal switching) HOP, LOP	—	—	100	mV	I_O = 1 mA
V_{OL}	Low level output voltage, V_O (normal switching) HON, LON	—	—	100		
I_{IN+}	Logic “1” input bias current	—	150	—	µA	V_{IN} = 0V
I_{IN-}	Logic “0” input bias current	—	80	—		V_{IN} = 5V
I_{DESAT+}	“high” DESAT input bias current	—	—	15		V_{DESAT} = 15V
I_{DESAT-}	“low” DESAT input bias current	—	—	.1		V_{DESAT} = 0V
I_{O+}	Output high short circuit pulsed current	220	300	—	mA	V_O = 0V, V_{IN} = 0V PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	460	550	—		V_O = 15V, V_{IN} = 5V PW ≤ 10 µs
I_{OBR+}	BR output high short circuit pulsed current	40	75	—		V_{BR}=0V, V_{BRIN}=0V PW ≤ 10 µs
I_{OBR-}	BR output low short circuit pulsed current	80	120	—		V_{BR}=15V,V_{BRIN}=5V PW ≤ 10 µs
V_{OHB}	BR high level output voltage, V_{BIAS}-V_{BR}	—	—	300	mV	I_{BR} = 1mA
V_{OLB}	BR low level output voltage, V_{BR}	—	—	150		
$R_{ON,SS}$	Soft shutdown on resistance	—	500	—	Ω	ITRIP = 0V
$R_{ON,FLT}$	FAULT low on resistance	—	60	—		
V_{DESAT+}	High DESAT input threshold voltage	—	5.2	—	V	

AC Electrical Characteristics

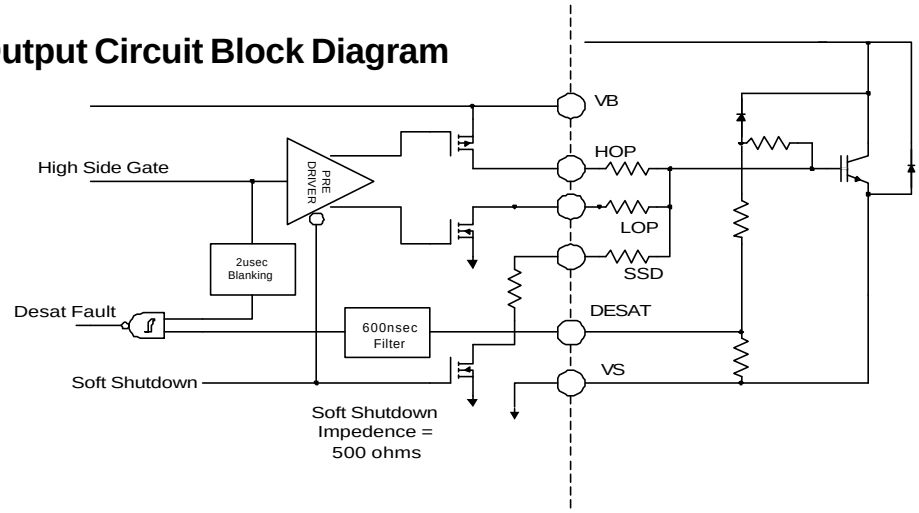
V_{BIAS} (V_{CC}, V_{BS}) = 15V, $V_{S1,2,3}$ = V_{SS}, T_A = 25°C and C_L = 1000 pF unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Propagation Delay Characteristics						
t_{on}	Turn-on propagation delay	150	400	600	ns	V_{IN} = 0 & 5V $V_{S1,2,3}$ = 0 to 600V or 1200V HOP=HON,LOP=LON Figure 4
t_{off}	Turn-off propagation delay	150	400	600		
t_r	Turn-on rise time	—	115	—		
t_f	Turn-off fall time	—	25	—		
t_{ITRIP}	ITRIP to output shutdown propagation delay	—	1000	1400		V_{IN},V_{DESAT}=0 V_{SD} = 5V
t_{SD}	SD to output shutdown propagation delay	—	1200	1500		V_{IN},V_{DESAT} = 0 V_{ITRIP} = 5V, fig. 7
t_{DESAT1}	DESAT to output shutdown propagation delay at HOPx turn-on	1400	2800	4200		$V_{S1,2,3}$ = 0 to 600V or 1200V V_{HIN} = 0V, V_{SD}, V_{ITRIP} = 5V, V_{DESAT} = 15V, fig. 5
t_{DESAT2}	DESAT to output shutdown propagation delay after blanking	600	1150	1700		
$t_{FLT, IT}$	ITRIP to FAULT output delay	—	800	1100		V_{IN},V_{ITRIP} =0V, V_{SD} = 5V, V_{DESAT}= 0V, fig. 7
t_{FLTCLR}	FLTCLR to FAULT output delay	—	1100	1400		V_{SD} = 5V, V_{DESAT} = 0V, fig. 7
$t_{FLT,DESAT1}$	DESAT to FAULT output delay propagation delay at HOPx turn-on	—	2500	—		$V_{S1,2,3}$ = 0 to 600V or 1200V V_{IN} = 0V, V_{SD}, V_{ITRIP} = 5V, V_{DESAT} = 15V, Figure 5
$t_{FLT,DESAT2}$	DESAT to FAULT output delay propagation delay after blanking	—	850	—		
t_{BL}	DESAT blanking time at turn-on	—	2000	—		
t_{onBR}	BR output turn-on propagation delay	—	120	200		Figure 4
t_{offBR}	BR output turn-off propagation delay	—	85	150		
t_{rBR}	BR output turn-on rise time	—	300	—		
t_{fBR}	BR output turn-off fall time	—	150	—		
Deadtime/Delay Matching Characteristics						
DT	Deadtime	—	300	—	ns	Figure 6
MDT	Matching delay, max (t_{on},t_{off}) - min (t_{on},t_{off}), (ton,toff are applicable to all six channels)	—	0	75		External dead time >400nsec
PM	Output pulse width matching, IPWin - PWoutl (exclude BRIN/BR)	—	0	75		External dead time >400nsec, Fig. 4

Functional Block Diagram



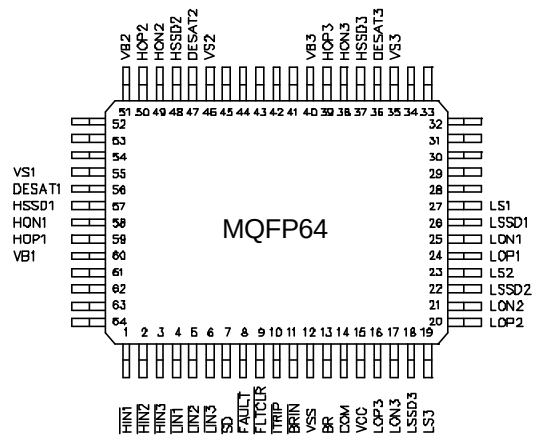
Driver Output Circuit Block Diagram



Lead Definitions

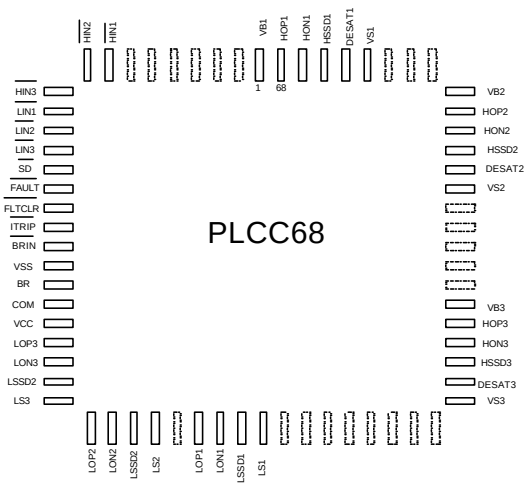
Symbol	Description
V_{CC}	Low side and logic supply voltage
VSS	Logic Ground
$\overline{HIN1,2,3}$	Logic inputs for high side gate driver outputs (HOP1,2,3/HON1,2,3, out of phase)
$\overline{LIN1,2,3}$	Logic inputs for low side gate driver outputs (LOP1,2,3/LON1,2,3, out of phase)
$\overline{SD}$	Logic input for shutdown (hard shutdown, level sensitive signal, negative logic)
$\overline{ITRIP}$	Logic input for overcurrent shutdown (soft shutdown, edge sensitive, negative signal)
$\overline{FLTCLR}$	Logic input for FAULT clear (edge sensitive, negative signal)
$\overline{BRIN}$	Logic input for brake driver, out of phase with BR
$\overline{FAULT}$	Fault output indicates over current and desaturation shutdown (open drain)
BR	Brake driver output
COM	Brake driver return
V_B1,2,3	High side gate drive floating supply
HOP1,2,3	High side driver pull up output
HON1,2,3	High side driver pull down output
HSSD1,2,3	High side soft shutdown output
DESAT1,2,3	IGBT desaturation protection input
$V_{S1,2,3}$	High voltage floating supply return
LOP1,2,3	Low side driver pull up output
LON1,2,3	Low side driver pull down output
LSSD1,2,3	Low side soft shutdown output
LS1,2,3	Low side driver returns

Lead Assignments



64 Lead MQFP

IR2137Q/ IR2237Q



68 Lead PLCC

IR2137J/IR2237J

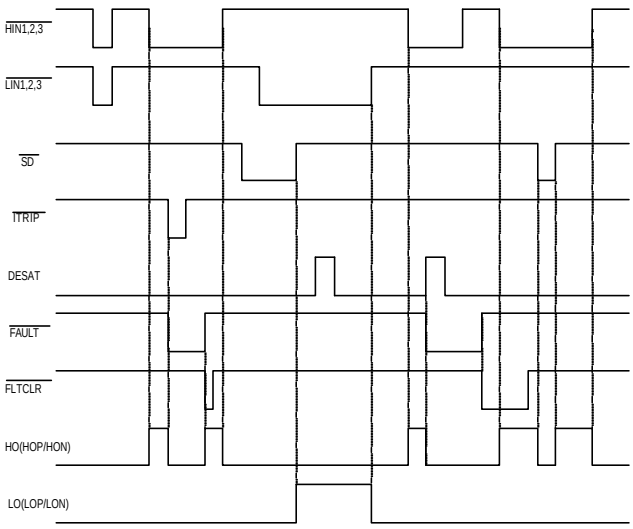


Figure 3. Timing Diagram

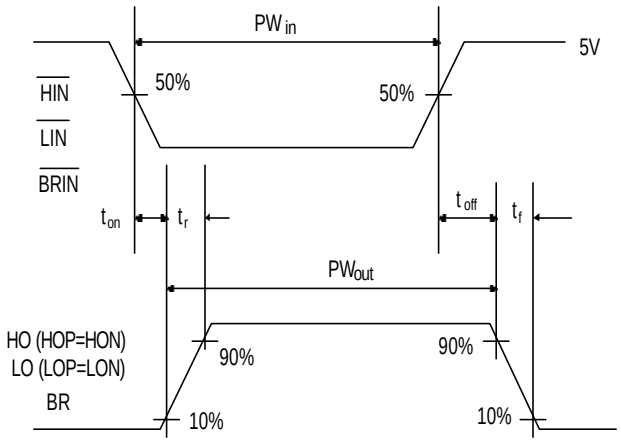


Figure 4. Switching Time Waveforms

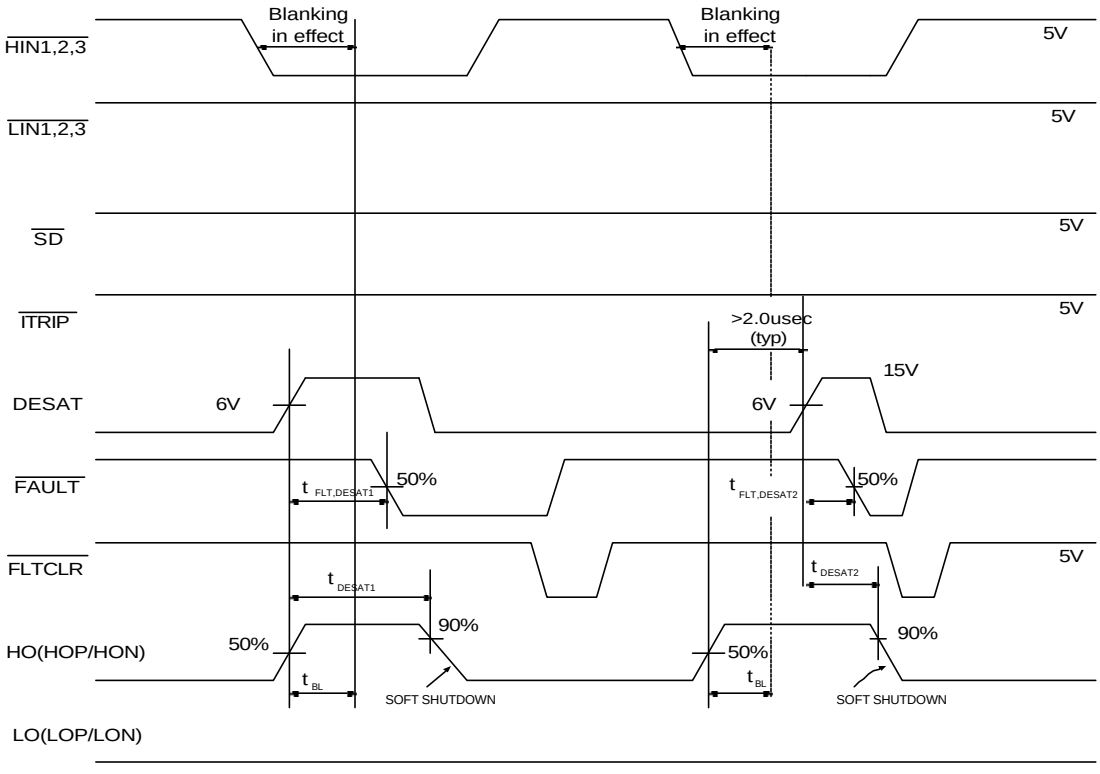


Figure 5. DESAT Timing

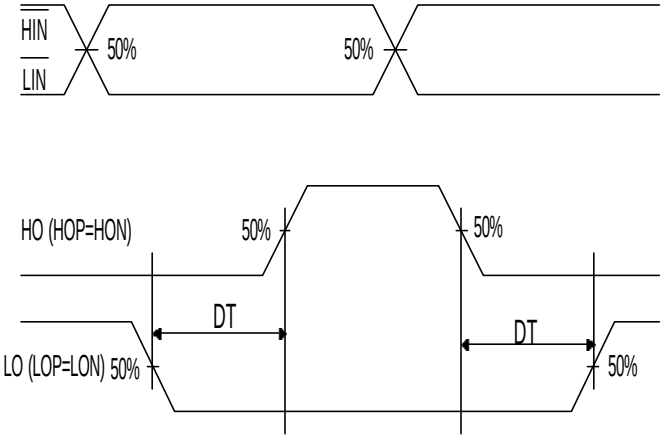


Figure 6. Internal Deadtime Timing

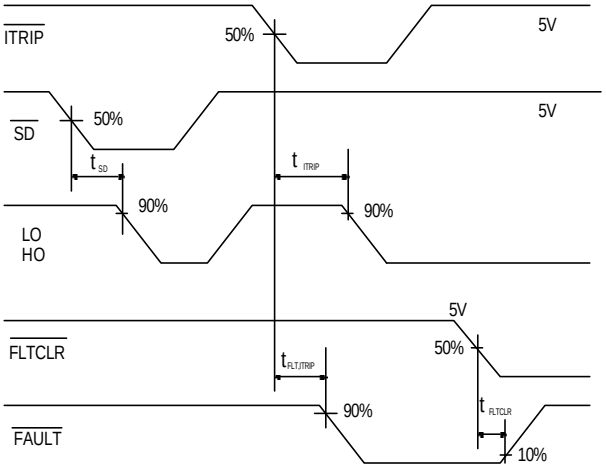
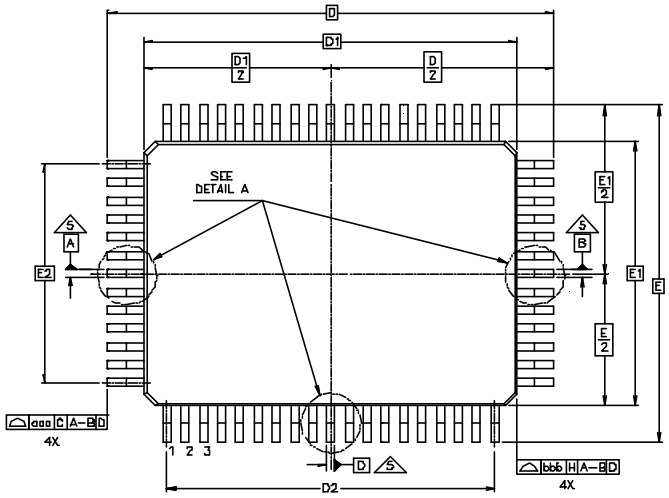
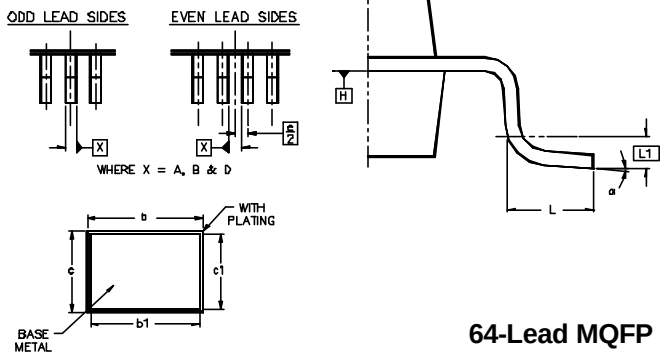


Figure 7. SD, ITRIP Timing

Case outlines





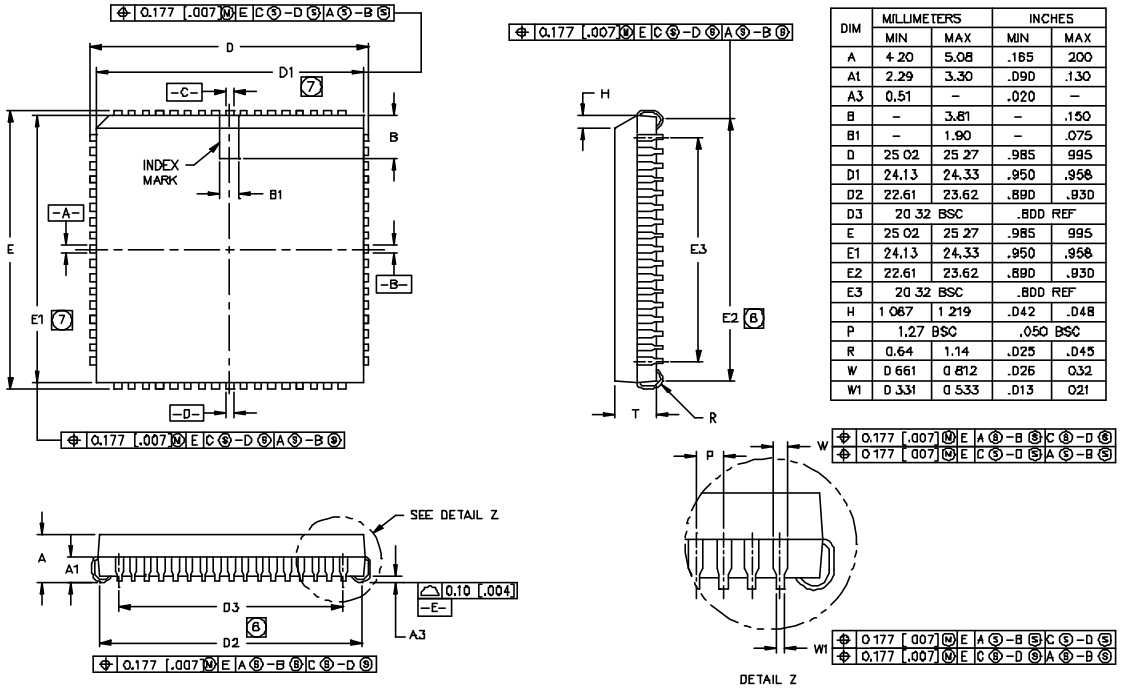
SYMBOL	DIMENSIONS					
	MILLIMETERS MS-022GA-2			INCHES MS-022GA-2		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.50	2.83	3.15	.098	.111	.124
A1	0.00	0.13	0.25	.000	.005	.010
A2	2.50	2.70	2.90	.098	.106	.114
b	0.35	---	0.50	.014	---	.020
b1	0.35	0.40	0.45	.014	.016	.018
c	0.09	---	0.20	.004	---	.007
c1	0.09	---	0.16	.004	---	.006
D	23.20 BSC			.913 BSC		
D1	20.00 BSC			.787 BSC		
D2	18.00 REF			.709 REF		
E	17.20 BSC			.677 BSC		
E1	14.00 BSC			.551 BSC		
E2	12.00 REF			.472 REF		
e	1.00 BSC			.039 BSC		
L	0.73	0.88	1.03	.029	.035	.040
L1	0.25 BSC			.010 BSC		
α	0°	---	7°	0°	---	7°
aaa	0.25			.010		
bbb	0.20			.008		
ccc	0.20			.008		
ddd	0.10			.004		

NOTES

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS AND INCHES.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
5. DATUM A – B AND D TO BE DETERMINED AT DATUM PLANE H.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. OUTLINE CONFORMS TO JEDEC OUTLINE MS-022GB1.

64-Lead MQFP

01-6054 00
01-202301 MS-022GA-2



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.20	5.08	.165	200
A1	2.29	3.30	.090	.130
A3	0.51	–	.020	–
B	–	3.81	–	.150
B1	–	1.90	–	.075
D	25.02	25.27	.985	995
D1	24.13	24.33	.950	.958
D2	22.61	23.62	.890	.930
D3	20.32 BSC		.800 REF	
E	25.02	25.27	.985	995
E1	24.13	24.33	.950	.958
E2	22.61	23.62	.890	.930
E3	20.32 BSC		.800 REF	
H	1.067	1.219	.042	.048
P	1.27 BSC		.050 BSC	
R	0.64	1.14	.025	.045
W	0.661	0.812	.026	032
W1	0.331	0.533	.013	021

NOTES:

1. DIMENSIONING & TOLERENCING PER ANSI Y14.5M–1982
2. DIMENSIONS SHOWN IN MILLIMETERS [INCHES]
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE MS–018AC.
5. DATUMS –A–, –B–, –C–, & –D– ARE DETERMINED BY WHERE THE TOP OF THE LEADS EXIT PLASTIC BODY AT MOLD PARTING LINE.
6. TO BE MEASURED AT –E– SEATING PLANE.
7. DIMENSIONS DO NOT INCLUDE MOLD FLASH, ALLOWABLE FLASH IS 0.254 [.010].

68-Lead PLCC

01-6055 00
01-3068 01 (MS-018AC)