

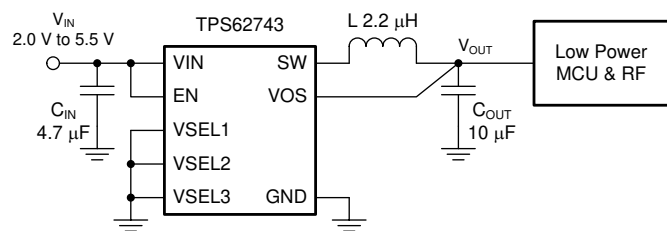
TPS62743 TPS627431 300/400 mA High Efficiency Buck Converter with Ultra-low Quiescent Current

1 Features

- Input voltage range V_{IN} from 2.15 V to 5.5 V
- Input voltage range down to 2.0 V once started
- output current
 - TPS62743 300 mA
 - TPS627431 400 mA
- 360-nA operational quiescent current
- Up to 90% efficiency at 10- μ A output current
- Power save mode operation
- Selectable output voltages
 - Eight voltage options between 1.2 V to 3.3 V
- Output voltage discharge
- Low output voltage ripple
- Automatic transition to no ripple 100% mode
- RF friendly DCS-Control™
- Total solution size < 10 mm²
- Small 1.6-mm × 0.9-mm, 8-ball WCSP package

2 Applications

- [Wearables](#)
- [Fitness tracker](#)
- [Smartwatch](#)
- Health monitoring
- [Bluetooth®](#) low energy, RF4CE, [Zigbee](#)
- High-efficiency, ultra-low power applications
- Energy harvesting



Typical Application

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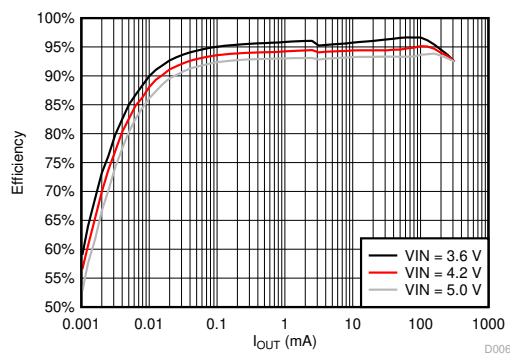
3 Description

The TPS62743 is a high efficiency step down converter with ultra low quiescent current of typical 360 nA. The device is optimized to operate with a 2.2- μ H inductor and 10 μ F output capacitor. The device uses DCS-Control™ and operates with a typical switching frequency of 1.2 MHz. In Power Save Mode the device extends the light load efficiency down to a load current range of 10- μ A and below. TPS62743 provides an output current of 300 mA. Once started the device operates down to an input voltage range of 2.0 V. This allows to operate the device directly from a single Li-MnO₂ coin cell.

The TPS62743 provides 8 programmable output voltages between 1.2V and 3.3V selectable by three selection pins. The TPS62743 is optimized to provide a low output voltage ripple and low noise using a small output capacitor. Once the input voltage comes close to the output voltage the device enters the No Ripple 100% mode to prevent an increase of output ripple voltage. In this operation mode the device stops switching and turns the high side MOSFET switch on.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-----------|-------------------|
| TPS62743 | DSBGA (8) | 1.57 mm × 0.88 mm |
| TPS627431 | DSBGA (8) | 1.57 mm x 0.88 mm |



D006



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (May 2016) to Revision B (March 2021) | Page |
|---|-------------|
| • Updated the numbering format for tables, figures and cross-references throughout the document. | 1 |

| Changes from Revision * (June 2015) to Revision A (May 2016) | Page |
|---|-------------|
| • Added TPS627431 device to data sheet | 1 |
| • Added device option TPS627431: 400mA output current, other output voltages than TPS62743..... | 1 |
| • Added TPS627431 to Section 5 | 3 |
| • Added Figure 9-2 | 11 |

5 Device Comparison Table

| T _A | PART NUMBER | OUTPUT VOLTAGE SETTINGS (VSEL 1 - 3) | OUTPUT CURRENT | PACKAGE MARKING |
|----------------|-------------|--|----------------|-----------------|
| –40°C to 85°C | TPS62743 | 1.2 V, 1.5 V, 1.8 V, 2.1 V, 2.5 V, 2.8 V, 3.0 V, 3.3 V | 300 mA | TPS743 |
| –40°C to 85°C | TPS627431 | 1.3 V, 1.4 V, 1.6 V, 1.7 V, 1.9 V, 2.0 V, 2.9 V, 3.1 V | 400 mA | 627431 |

6 Pin Configuration and Functions

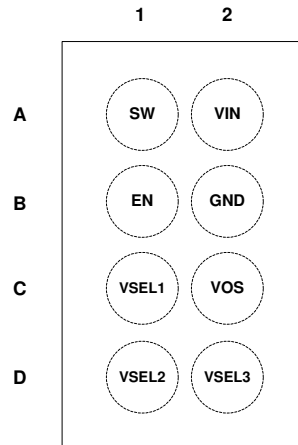


Figure 6-1. YFP Package 8-Pin DSBGA Top View

Table 6-1. Pin Functions

| PIN | | I/O | DESCRIPTION |
|-------|----|-----|---|
| NAME | NO | | |
| VIN | A2 | PWR | V _{IN} power supply pin. Connect the input capacitor close to this pin for best noise and voltage spike suppression. A ceramic capacitor of 4.7 μF is required. |
| SW | A1 | OUT | The switch pin is connected to the internal MOSFET switches. Connect the inductor to this terminal. |
| GND | B2 | PWR | GND supply pin. Connect this pin close to the GND terminal of the input and output capacitor. |
| VOS | C2 | IN | Feedback pin for the internal feedback divider network and regulation loop. Discharges V _{OUT} when the converter is disabled. Connect this pin directly to the output capacitor with a short trace. |
| VSEL3 | D2 | IN | Output voltage selection pins. See Table 6-2 for V _{OUT} selection. These pin must be terminated. The pins can be dynamically changed during operation. |
| VSEL2 | D1 | | |
| VSEL1 | C1 | | |
| EN | B1 | IN | High level enables the devices, low level turns the device off. The pin must be terminated. |

Table 6-2. Output Voltage Setting

| OUTPUT VOLTAGE SETTING V _{OUT} [V] | | VSEL SETTING | | |
|---|-----------|--------------|-------|-------|
| TPS62743 | TPS627431 | VSEL3 | VSEL2 | VSEL1 |
| 1.2 | 1.3 | 0 | 0 | 0 |
| 1.5 | 1.4 | 0 | 0 | 1 |
| 1.8 | 1.6 | 0 | 1 | 0 |
| 2.1 | 1.7 | 0 | 1 | 1 |
| 2.5 | 1.9 | 1 | 0 | 0 |
| 2.8 | 2.0 | 1 | 0 | 1 |
| 3.0 | 2.9 | 1 | 1 | 0 |
| 3.3 | 3.1 | 1 | 1 | 1 |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| | | MIN | MAX | UNIT |
|--|-------------|------|------------------------|------|
| Pin voltage ⁽²⁾ | VIN | -0.3 | 6 | V |
| | SW, | -0.3 | V _{IN} + 0.3V | V |
| | EN, VSEL1-3 | -0.3 | V _{IN} + 0.3V | V |
| | VOS | -0.3 | 3.7 | V |
| Operating junction temperature, T _J | | -40 | 125 | °C |
| Storage temperature, T _{stg} | | -65 | 150 | °C |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal GND.

7.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | ±500 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|------------------|---|--|------|-----|-----|------|
| V _{IN} | Supply voltage V _{IN} | | 2.15 | | 5.5 | V |
| V _{IN} | Supply voltage V _{IN} , once started | | 2.0 | | 5.5 | V |
| I _{OUT} | Device output current | TPS62743 / TPS627431 5.5V ≥ V _{IN} ≥ (V _{OUTnom} + 0.7V) ≥ 2.15V | | | 300 | mA |
| | | 5.5V ≥ V _{IN} ≥ (V _{OUTnom} + 0.7V) ≥ 3V | | | 400 | |
| T _J | Operating junction temperature range | | -40 | | 125 | °C |

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TPS62743 | |
|-------------------------------|--|----------|------|
| | | YFP | |
| | | 8 PINS | |
| | | | UNIT |
| R _{θJA} | Junction-to-ambient thermal resistance | 103 | °C/W |
| R _{θJctop} | Junction-to-case (top) thermal resistance | 1.0 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 20 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 0.3 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 20 | °C/W |
| R _{θJcbot} | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

V_{IN} = 3.6V, T_A = -40°C to 85°C typical values are at T_A = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|---------------------------------------|--|-----|-------|------|------|
| SUPPLY | | | | | | |
| I _Q | Operating quiescent current | EN = V _{IN} , I _{OUT} = 0μA, V _{OUT} = 1.8V, device not switching | | 360 | 1800 | nA |
| | | EN = V _{IN} , I _{OUT} = 0mA, V _{OUT} = 1.8V, device switching | | 460 | | |
| I _{SD} | Shutdown current | EN = GND, shutdown current into V _{IN} | | 70 | 1000 | nA |
| V _{TH_UVLO+} | Undervoltage lockout threshold | Rising V _{IN} | | 2.075 | 2.15 | V |
| V _{TH_UVLO-} | | Falling V _{IN} | | 1.925 | 2 | |
| INPUTS (EN, VSEL1-3) | | | | | | |
| V _{IHTH} | High level input threshold | 2.2V ≤ V _{IN} ≤ 5.5V | | | 1.1 | V |
| V _{ILTH} | Low level input threshold | 2.2V ≤ V _{IN} ≤ 5.5V | 0.4 | | | V |
| I _{IN} | Input bias Current | | | 10 | 25 | nA |
| POWER SWITCHES | | | | | | |
| R _{DS(ON)} | High side MOSFET on-resistance | I _{OUT} = 50mA | | 0.45 | 1.12 | Ω |
| | Low Side MOSFET on-resistance | | | 0.22 | 0.65 | |
| I _{LIMF} | High side MOSFET switch current limit | TPS62743 3.0V ≤ V _{IN} ≤ 5.5V | 480 | 600 | 720 | mA |
| | | TPS627431 3.0V ≤ V _{IN} ≤ 5.5V | 590 | 650 | 800 | |
| | Low side MOSFET switch current limit | TPS62743 | | 600 | | |
| | | TPS627431 | | 650 | | |
| OUTPUT VOLTAGE DISCHARGE | | | | | | |
| R _{Dsch_VOS} | MOSFET on-resistance | EN = GND, I _{VOS} = -10mA into VOS pin | | 30 | 65 | Ω |
| I _{IN_VOS} | Bias current into VOS pin | EN = V _{IN} , V _{OUT} = 2V | | 40 | 1010 | nA |

$V_{IN} = 3.6V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$ typical values are at $T_A = 25^{\circ}C$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------|---|--|------|-------|-----|------|
| AUTO 100% MODE TRANSITION | | | | | | |
| V_{TH_100+} | Auto 100% Mode leave detection threshold ⁽¹⁾ | Rising V_{IN} , 100% Mode is left with $V_{IN} = V_{OUT} + V_{TH_100+}$ | 150 | 250 | 350 | mV |
| V_{TH_100-} | Auto 100% Mode enter detection threshold ⁽¹⁾ | Falling V_{IN} , 100% Mode is entered with $V_{IN} = V_{OUT} + V_{TH_100-}$ | 85 | 200 | 290 | |
| OUTPUT | | | | | | |
| $I_{LIM_softstart}$ | High side softstart switch current limit | EN=low to high | 80 | 150 | 200 | mA |
| | Low side softstart switch current limit | | 150 | | | |
| V_{OUT} | Output voltage range | Output voltages are selected with pins VSEL 1 - 3 | 1.2 | | 3.3 | V |
| | Output voltage accuracy | $I_{OUT} = 10mA$, $V_{OUT} = 1.8V$ | -2.5 | 0% | 2.5 | |
| | | $I_{OUT} = 100mA$, $V_{OUT} = 1.8V$ | -2 | 0% | 2 | |
| | DC output voltage load regulation | $V_{OUT} = 1.8V$ | | 0.001 | | %/mA |
| | DC output voltage line regulation | $V_{OUT} = 1.8V$, $I_{OUT} = 100mA$, $2.2V \leq V_{IN} \leq 5.0V$ | | 0 | | %/V |

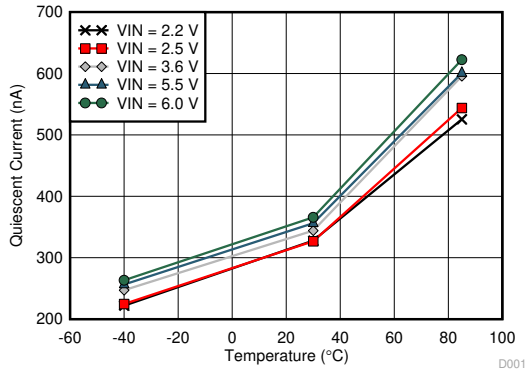
- (1) V_{IN} is compared to the programmed output voltage (V_{OUT}). When $V_{IN}-V_{OUT}$ falls below V_{TH_100-} , the device enters 100% Mode by turning the high side MOSFET on. The 100% Mode is exited when $V_{IN}-V_{OUT}$ exceeds V_{TH_100+} and the device starts switching. The hysteresis for the 100% Mode detection threshold $V_{TH_100+} - V_{TH_100-}$ will always be positive and will be approximately 50 mV(typ)

7.6 Timing Requirements

 $V_{IN} = 3.6V$, $T_J = -40^{\circ}C$ to $85^{\circ}C$ typical values are at $T_A = 25^{\circ}C$ (unless otherwise noted)

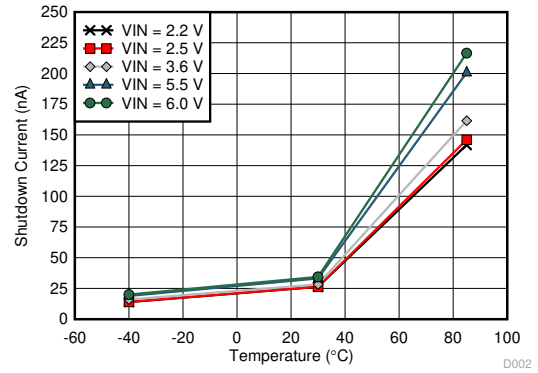
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|-------------------------------|--|-----|-----|------|---------|
| OUTPUT | | | | | | |
| t_{ONmin} | Minimum ON time | $V_{OUT} = 2.0V$, $I_{OUT} = 0$ mA | | 225 | | ns |
| t_{OFFmin} | Minimum OFF time | $V_{IN} = 2.3V$ | | 50 | | ns |
| $t_{Startup_delay}$ | Regulator start up delay time | From transition EN = low to high until device starts switching | | 10 | 25 | ms |
| $t_{Softstart}$ | Softstart time | $2.2V \leq V_{IN} \leq 5.5V$, EN = V_{IN} | | 700 | 1200 | μs |

7.7 Typical Characteristics



EN = VIN, V_{OUT} = 1.8V Device Not Switching

Figure 7-1. Quiescent Current vs Temperature



EN = GND

Figure 7-2. Shutdown Current I_{SD} vs Temperature

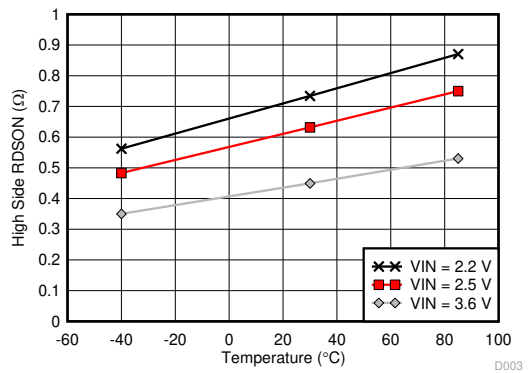


Figure 7-3. High Side R_{DS(on)} vs Temperature

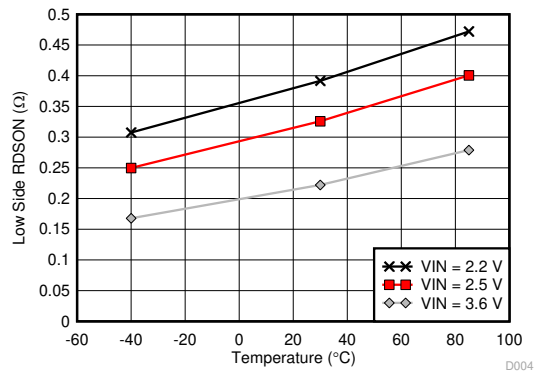


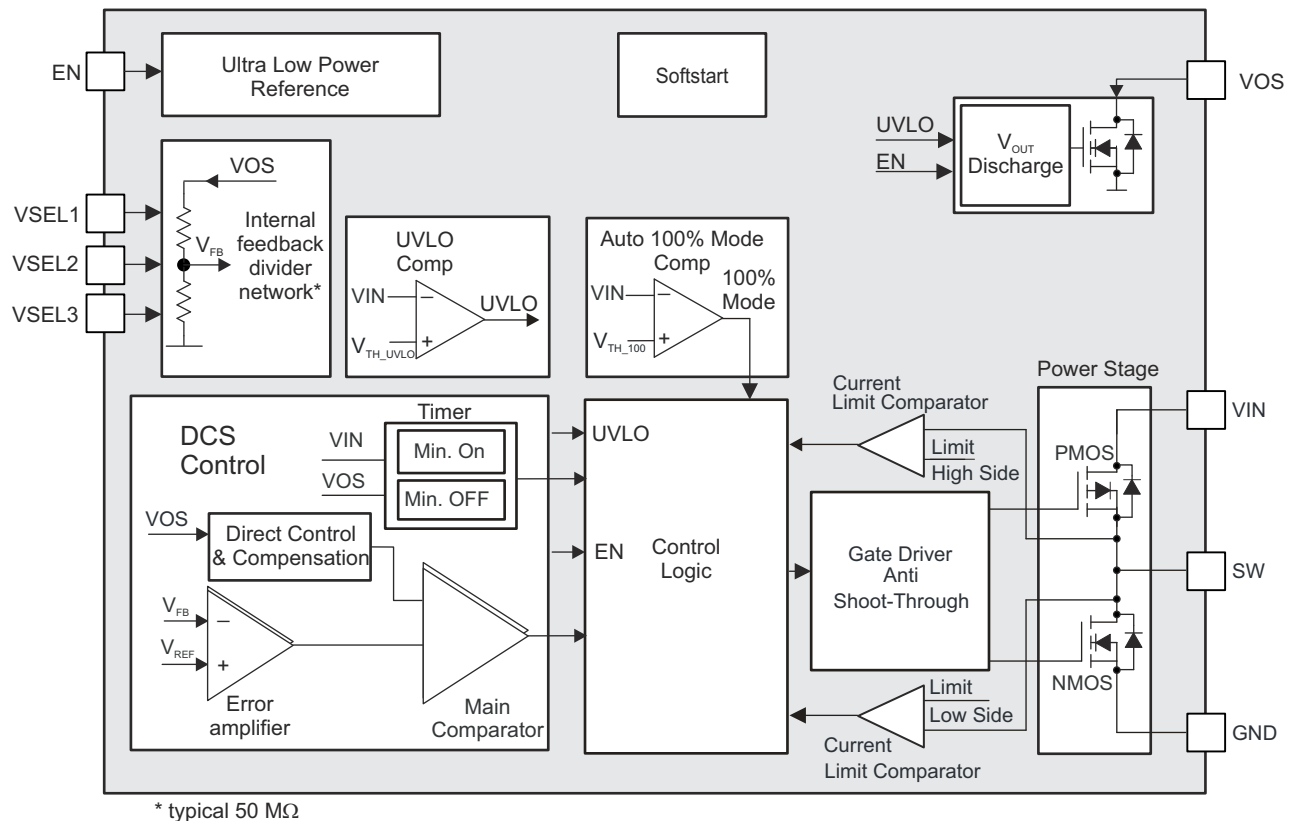
Figure 7-4. Low-side R_{DS(on)} vs Temperature

8 Detailed Description

8.1 Overview

The TPS62743 is a high frequency step down converter with ultra low quiescent current. The device operates with a quasi fixed switching frequency typically at 1.2 MHz. Using TI's DCS-Control™ topology the device extends the high efficiency operation area down to a few microamperes of load current during Power Save Mode Operation.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 DCS-Control™

TI's DCS-Control™ (Direct Control with Seamless Transition into Power Save Mode) is an advanced regulation topology, which combines the advantages of hysteretic and voltage mode control. Characteristics of DCS-Control™ are excellent AC load regulation and transient response, low output ripple voltage and a seamless transition between PFM and PWM mode operation. DCS-Control™ includes an AC loop which senses the output voltage (VOS pin) and directly feeds the information to a fast comparator stage. This comparator sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. In order to achieve accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

The DCS-Control™ topology supports PWM (Pulse Width Modulation) mode for medium and high load conditions and a Power Save Mode at light loads. During PWM mode, it operates in continuous conduction mode. The switching frequency is typically 1.2 MHz with a controlled frequency variation depending on the input voltage and load current. If the load current decreases, the converter seamlessly enters Power Save Mode to maintain high efficiency down to very light loads. In Power Save Mode, the switching frequency varies linearly with the load current. Since DCS-Control™ supports both operation modes within one single building block, the transition from PWM to Power Save Mode is seamless with minimum output voltage ripple. The TPS62743

offers both excellent DC voltage and superior load transient regulation, combined with low output voltage ripple, minimizing interference with RF circuits.

8.3.2 Power Save Mode Operation

In Power Save Mode the device operates in PFM (Pulse Frequency Modulation) that generates a single switching pulse to ramp up the inductor current and recharges the output capacitor, followed by a sleep period where most of the internal circuits are shutdown to achieve lowest operating quiescent current. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current. During the sleep periods, the current consumption of TPS62743 is reduced to 360 nA. This low quiescent current consumption is achieved by an ultra low power voltage reference, an integrated high impedance feedback divider network and an optimized Power Save Mode operation.

8.3.3 Output Voltage Selection

The TPS62743 doesn't require an external resistor divider network to program the output voltage. The device integrates a high impedance feedback resistor divider network that is programmed by the pins VSEL1-3. TPS62743 supports an output voltage range from 1.2 V to 3.3 V. The output voltage is programmed according to [Table 6-2](#). The output voltage can be changed during operation. This can be used for simple dynamic output voltage scaling.

8.3.4 Output Voltage Discharge of the Buck Converter

The device provides automatic output voltage discharge when EN is pulled low or the UVLO is triggered. The output of the buck converter is discharged over VOS. Because of this the output voltage will ramp up from zero once the device is enabled again. This is very helpful for accurate start-up sequencing.

8.3.5 Undervoltage Lockout UVLO

To avoid misoperation of the device at low input voltages, an undervoltage lockout is used. The UVLO shuts down the device at a maximum voltage level of 2.0 V. The device will start at a UVLO level of 2.15 V.

8.3.6 Short circuit protection

The TPS6274x integrates a current limit on the high side, as well on the low side MOSFETs to protect the device against overload or short circuit conditions. The peak current in the switches is monitored cycle by cycle. If the high side MOSFET current limit is reached, the high side MOSFET is turned off and the low side MOSFET is turned on until the switch current decreases below the low side MOSFET current limit. Once the low side MOSFET current limit trips, the low side MOSFET is turned off and the high side MOSFET turns on again.

8.4 Device Functional Modes

8.4.1 Enable and Shutdown

The device is turned on with EN=high. With EN=low the device enters shutdown. This pin must be terminated.

8.4.2 Device Start-up and Softstart

The device has an internal softstart to minimize input voltage drop during start-up. This allows the operation from high impedance battery cells. Once the device is enabled the device starts switching after a typical delay time of 10ms. Then the softstart time of typical 700 μ s begins with a reduced current limit of typical 150 mA. When this time passed by the device enters full current limit operation. This allows a smooth start-up and the device can start into full load current. Furthermore, larger output capacitors impact the start-up behaviour of the DC/DC converter. Especially when the output voltage does not reach its nominal value after the typical soft-start time of 700 μ s, has passed.

8.4.3 Automatic Transition Into No Ripple 100% Mode

Once the input voltage comes close to the output voltage, the DC/DC converter stops switching and enters 100% duty cycle operation. It connects the output V_{OUT} via the inductor and the internal high side MOSFET switch to the input V_{IN} , once the input voltage V_{IN} falls below the 100% mode enter threshold, V_{TH_100-} . The DC/DC regulator is turned off, switching stops and therefore no output voltage ripple is generated. Since the output is connected to the input, the output voltage follows the input voltage minus the voltage drop across the internal high side switch and the inductor. Once the input voltage increases and trips the 100% mode exit threshold, V_{TH_100+} , the DC/DC regulator turns on and starts switching again. See [Figure 8-1](#) and [Figure 9-21](#).

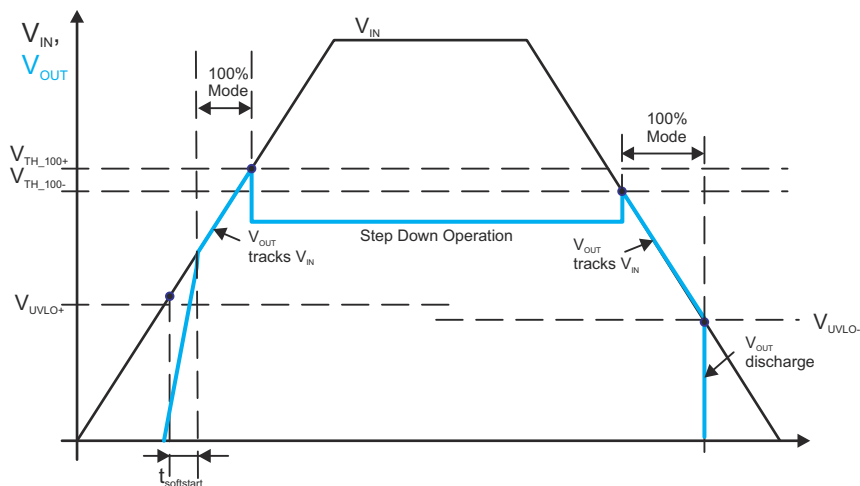


Figure 8-1. Automatic Transition into 100% Mode

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS62743 is a high efficiency step down converter with ultra low quiescent current of typically 360 nA. The device operates with a tiny 2.2- μ H inductor and 10- μ F output capacitor over the entire recommended operation range. A dedicated measurement set-up is required for the light load efficiency measurement and device quiescent current due to the operation in the sub microampere range. In this range any leakage current in the measurement set-up will impact the measurement results.

9.2 Typical Application

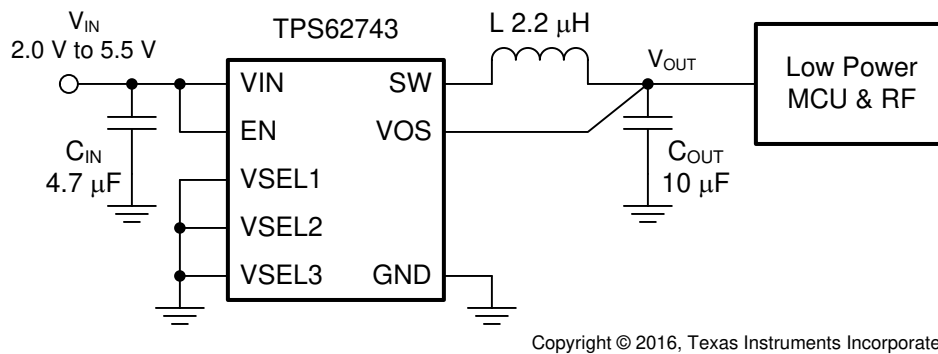


Figure 9-1. TPS62743 Typical Application Circuit

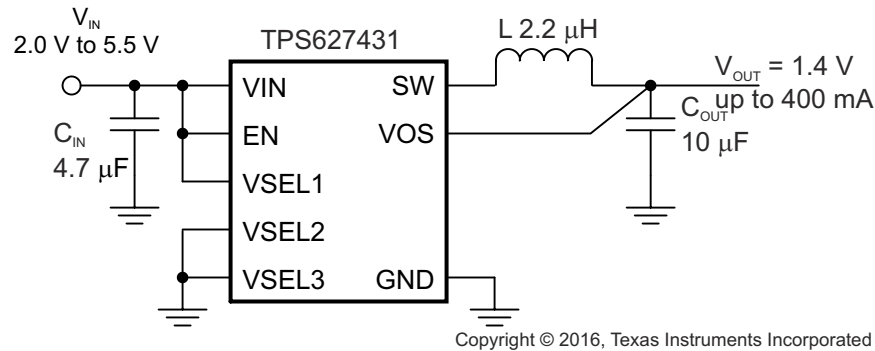


Figure 9-2. TPS627431 Typical Application Circuit

9.2.1 Design Requirements

The TPS62743 is a highly integrated DC/DC converter. The output voltage is set via a VSEL pin interface. The design guideline provides a component selection to operate the device within the recommended operating conditions.

[Table 9-1](#) shows the list of components for the Application Characteristic Curves.

Table 9-1. Components for Application Characteristic Curves

| Reference | Description | Value | Manufacturer |
|-----------|--------------------------------------|-------------|-------------------|
| TPS62743 | 360nA Iq step down converter | | Texas Instruments |
| CIN | Ceramic capacitor, GRM155R61C475ME15 | 4.7 μ F | Murata |
| COU | Ceramic capacitor, GRM155R60J106ME11 | 10 μ F | Murata |
| L | Inductor DFE201610C | 2.2 μ H | Toko |

9.2.2 Detailed Design Procedure

The first step in the design procedure is the selection of the output filter components. To simplify this process, [Table 9-2](#) outlines possible inductor and capacitor value combinations.

Table 9-2. Recommended LC Output Filter Combinations

| Inductor Value [μ H] ⁽²⁾ | Output Capacitor Value [μ F] ⁽¹⁾ | | | | |
|---|--|------------------|------------|------------|-------------|
| | 4.7 μ F | 10 μ F | 22 μ F | 47 μ F | 100 μ F |
| 2.2 | √ | √ ⁽³⁾ | √ | √ | |

- (1) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance varies by +20% and –50%.
 (2) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by 20% and -30%.
 (3) Typical application configuration. Other check marks indicate alternative filter combinations.

9.2.2.1 Inductor Selection

The inductor value affects the peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT} and can be estimated according to [Equation 1](#).

[Equation 2](#) calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current, as calculated with [Equation 2](#). This is recommended because during a heavy load transient the inductor current rises above the calculated value. A more conservative way is to select the inductor saturation current according to the high-side MOSFET switch current limit, I_{LIMF} .

$$\Delta I_L = V_{out} \times \frac{1 - \frac{V_{out}}{V_{in}}}{L \times f} \quad (1)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (2)$$

where

- f = Switching Frequency
- L = Inductor Value
- ΔI_L = Peak to Peak inductor ripple current
- I_{Lmax} = Maximum Inductor current

[Table 9-3](#) shows a list of possible inductors.

Table 9-3. List of Possible Inductors

| INDUCTANCE [μ H] | DIMENSIONS [mm^3] | INDUCTOR TYPE | Isat/DCR | SUPPLIER ⁽¹⁾ | Comment |
|-----------------------|------------------------------|----------------|----------------------|-------------------------|---|
| 2.2 | 2.0 x 1.6 x 1.0 | DFE201610C | 1.4 A/170 m Ω | TOKO | Efficiency plot Figure 9-9 |
| 2.2 | 2.0 x 1.25 x 1.0 | MIPSZ2012D 2R2 | 0.7 A/230 m Ω | FDK | |
| 2.2 | 2.0 x 1.2 x 1.0 | 744 797 752 22 | 0.7 A/200 m Ω | Würth Elektronik | |
| 2.2 | 1.6 x 0.8 x 0.8 | MDT1608-CH2R2M | 0.7 A/300 m Ω | TOKO | |

(1) See [Third-party Products Disclaimer](#)

9.2.2.2 Output Capacitor Selection

The DCS-Control™ scheme of the TPS62743 allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. At light load currents, the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value. A larger output capacitors can be used reducing the output voltage ripple. The leakage current of the output capacitor adds to the overall quiescent current.

9.2.2.3 Input Capacitor Selection

Because the buck converter has a pulsating input current, a low ESR input capacitor is required for best input voltage filtering to minimize input voltage spikes. For most applications a 4.7- μ F input capacitor is sufficient. When operating from a high impedance source, like a coin cell a larger input buffer capacitor $\geq 10\mu$ F is recommended avoiding voltage drops during start-up and load transients. The input capacitor can be increased without any limit for better input voltage filtering. The leakage current of the input capacitor adds to the overall quiescent current. [Table 9-4](#) shows a selection of input and output capacitors.

Table 9-4. List of Possible Capacitors⁽¹⁾

| CAPACITANCE [μ F] | SIZE | CAPACITOR TYPE | SUPPLIER |
|------------------------|------|-------------------|----------|
| 4.7 | 0402 | GRM155R61C475ME15 | Murata |
| 10 | 0402 | GRM155R60J106ME11 | Murata |

(1) See [Third-party Products Disclaimer](#)

9.2.3 Application Curves

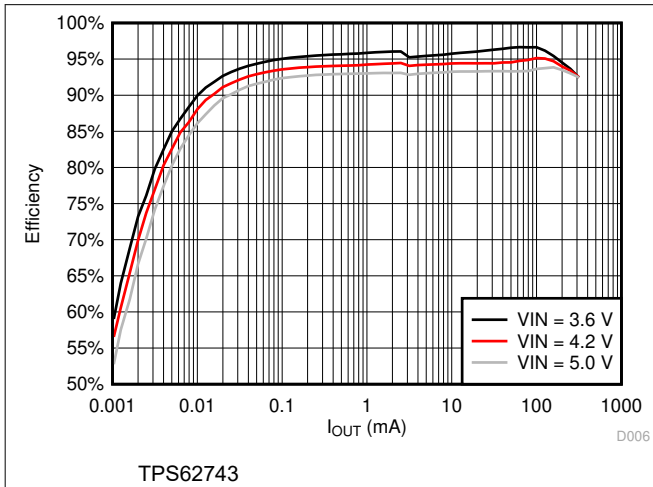


Figure 9-3. Efficiency vs Load Current, $V_{OUT} = 3.3\text{ V}$

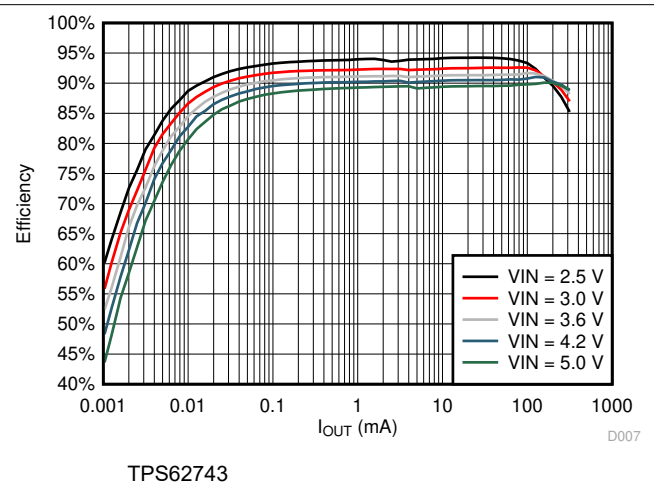


Figure 9-4. Efficiency vs Load Current; $V_{OUT} = 2.1\text{ V}$

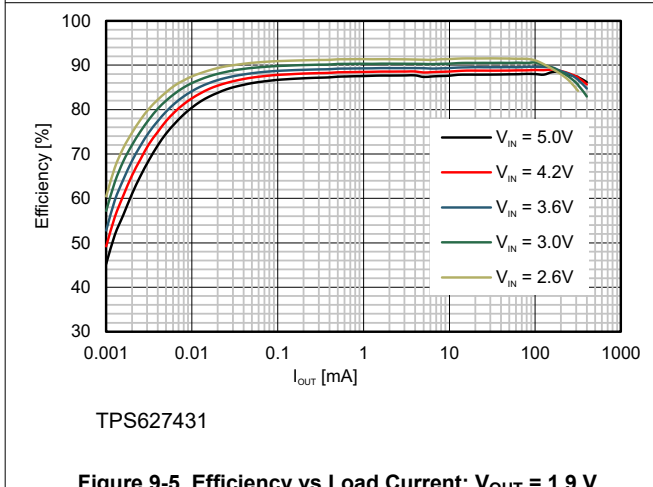


Figure 9-5. Efficiency vs Load Current; $V_{OUT} = 1.9\text{ V}$

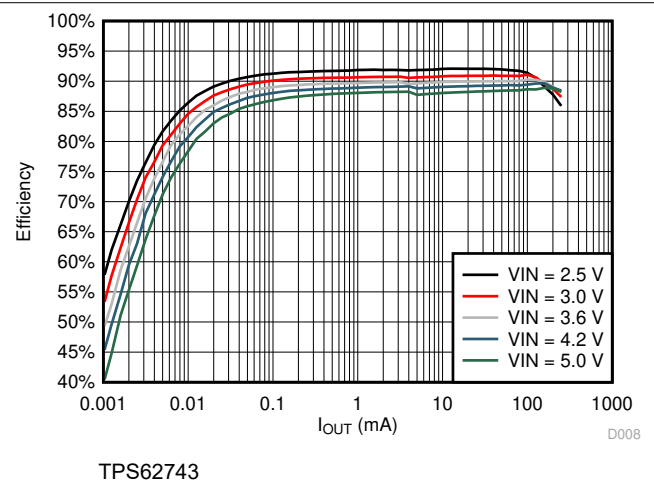


Figure 9-6. Efficiency vs Load Current; $V_{OUT} = 1.8\text{ V}$

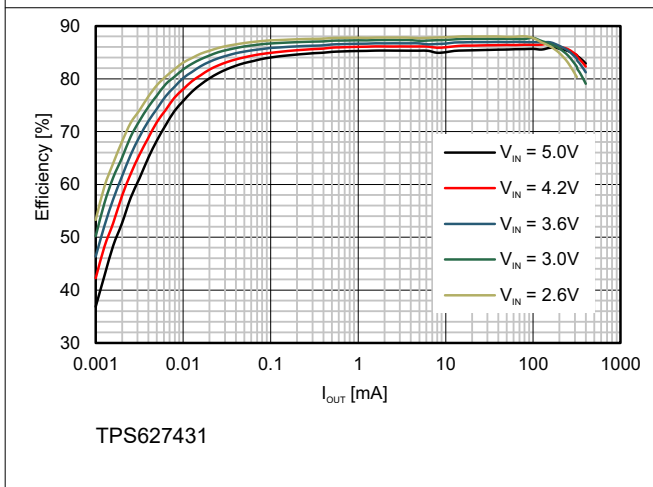


Figure 9-7. Efficiency vs Load Current; $V_{OUT} = 1.4\text{ V}$

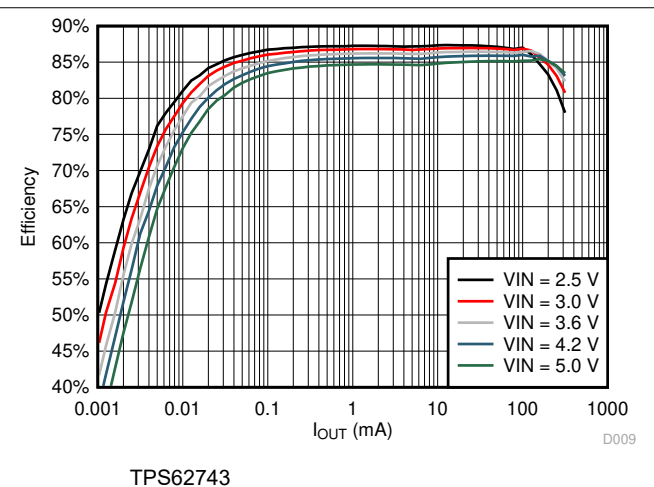


Figure 9-8. Efficiency vs Load Current; $V_{OUT} = 1.2\text{ V}$

9.2.3 Application Curves (continued)

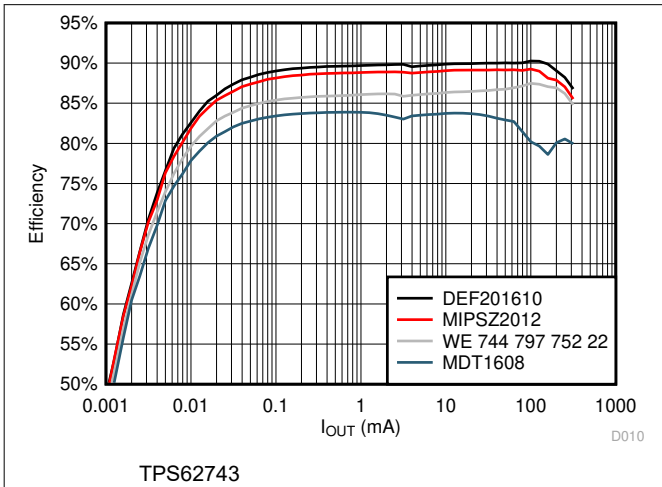


Figure 9-9. Efficiency vs Load Current; $V_{OUT} = 1.8\text{ V}$

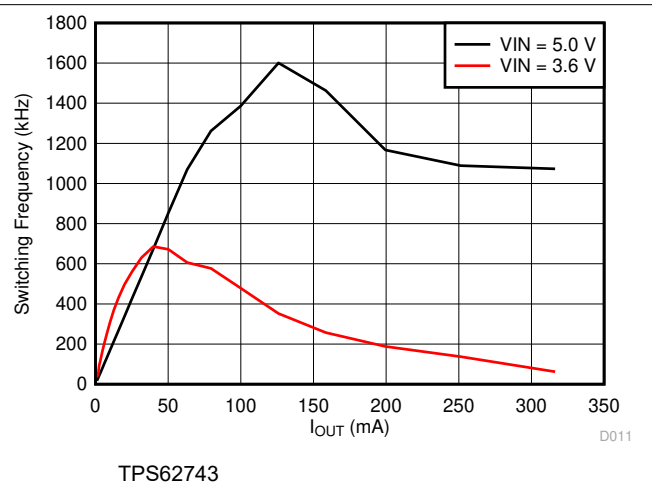


Figure 9-10. Switching Frequency vs Load Current $V_{OUT} = 3.3\text{ V}$

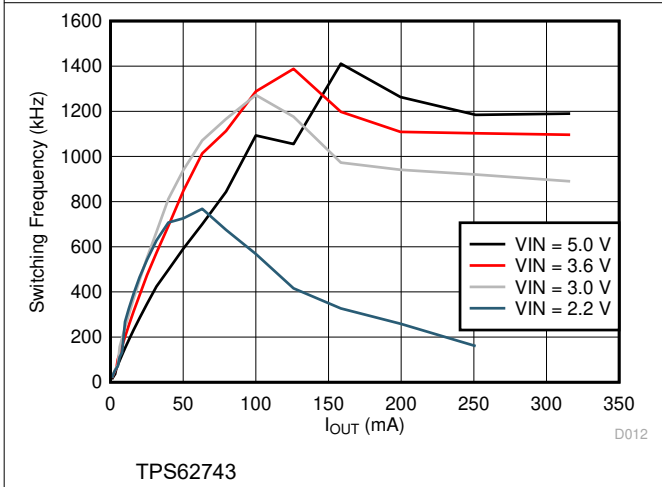


Figure 9-11. Switching Frequency vs Load Current $V_{OUT} = 1.8\text{ V}$

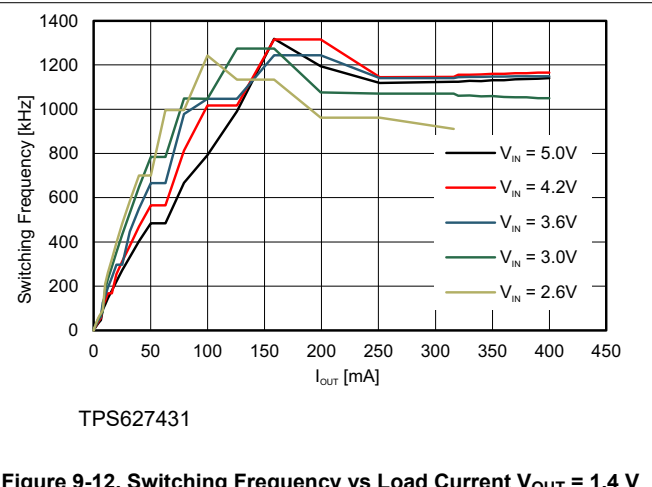


Figure 9-12. Switching Frequency vs Load Current $V_{OUT} = 1.4\text{ V}$

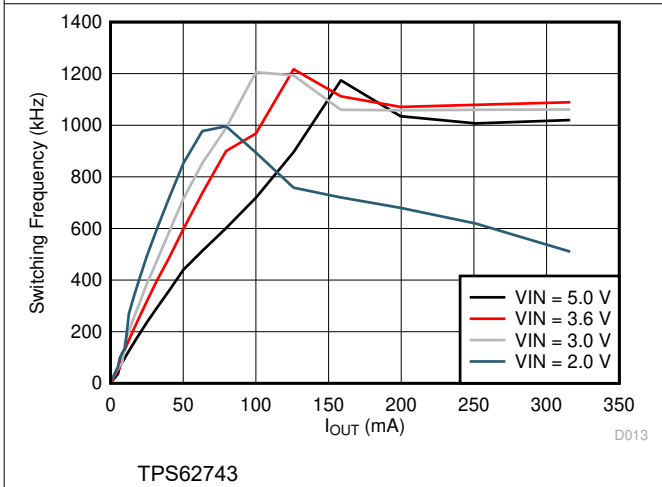


Figure 9-13. Switching Frequency vs Load Current $V_{OUT} = 1.2\text{ V}$

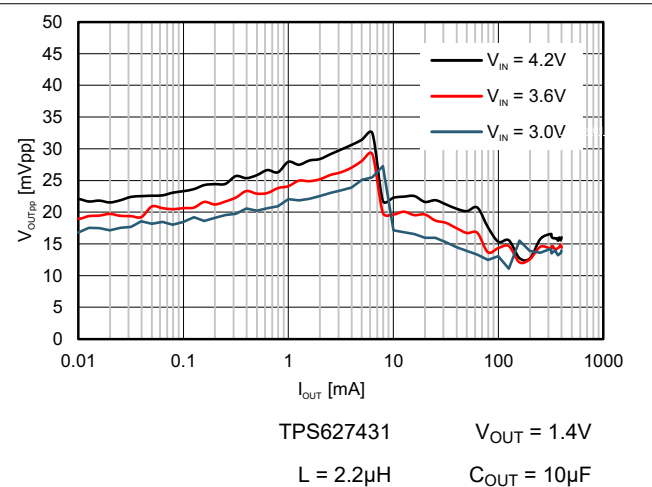


Figure 9-14. Typical Output Ripple Voltage $V_{OUT} = 1.4\text{ V}$

9.2.3 Application Curves (continued)

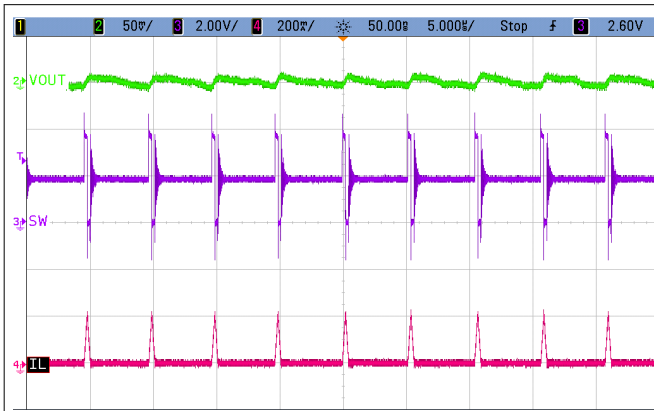


Figure 9-15. PFM (Power Save Mode) Mode Operation

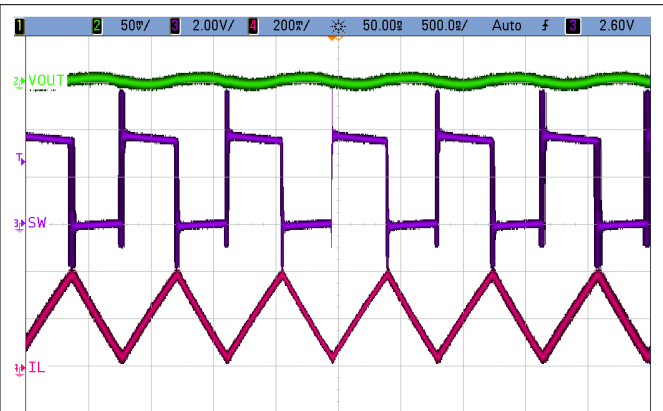


Figure 9-16. PWM Mode Operation

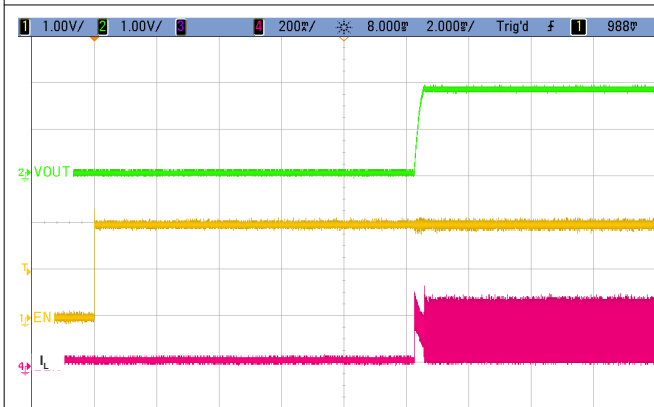


Figure 9-17. Startup Into 100 mA Electronic Load EN Delay + Soft-Start Delay

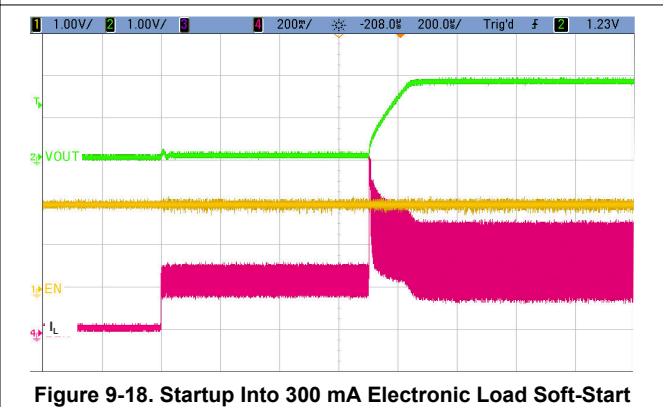


Figure 9-18. Startup Into 300 mA Electronic Load Soft-Start Delay

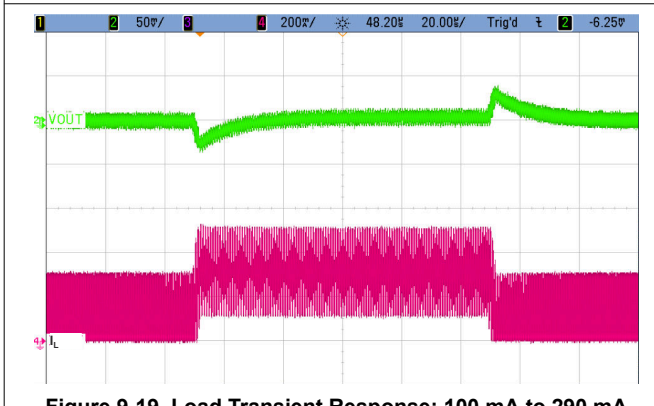


Figure 9-19. Load Transient Response; 100 mA to 290 mA

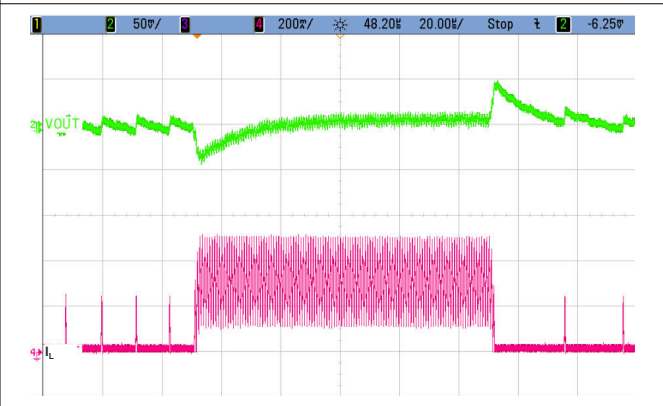
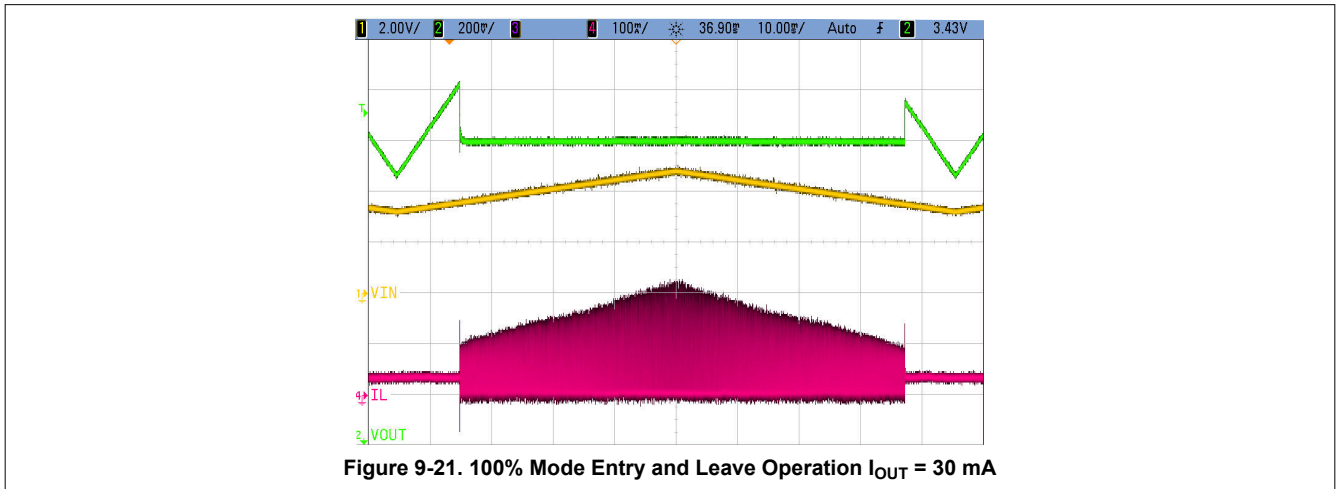


Figure 9-20. Load Transient Response; 5 mA to 290 mA

9.2.3 Application Curves (continued)



9.3 System Example

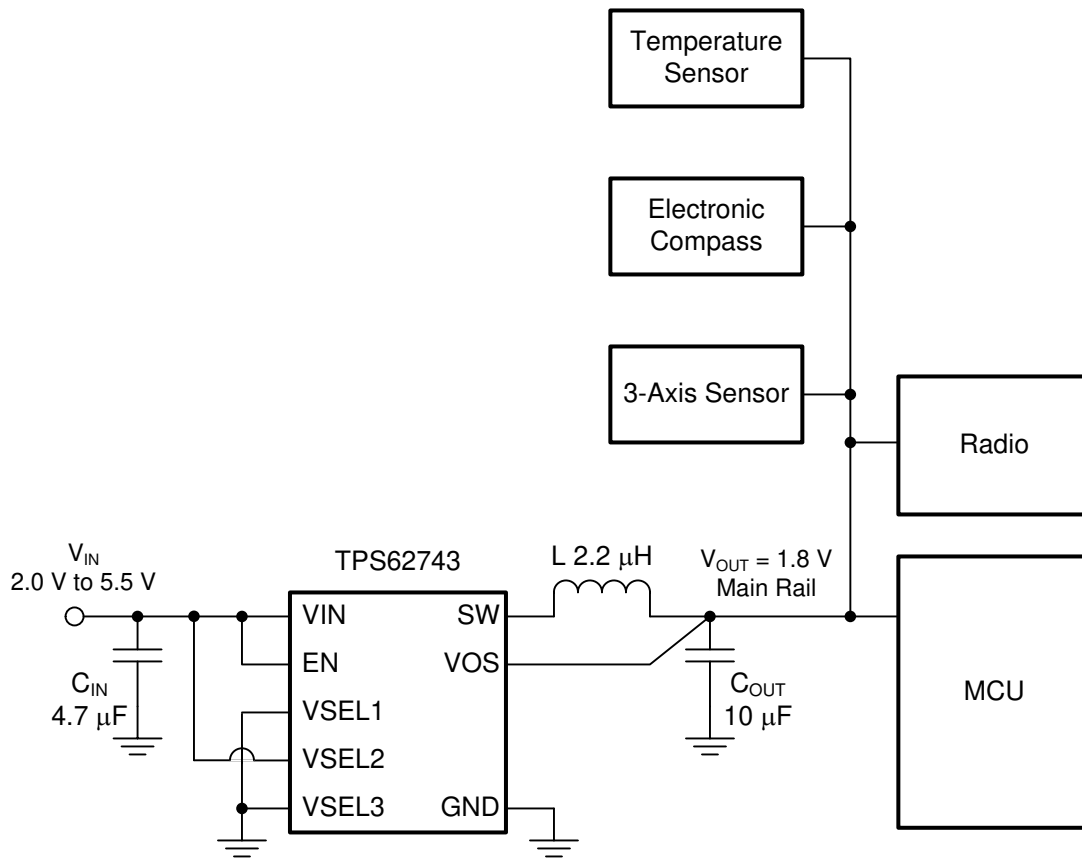


Figure 9-22. Example Of Implementation In A Master MCU Based System

10 Power Supply Recommendations

The power supply must provide a current rating according to the supply voltage, output voltage and output current of the TPS62743.

11 Layout

11.1 Layout Guidelines

- As for all switching power supplies, the layout is an important step in the design. Care must be taken in board layout to get the specified performance.
- It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths.
- The input capacitor should be placed as close as possible to the IC pins VIN and GND. This is the most critical component placement.
- The V_{OS} line is a sensitive high impedance line and should be connected to the output capacitor and routed away from noisy components and traces (e.g. SW line) or other noise sources.

11.2 Layout Example

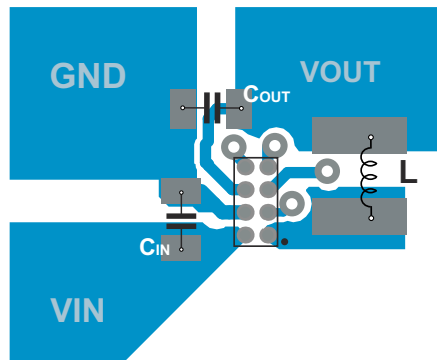


Figure 11-1. Recommended PCB Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

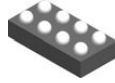
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

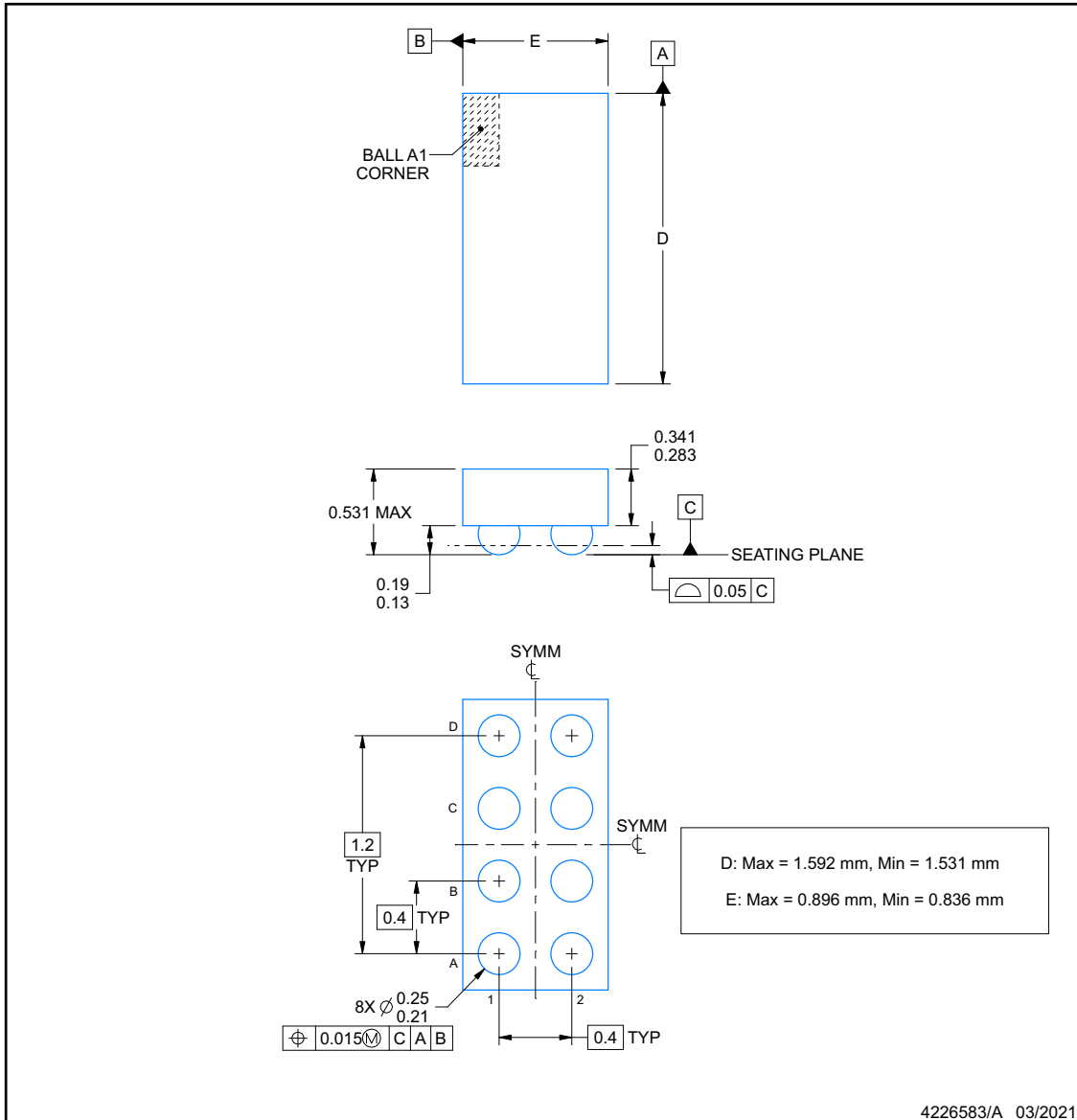


PACKAGE OUTLINE

YFP0008-C01

DSBGA - 0.531 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

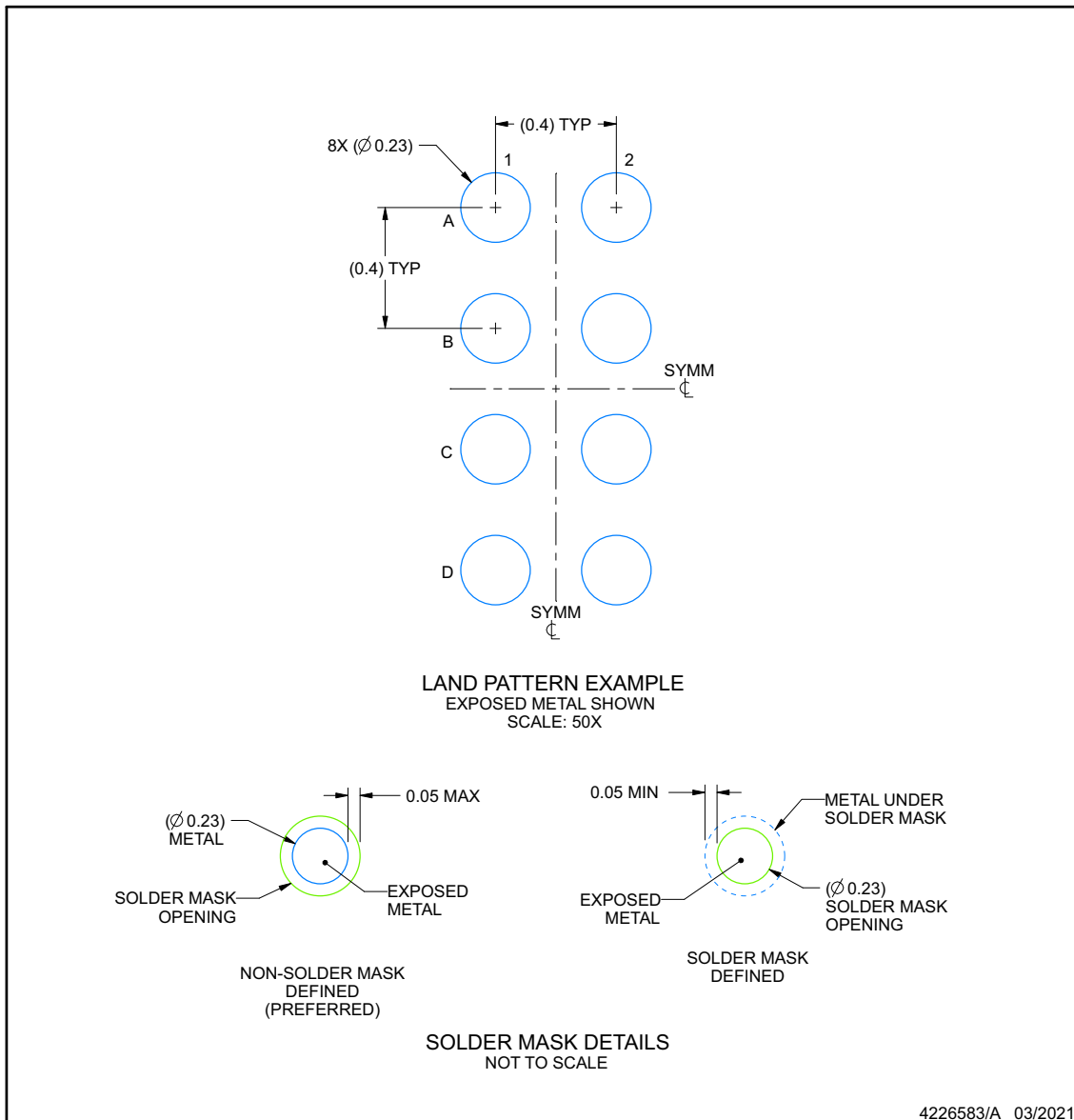
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YFP0008-C01

DSBGA - 0.531 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

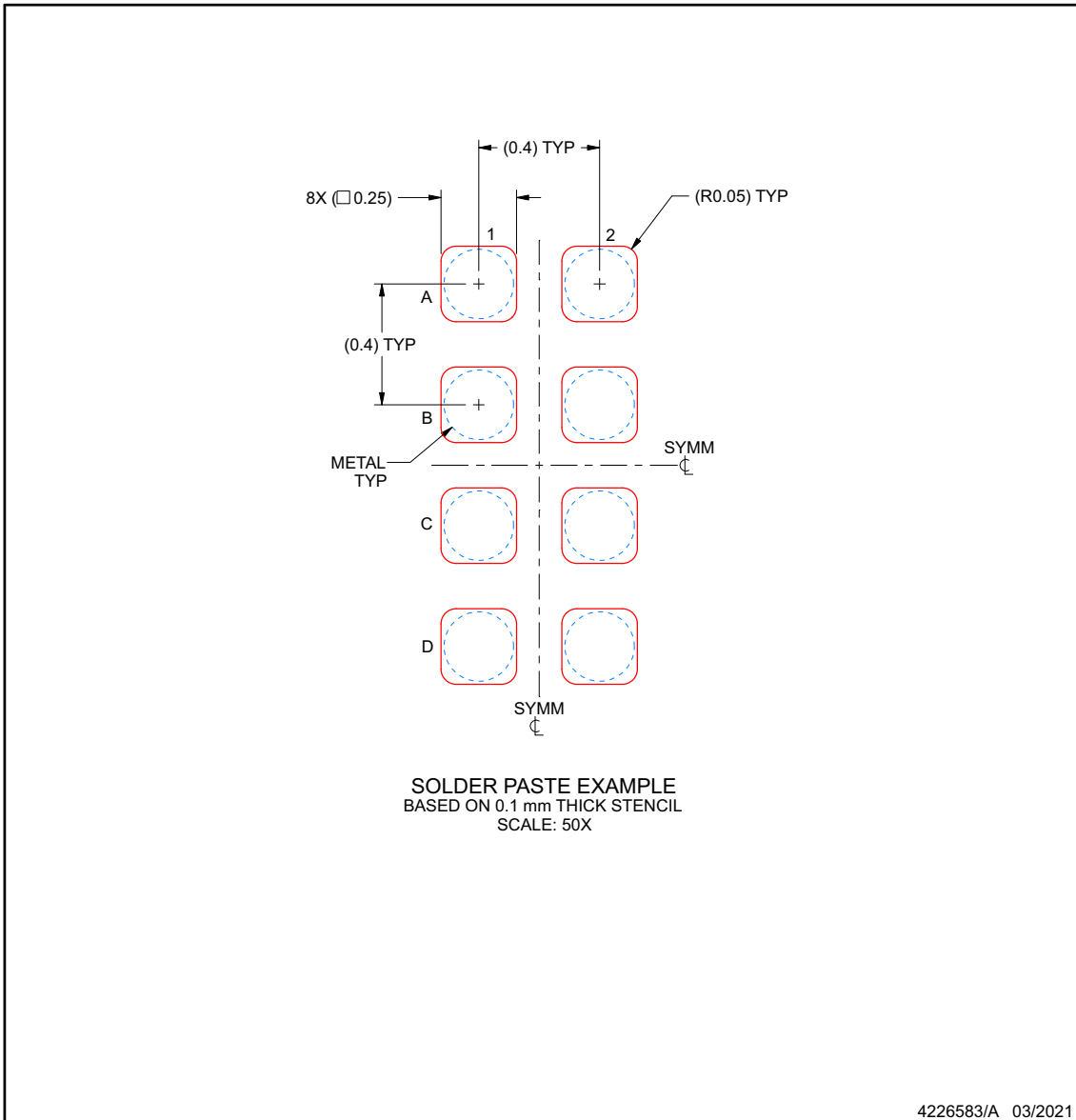
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFP0008-C01

DSBGA - 0.531 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

- 4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS627431YFPR | ACTIVE | DSBGA | YFP | 8 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 627431 | Samples |
| TPS627431YFPT | ACTIVE | DSBGA | YFP | 8 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 627431 | Samples |
| TPS62743YFPR | ACTIVE | DSBGA | YFP | 8 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | TPS743 | Samples |
| TPS62743YFPT | ACTIVE | DSBGA | YFP | 8 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | TPS743 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS627431YFPR | DSBGA | YFP | 8 | 3000 | 180.0 | 8.4 | 0.98 | 1.68 | 0.59 | 4.0 | 8.0 | Q1 |
| TPS627431YFPT | DSBGA | YFP | 8 | 250 | 180.0 | 8.4 | 0.98 | 1.68 | 0.59 | 4.0 | 8.0 | Q1 |
| TPS62743YFPR | DSBGA | YFP | 8 | 3000 | 180.0 | 8.4 | 0.98 | 1.68 | 0.59 | 4.0 | 8.0 | Q1 |
| TPS62743YFPT | DSBGA | YFP | 8 | 250 | 180.0 | 8.4 | 0.98 | 1.68 | 0.59 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS627431YFPR | DSBGA | YFP | 8 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS627431YFPT | DSBGA | YFP | 8 | 250 | 182.0 | 182.0 | 20.0 |
| TPS62743YFPR | DSBGA | YFP | 8 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS62743YFPT | DSBGA | YFP | 8 | 250 | 182.0 | 182.0 | 20.0 |

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